Sorin Cotofana

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Biography

Sorin Cotofana received the MSc degree in Computer Science from the "Politechnica" University of Bucharest, Romania, and the PhD degree in Electrical Engineering from Delft University of Technology, The Netherlands. He is currently with the Electrical Engineering, Mathematics and Computer Science Faculty, Delft University of Technology, Delft, the Netherlands. His current research is focused on: (i) the design and implementation of dependable/reliable systems out of unpredictable/unreliable components; (ii) ageing assessment/prediction and lifetime reliability aware resource management; and (iii) unconventional computation paradigms and computation with emerging nano-devices. He (co-)authored more than 250 papers in peer-reviewed international journal and conferences, and received 12 international conferences best paper awards, e.g., 2012 IEEE Conference on Nanotechnology, 2012 ACM/IEEE International Symposium on Nanoscale Architectures, 2005 IEEE Conference on Nanotechnology, 2001 International Conference on Computer Design. He served as Associate editor for IEEE Transactions on CAS I (2009-2011), IEEE Transactions on Nanotechnology (2008-2014), member of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems Senior Editorial Board (2016-2017), Steering Committee member for IEEE Transactions on Multi-Scale Computing Systems (2014-2018), Chair of the Giga-Nano IEEE CASS Technical Committee (2013-2015), and IEEE Nano Council CASS representative (2013-2014) and has been actively involved as reviewer, Technical Program Committee (TPC) member, and Program Committee (track) and General (co)-chair, in the organization of numerous international conferences. He is currently Associate Editor in Chief and Senior Editor for IEEE Transactions on Nanotechnology and Steering Committee member for IEEE Transactions on Multi-Scale Computing Systems. He is a Fellow IEEE member (Circuits and System Society (CASS) and Computer Society) and a HiPEAC member.

Lecture 1: Energy Effective Graphene Based Computing

In this presentation we argue and provide Non-Equilibrium Green's Function Landauer formalism-based simulation evidence that in spite of Graphene's bandgap absence, Graphene Nanoribbons (GNRs) can provide support for energy effective computing. We start by demonstrating that: (i) band gap can be opened by means of GNR topology and (ii) GNR's conductance can be mold according to some desired functionality, i.e., 2- and 3-input AND, NAND, OR, NOR, XOR, and XNOR, via shape and electrostatic interaction. Afterwards, we introduce a generic GNR based Boolean gate structure composed of a pull-up GNR performing the gate Boolean function and a pull-down GNR performing the gate inverted Boolean function, and, by properly adjusting GNRs' dimensions and topology, we design and evaluate by means of SPICE simulations inverter, buffer, and 2-input GNR based AND, NAND, and XOR gates. Finally, we compare the proposed gates with state-of-the-art graphene FET and CMOS based counterparts. Our analysis suggests that the GNR-based gates outperform its challengers, e.g.,

up to 6x smaller propagation delay, 2 orders of magnitude smaller power consumption, while requiring 1 to 2 orders of magnitude smaller active area footprint when compared with 7nm CMOS equivalents, which is a clear indication that they have great potential as basic building blocks for future beyond CMOS energy effective nanoscale circuits.

Man-Kay Law

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Biography

Man-Kay Law (M'11-SM'16) received the B.Sc. degree in Computer Engineering and the PhD degree in Electronic and Computer Engineering from Hong Kong University of Science and Technology (HKUST), in 2006 and 2011, respectively. From February 2011, he joined HKUST as a Visiting Assistant Professor. He is currently an Associate Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, Faculty of Science and Technology, University of Macau, Macao.

His research interests are on the development of ultra-low power sensing circuits and integrated energy harvesting techniques for wireless and biomedical applications. He developed an ultra-low power fully integrated CMOS temperature sensing passive UHF RFID tag together with Zhejiang Advanced Manufacturing Institute (ZAMI) and HKUST. He has authored and co-authored over 80 technical journals and conference papers and holds 6 U.S. patents.

Prof. Law is/has been a member of the Technical Program Committee of Asia Symposium on Quality Electronic Design, IEEE International Symposium on Circuits and Systems (ISCAS), Biomedical Circuits and Systems Conference (BioCAS), International Symposium on Integrated Circuits (ISIC), and the University Design Contest Co-Chair of Asia and South Pacific Design Automation Conference (ASPDAC). He was a co-recipient of the ASQED Best Paper Award'13, A-SSCC Distinguished Design Award'15 and ASPDAC Best Design Award'16. He also received the Macao Science and Technology Invention Award (2nd Class) by Macau Government – FDCT'14 and '18. He is a senior member of the IEEE, and serves as a technical committee member in both the IEEE CAS committee on Sensory Systems as well as Biomedical Circuits and Systems. He is currently an ITPC member of the IEEE International Solid-State Circuits Conference (ISSCC).

Lecture 1: High Efficiency Capacitive Piezoelectric Energy Harvesting Interfaces

Piezoelectric energy harvester (PEH) is one of the most promising candidate for ambient vibration energy scavenging for ubiquitous miniaturized Internet of Things (IoT) devices. Due to the PEH inherent capacitance, the extractable AC-DC electrical power in traditional PEH interface using full-bridge rectifier (FBR) is limited. Existing PEH interfaces generally employ non-linear techniques such as the parallel-synchronized-switch harvesting-on-inductor (P-SSHI) and fractional open circuit technique to enhance the extracted power and achieve efficient maximum power point tracking (MPPT). However, they typically require bulky external high-Q inductors to extend the damping duration while inducing excessive device voltage stress during MPPT. This seminar will focus on the development of recent inductor-less PEH interfaces exploiting only capacitors for flipping the PEH voltage for energy extraction improvement. It will first cover the basic operations of capacitive PEH interfaces and provide the fundamental analysis on its performance limits. The design tradeoffs between the achievable extracted

energy and the different loss mechanisms will be outlined. System level implementation of maximum power point tracking (MPPT) and output voltage regulation will also be discussed.

Lecture 2: Ultra-low Power/Energy Efficient High Accuracy CMOS Temperature Sensors for passive RFID Applications

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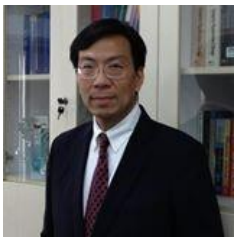
Lecture 3: Reconfigurable Fully Integrated Switched-Capacitor DC-DC Converter for IoT Applications

The recent wireless sensing and emerging Internet-of-Thing (IoT) market have enabled the development of miniaturized systems with different application requirements. While highly efficient power management is mandatory to ensure the system performance and operation lifetime, on-chip inductive power converters generally exhibits increased manufacturing cost despite of their higher achievable power densities. Due to the full integration together with high energy efficiency and adaptability, reconfigurable switched-capacitor (SC) DC-DC converters are promising for ultra-compact on-chip power solutions. This tutorial will first cover the basic operations and control methodologies of SC DC-DC converters. It will then introduce the conventional SC DC-DC topologies, followed by the fundamental analyses and different loss mechanisms. In-depth studies of different state-of-the-art topology choices for reconfigurable SC DC-DC converters capable of systematic multiple rational voltage conversion ratio (VCR) generation and their fundamental limits will be detailed. Adaptive gate driving techniques with consistent switch driving voltage while preventing reversion loss under wide voltage dynamics will also be introduced. These techniques enable highly efficient SC power converters with better SoC integration for next generation ultra-compact low-cost IoT devices.



Gwo Giun (Chris) Lee

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Biography

Chris Gwo Giun Lee is an investigator in the field of signal processing systems including multimedia and bioinformatics. His endeavors in system design, based on analytics of algorithm concurrently with analytics architecture, has made possible computations on System-on-Chip and cloud platforms in resolving complex problems with both accuracy and efficiency. Having previously held leading and managerial positions in the industry such as System Architect in former Philips Semiconductor in Silicon Valley, Lee was recruited to NCKU in 2003 where he found and is currently directing the Bioinfotronics Research Center.

Lee received his B.S. degree in electrical engineering from National Taiwan University and both his M.S. and Ph.D. degrees in electrical engineering from University of Massachusetts. He has contributed more than 130 original research and technical publications with the invention of 100+ patents worldwide.

Lee serves as the AE for IEEE TSP and Journal of Signal Processing Systems. He was formerly the AE for IEEE TCSVT for which he received the Best Associate Editor's Award in 2011.

Lecture 1: Making Healthcare More Accessible via AI: Extension of Telemedicine

This seminar will focus on innovative digital health ecosystem and analytics system which fosters extension of telemedicine through the transfer of comprehensive medical expertise and experiences via Artificial Intelligence (AI) from tertiary medical centers to remote care facilities in making healthcare more accessible! Cancer is among the most important issues of healthcare worldwide. However, under current medical systems, diagnosis of these severe diseases is commonly delayed, especially in remote locations with limited medical resources. Hence it is necessary to facilitate early screening at these distant care units using Computer-Aided-Diagnostic (CAD) tools possessing tertiary centers' experiences accumulated through AI. In attempts to reform and advance the digital health environment, using skin care as example, this seminar introduces an ecosystem, by which integration of remote care facilities in Eastern Taiwan is substantiated, with Hualien Tzuchi Medical Center as the center, through utilization of high efficiency of AI as extension of telemedicine! Being an exemplary, this AI medical networking model is readily extensible to global medical and biotech communities! This seminar will also introduce the speaker's skin analytics system for the detection of BCC with 97% accuracy using only 2,000 images whereas Stanford Medical Center reported on the diagnosis of skin cancer with 72% accuracy using ~130,000 images and Heidelberg University having 95% accuracy on melanoma detection using ~100,000 images.

Lecture 2: TUTORIAL: Algorithm/Architecture Co-design for Smart Signals and Systems in Cognitive Cloud/Edge

This seminar will focus on innovative digital health ecosystem and analytics system which fosters extension of telemedicine through the transfer of comprehensive medical expertise and experiences via Artificial Intelligence (AI) from tertiary medical centers to remote care facilities in making healthcare more accessible! Cancer is among the most important issues of healthcare worldwide. However, under current medical systems, diagnosis of these severe diseases is commonly delayed, especially in remote locations with limited medical resources. Hence it is necessary to facilitate early screening at these distant care units using Computer-Aided-Diagnostic (CAD) tools possessing tertiary centers' experiences accumulated through AI. In attempts to reform and advance the digital health environment, using skin care as example, this seminar introduces an ecosystem, by which integration of remote care facilities in Eastern Taiwan is substantiated, with Hualien Tzuchi Medical Center as the center, through utilization of high efficiency of AI as extension of telemedicine! Being an exemplary, this AI medical networking model is readily extensible to global medical and biotech communities! This seminar will also introduce the speaker's skin analytics system for the detection of BCC with 97% accuracy using only 2,000 images whereas Stanford Medical Center reported on the diagnosis of skin cancer with 72% accuracy using ~130,000 images and Heidelberg University having 95% accuracy on melanoma detection using ~100,000 images.

Andrew Mason

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Biography

Andrew J. Mason (S'90–M'99–SM'06) received the BS in Physics with highest distinction from Western Kentucky University in 1991, the BSEE with honors from the Georgia Institute of Technology in 1992, and the MS and Ph.D. in Electrical Engineering from The University of Michigan, Ann Arbor in 1994 and 2000, respectively. From 1999 to 2001 he was an Assistant Professor at the University of Kentucky. In 2001 he joined the Department of Electrical and Computer Engineering at Michigan State University in East Lansing, Michigan, where he is currently a Professor. His research explores mixed-signal circuits, microfabricated structures and machine learning algorithms for integrated microsystems in biomedical, environmental monitoring and sustainable lifestyle applications. Current projects are focused on design of augmented human awareness systems including signal processing algorithms and hardware for brain-machine interface, wearable/implantable biochemical and neural sensors, and lab-on-CMOS integration of sensing, instrumentation, and microfluidics.

Dr. Mason is a Senior Member of the Institute of Electrical and Electronic Engineers (IEEE) and serves on the Sensory Systems and Biomedical Circuits and Systems Technical Committees of the IEEE Circuits and Systems Society. He is an Associate Editor for the IEEE Trans. Biomedical Circuits and Systems and regularly serves on the technical and review committees for several IEEE conferences. Dr. Mason was co-General Chair of the 2011 IEEE Biomedical Circuits and Systems Conference. He is a recipient of the 2006 Michigan State University Teacher-Scholar Award and the 2010 Withrow Award for Teaching Excellence.

Lecture 1: Augmented Perception: Next Generation Wearables and Human-Machine Interfaces

Products like Fitbit and the Apple Watch have brought to the public decades of foundational work on wearable technologies achieved by researchers in the IEEE CAS Society and related groups. Similarly, research into brain- and human-machine interface is starting to enter the public domain in applications including deep brain stimulation, prosthetic limb control, and human assistive devices. While researchers continue to explore new wearable sensing and human-interface paradigms, it is vital that we also explore what applications the next generation of wearable human-machine interfaces can and should enable. This talk will review key challenges and approaches within wearable assistive device and brain/human interface technologies. Aspects of physiological, environmental, and behavioral sensing within wearable platforms will be discussed, and technical challenges such as miniaturization, power efficiency and artifact removal will be highlighted. Approaches to brain-machine interface and human assistive technologies will, likewise, be analyzed. Finally, the next generation concept of augmented human perception, real time machine-enhanced awareness that expands natural

human senses, will be introduced. Utilizing wearable sensing and real-time feedback through visual, audio and tactile mechanism, augmented perception is poised to revolutionize the human experience, enhance daily performance, and enable new pathways to address mental and physical health concerns.

Keshab Parhi

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Biography

Keshab Parhi (Fellow'1996) received the B.Tech. degree from the Indian Institute of Technology (IIT), Kharagpur, in 1982, the M.S.E.E. degree from the University of Pennsylvania, Philadelphia, in 1984, and the Ph.D. degree from the University of California, Berkeley, in 1988. He has been with the University of Minnesota, Minneapolis, since 1988, where he is currently Distinguished McKnight University Professor and Edgar F. Johnson Professor in the Department of Electrical and Computer Engineering. He has published 600 papers, is the inventor of 29 patents, and has authored the textbook VLSI Digital Signal Processing Systems (Wiley, 1999) and coedited the reference book Digital Signal Processing for Multimedia Systems (Marcel Dekker, 1999). Dr. Parhi is widely recognized for his work on high-level transformations of iterative data-flow computations, for developing a formal theory of computing for design of digital signal processing systems, and for his contributions to multi-gigabit Ethernet systems on copper and fiber and for backplanes. His current research addresses VLSI architecture design of signal processing systems, hardware security, and molecular computing. He is also currently working on intelligent classification of biomedical signals and images, for applications such as seizure prediction and detection, schizophrenia classification, biomarkers for mental disorders, brain connectivity, and diabetic retinopathy screening. Dr. Parhi is the recipient of numerous awards including the 2017 Mac Van Valkenburg award and the 2012 Charles A. Desoer Technical Achievement award from the IEEE Circuits and Systems Society, the 2004 F. E. Terman award from the American Society of Engineering Education, the 2003 IEEE Kiyo Tomiyasu Technical Field Award, the 2001 IEEE W. R. G. Baker prize paper award, and a Golden Jubilee medal from the IEEE Circuits and Systems Society in 2000. He is a Fellow of IEEE (1996) and the American Association for Advancement of Science (AAAS) (2017). He served as the Editor-inChief of the IEEE Trans. Circuits and Systems, Part I during 2004-2005, as Chair of the VLSI Systems and Applications Technical Committee during 2002-2004, and as an elected member of the Board of Governors of the IEEE Circuits and Systems society from 2005 to 2007.

Lecture 1: Machine Learning Systems: Low-Energy VLSI Architectures and Applications

Machine learning and data analytics continue to expand the fourth industrial revolution and affect many aspects of our lives. This talk will explore machine learning applications in data-driven neuroscience, and low-energy implementations of machine learning systems. Data-driven neuroscience can exploit machine learning approaches including deep learning to generate hypotheses associated with biomarkers for specific neuro-psychiatric disorders. In the first part, I will talk about use of machine learning to find biomarkers for epilepsy and adolescent mental disorders such as borderline personality disorder (BPD), using electroencephalogram (EEG) and functional magnetic resonance imaging (fMRI), respectively. In the second part of the talk, I will talk about approaches for energy-efficient implementations for both traditional

machine learning and deep learning systems. I will talk about the roles of feature ranking and incremental-precision approaches to reduce energy consumption of traditional machine learning systems. I will then talk about our recent work on Perm-DNN based on permuted-diagonal interconnections in deep convolutional neural networks and how structured sparsity can reduce energy consumption associated with memory access in these systems.

Lecture 2: Hardware Security: Authentication and Functional Encryption.

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Nan Sun

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Biography

Nan Sun is Associate Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin. He received the B.S. degree from Tsinghua University, Beijing, China in 2006, where he ranked top and graduated with the highest honor. He received the Ph.D. degree from Harvard University in 2010. Dr. Sun received the NSF Career Award in 2013, and the Jack Kilby Research Award from UT Austin in both 2015 and 2016. He holds the AMD Endowed Development Chair from 2013 to 2017. He serves on the Technical Program Committee of the IEEE Custom Integrated Circuits Conference and the IEEE Asian Solid-State Circuit Conference. He is an Associate Editor of the IEEE Transactions on Circuits and Systems – I: Regular Papers, and a Guest Editor of the IEEE Journal of Solid-State Circuits. He also serves as IEEE Circuits-and-Systems Society Distinguished Lecturer from 2019 to 2020

Lecture 1: When SAR meets sigma-delta - Hybridization of SAR and sigma-delta ADCs

SAR is widely used for medium resolution applications due to its simplicity, scaling compatibility, and low-power consumption. However, its power efficiency degrades as the resolution increases due to its tight requirement on the comparator noise and the exponentially growing capacitor DAC array. By contrast, DS ADC is a popular architecture for high-resolution applications. Taking advantage of noise shaping, it can achieve high resolution with a low-resolution quantizer and DAC. However, it typically requires the use of op-amps that are power hungry and scaling unfriendly. This talk will present latest hybrid ADCs that aim to combine the merits of SAR and DS while simultaneously obviating their drawbacks. After providing a high-level review of published works, this talk will take a deep dive into two interesting noise-shaping SAR ADC architectures. The first one uses fully passive switched-capacitor filter to achieve 2nd-order noise shaping. It is fully dynamic and can be easily duty cycled. In addition, it is robust and calibration free. Thus, it is well suited for low-power sensor applications. The second one adopts an error-feedback structure, which simplifies the filter design. It consumes very low power by using a dynamic amplifier and address its process, voltage, and temperature (PVT) sensitivity via a fast-convergence background calibration loop.

Lecture 2: New Ingredients in the Pot - Rethink Analog IC Design

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Lecture 3: Handheld CMOS NMR Biosensor

This talk will showcase how silicon RF chips can be used not only for wireless RF applications, but also for biomolecular sensing aimed at low-cost disease screening. The main function of the RF chip is to manipulate and monitor the dynamics of protons in water via nuclear magnetic resonance (NMR). Target biological objects such as cancer marker proteins alter the proton dynamics, which is the basis for the biosensing. The high sensitivity of the RF chip made possible the construction of an entire NMR system around the RF chip in a 100-g platform, which is 1200 times lighter, yet 150 times more spin-mass sensitive than a state-of-the-art commercial benchtop NMR system. The system can become a useful addition in pursuing disease detection in a low-cost, hand-held platform.

Lecture 4: Time-Domain Analog Signal Processing - Building ADCs using Ring Oscillators

The conventional way to design analog and mixed-signal circuits relies heavily on the use of operational amplifiers (op-amps) to process signals in the voltage domain (VD). This well-established VD analog signal processing (ASP) scheme encounters severe difficulties in advanced nanometer-scale CMOS processes due to reduced supply voltage and transistor intrinsic gain. As a result, traditional VD AMS circuits still require thick-oxide long-channel transistors and large supply voltages, resulting in increased cost/area and significant performance penalties in power and speed. The advent of nanometer CMOS technology calls for a new ASP framework that not only does not suffer from scaling but actually benefit from it. This talk presents scaling-friendly time-domain (TD) ASP circuits that can make use of simple digital logic gates (e.g., inverter, XOR, and latch) to process analog information. In TD circuits, the analog information is represented not by voltage, but by time. As the technology advances, the transistor speed keeps increasing and the inverter delay keeps shrinking, leading to higher timing resolution and wider TD dynamic range. This talk reviews the historical development of TD ASP circuits, as well as its latest exciting progresses. Specifically, this talk focuses on the design of TD analog-to-digital converters (ADCs) using ring oscillators that can perform TD integration and quantization.

Chua-Chin Wang

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Biography

Dr. Chua-Chin Wang received the Ph.D. degree in electrical engineering from SUNY (State University of New York) at Stony Brook, USA, in 1992. He then joined Department of Electrical Engineering, National Sun Yat-Sen University (NSYSU), Taiwan. He was Chairman of this department during 2009 - 2012. He was CEO of Operation Center of Industry-University Cooperation, NSYSU, in 2012-2014. He was appointed to be VP of Office of Industrial Collaboration and Continuing Education Affairs, from Aug. 2014 to 2015. He was elected as Dean of Engineering College during 2014-2017. He is now Director of Underwater Vehicle R&D Center.

Dr. Wang's research interests include memory and logic circuit design, communication circuit design, bio-medical circuits, and particularly interfacing I/O circuits. He also won Distinguished Electrical Engineering Professor Award of Chinese Institute of Electrical Engineers in 2007. In 2010, he was honored to be Distinguished Professor of National Sun Yat-Sen University. In 2012, he won "Distinguished Engineering Professor" Award of Chinese Institute of Engineers and Outstanding Research Award of NSYSU. He became IET Fellow in 2012. He was named as ASE Chair Professor in 2013 for the recognition of his achievement in the area of VLSI design and contribution to industry technology development. He won Outstanding Technical Achievement Award of IEEE Tainan Section in 2018.

Prof. Wang has devoted himself for many IEEE services. He was Tainan Chapter Chair of IEEE Circuits and Systems Society (CASS) in 2007-2008. He was also the founding Tainan Chair of IEEE Solid-State Circuits Society (SSCS) for 2007-2008, and the founding Consultant of IEEE NSYSU Student Branch. He was elected to be Vice Chair of IEEE Tainan Section in 2012. He was elected to be Chair of IEEE CASS Nanoelectronics and Giga-scale Systems (NG) Technical Committee to serve during 2008-2009. He has been invited to be Associate Editors of IEEE Trans. on TCAS-I (2010-2013) and TCAS-II (2010-2011). He was General Chair of 2012 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), which is the flagship conference of IEEE CASS Region 10.

Lecture 1: Nano-scale CMOS Mixed-voltage Digital I/O Buffer Design Methodology

Ever since the reliability issues caused by I/O (input/output) compatibility among chips fabricated using different processes were raised by cellular phone makers during mid-2000, on-silicon mixed-voltage I/O buffer with wide voltage tolerance was considered better solution than using signal level converters to shrink PCB size, number of discrete, and power consumption. However, various external voltages on I/O pad result in body effect, leakage, hot-carrier degradation, and gate-oxide overstress in stacked transistors of mixed-voltage I/O. What even worse is that slew rate (SR) was also found deteriorated by PVT (Process, Voltage, Temperature) variations. Therefore, many design techniques for CMOS mixed-voltage I/O buffer design using nano-scale CMOS processes will be introduced and analyzed, including

Clamping Dynamic Gate Bias Generator, Dynamic Biasing, and Leakage Detection, such that these I/O buffers will be able to transmit and receive digital signal with 2x or even 3x VDD voltage swing. Moreover, the reliability design consideration for the digital I/O buffers, including ESD, PVT detection, and slew rate (SR) auto-adjustment will also be discussed as well. Moreover, the maximum data rate can be drastically enhanced to meet the latest I/O interfacing protocol requirements.

Lecture 2: TUTORIAL: How to Design High-Speed Nano-scale CMOS Mixed-voltage Digital I/O Buffer with Reliable Slew Rate Insensitive to PVTL

Ever since the reliability issues caused by I/O (input/output) compatibility among chips fabricated using different processes were raised by cellular phone makers during mid-2000, on-silicon mixed-voltage I/O buffer with wide voltage tolerance was considered better solution than using signal level converters to shrink PCB size, number of discrete, and power consumption. However, various external voltages on I/O pad result in body effect, leakage, hot-carrier degradation, and gate-oxide overstress in stacked transistors of mixed-voltage I/O. What even worse is that slew rate (SR) was also found deteriorated by PVT (Process, Voltage, Temperature) variations. Therefore, many design techniques for CMOS mixed-voltage I/O buffer design using nano-scale CMOS processes will be introduced and analyzed, including Clamping Dynamic Gate Bias Generator, Dynamic Biasing, and Leakage Detection, such that these I/O buffers will be able to transmit and receive digital signal with 2x or even 3x VDD voltage swing. Moreover, the reliability design consideration for the digital I/O buffers, including ESD, PVT detection, and slew rate (SR) auto-adjustment will also be discussed as well. Moreover, the maximum data rate can be drastically enhanced to meet the latest I/O interfacing protocol requirements.

Jerald Yoo

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Biography

Jerald Yoo (S'05-M'10-SM'15) received the B.S., M.S., and Ph.D. degrees in Department of Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2002, 2007, and 2010, respectively.

From 2010 to 2016, he was with the Department of Electrical Engineering and Computer Science, Masdar Institute, Abu Dhabi, United Arab Emirates, where he was an Associate Professor. Since 2017, he has been with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, where he is currently an Associate Professor. He has pioneered researches on low-energy body-area-network (BAN) transceivers and wearable body sensor network using the planar-fashionable circuit board for continuous health monitoring system. He authored book chapters in IoT Physical Layer – Design and Implementation (Springer, 2019), Enabling the Internet of Things—From Circuits to Networks (Springer, 2017) and in Biomedical CMOS ICs (Springer, 2010). His current research interests include low-energy circuit technology for wearable bio signal sensors, flexible circuit board platform, BAN transceivers, ASIC for piezoelectric Micromachined Ultrasonic Transducers (pMUT) and System-on-Chip (SoC) design to system realization for wearable healthcare applications.

Dr. Yoo is the recipient or a co-recipient of several awards: the IEEE International Circuits and Systems (ISCAS) 2015 Best Paper Award (BioCAS Track), ISCAS 2015 Runner-Up Best Student Paper Award, the Masdar Institute Best Research Award in 2015 and the IEEE Asian Solid-State Circuits Conference (A-SSCC) Outstanding Design Awards (2005). He was the Vice Chair of IEEE Solid-State Circuits Society (SSCS) United Arab Emirates (UAE) Chapter. Currently, he serves as a Technical Program Committee Member of the IEEE A-SSCC, IEEE Custom Integrated Circuits Conference (CICC), and the IEEE International Solid-State Circuits Conference (ISSCC) Student Research Preview (SRP). He is also an Analog Signal Processing Technical Committee Member of IEEE Circuits and Systems Society. Dr. Yoo is an IEEE Circuits and Systems Society (CASS) Distinguished Lecturer. He also served as the IEEE Solid-State Circuits Society (SSCS) Distinguished Lecturer (2017-2018).

Lecture 1: Body Area Network – Connecting things together around the body

Chronic diseases account for over 1/3 of deaths around the world. To mitigate the impact of such diseases, healthcare paradigm is now shifting from reactive illness management towards proactive and preemptive health management; the goal here is to maintain a healthy life in the first place or to prevent illness from getting any worse by continuously monitoring health during normal daily life. Body Area Network (BAN) is an attractive means for continuous and pervasive health monitoring, yet its unique and harsh environment gives circuit designers many

challenges. As human body absorbs the majority of RF energy around GHz band, existing RF radio may not be an ideal for communications between and on-body sensors.

In order solve the issues, this talk presents the Body Coupled Communication (BCC)-based BAN. BCC BAN utilizes human body itself as a communication medium, which has orders of magnitude less pathloss when compared to RF based BAN. We will begin with channel characteristics, followed by design considerations and transceiver implementation examples. I will then discuss what circuit designers should consider in such non-conventional environments. Low energy circuit techniques to overcome their limitations will also be discussed. We will then will review their various system aspects.

Lecture 2: On-Chip Epilepsy Detection: Where Machine Learning Meets Wearable, Patient-Specific Wearable Healthcare

Epilepsy is a severe and chronic neurological disorder that affects over 65 million people worldwide. Yet current seizure/epilepsy detection and treatment largely relies on a physician interviewing the subject, which is not effective in infant/children group. Moreover, patient-to-patient and age-to-age variation on seizure pattern makes such detection particularly challenging. To expand the beneficiary group to even infants, and to effectively adapt to each patient, a wearable form-factor, patient-specific system with machine learning is of crucial. However, the wearable environment is challenging for circuit designers' due unstable skin-electrode interface, huge mismatch, and static/dynamic offset.

This lecture will cover the design strategies of patient-specific epilepsy detection System-on-Chip (SoC). We will first explore the difficulties, limitations and potential pitfalls in wearable interface circuit design, and strategies to overcome such issues. Starting from a 1 op-amp instrumentation amplifier (IA), we will cover various IA circuit topologies and their key metrics to deal with offset compensation. Several state-of-the-art instrumentation amplifiers that emphasize on different parameters will also be discussed. Moving on, we will cover the feature extraction and the patient-specific classification using Machine Learning technique. Finally, an on-chip epilepsy detection and recording sensor SoC will be presented, which integrates all the components covered during the lecture. The lecture will conclude with interesting aspects and opportunities that lie ahead.

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Biography

Ce Zhu is currently a Professor with the School of Information and Communication Engineering, University of Electronic Science and Technology of China, Chengdu, China. His research interests include image/video coding and communications, 3D video, visual analysis and understanding, visual perception and applications. He has served on the editorial boards of a few journals, including as an Associate Editor of IEEE Transactions on Image Processing, IEEE Transactions on Circuits and Systems for Video Technology, IEEE Transactions on Broadcasting, IEEE Signal Processing Letters, and IEEE Communications Surveys and Tutorials. He is a Fellow of the IEEE and a Fellow of the IET. For more information, please visit his homepage at http://www.avc2-lab.net/~eczhu

Lecture 1: Towards Global Rate Distortion Optimization in Video Coding: Recent Developments

The past decades have witnessed great advancement of video coding techniques and their wide applications in video storage and communications, where rate-distortion optimization (RDO) plays a crucial role to maximize coding efficiency in video coding. In the current block-based hybrid video coding framework, the RDO is typically performed on the block level individually and independently, which is far from being optimal as it ignores the strong spatial-temporal dependency. However, a global RDO problem becomes so complex that the processing of each coding unit is dependent and entangled with each other due to the extensive use of spatial-temporal predictions in video coding. In the talk, I will discuss the challenges of achieving global RDO in one-pass video coding and present our recent work considering the temporal dependency on top of the video coding standards H.264/AVC and HEVC, respectively.

Lecture 2: TUTORIAL: Rate Distortion Optimization in Video Coding: from Local to Global

The past decades have witnessed great advancement of video coding techniques and their wide applications in video storage and communications, where rate-distortion optimization (RDO) plays a crucial role to maximize coding efficiency in video coding. In the current block-based hybrid video coding framework, the RDO is typically performed on the block level individually and independently, which is far from being optimal as it ignores the strong spatial-temporal dependency. However, a global RDO problem becomes so complex that the processing of each coding unit is dependent and entangled with each other due to the extensive use of spatial-temporal predictions in video coding. In the talk, I will discuss the challenges of achieving global RDO in one-pass video coding and present our recent work considering the temporal dependency on top of the video coding standards H.264/AVC and HEVC, respectively.