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Lecture #1: Challenges in Circuits and Systems for Emerging Memory Based Energy-Efficient Intelligent Electronics

Memory has become one of the bottlenecks in the development of intelligent computing systems with high bandwidth and low energy consumption. This seminar will address trends in the development of emerging memory, including resistive RAM (ReRAM), STT-MRAM, and phase-change memory (PCM) for intelligent electronics. The fundamental circuits of nonvolatile memory (NVM) and eNVM will be introduced. This seminar will explore the challenges faced by researchers in the circuit designs, circuit-device-interaction, and architecture-circuit interactions for emerging memory. The 2nd part of this seminar will explore the implementation of emerging memory beyond conventional memory applications, such as nonvolatile-logics (nvLogics), nonvolatile processors, and neuromorphic computing for deep learning and artificial intelligent (AI) chips.

Lecture #2: Challenges and Trends of Memory Circuit Designs for Energy-Efficient IoT Devices

Memory has become one of the bottlenecks in the development of IoT and wearable devices with low energy consumption. This seminar addresses trends in the development of on-chip (embedded) volatile and nonvolatile memory (NVM) for energy-efficient IoT applications. In the first part, this talk will examine the challenges and trends in achieving low-voltage operation for embedded SRAM. Then, this talk will review silicon-verified circuit techniques for low-VDD SRAMs. The 2nd part of this seminar will introduce a variety of nonvolatile memory (NVM) technologies, including ROM, Flash, resistive RAM (ReRAM), phase-change memory (PCM), and STT-MRAM. This seminar will explore the challenges and silicon verified solutions in the design of low-power and high-speed circuits for on-chip NVM macros.

Biography

Dr. Marvin Chang is a full Professor in the Dept. of Electrical Engineering of National Tsing Hua University (NTHU), Taiwan. Since 2011, he has also served as the Associate Executive Director of National Program for Intelligent Electronics (NPIE) in Taiwan. Dr. Change obtained considerable practical experience before joining NTHU in 2006, having spent more than ten years working in industry.
Between 1997 and 2006, Dr. Chang worked in the development of SRAM/ROM/Flash macros/compilers at Mentor Graphics (New Jersey, US), TSMC (Taiwan), and the Intellectual Property Library Company (Taiwan). His research interests include circuit design for volatile and nonvolatile memory, 3D-Memory, spintronics logics, circuit-device-interactions in non-CMOS devices, computing-in-memory, memristor circuits, and neuromorphic circuits for deep learning and artificial intelligent chips.

Since 2010, Dr. Chang has authored or co-authored more than 50+ conference papers (including ISSCC, VLSI Symposia, IEDM, DAC) as well as 30+ IEEE journal papers and 30+ US patents. He is an associate editor for IEEE TVLSI, IEEE TCAD and IEICE Electronics. He has been serving on technical program committees for ISSCC, IEDM, A-SSCC, CASS, and numerous international conferences. He is a Distinguished Lecture (DL)

speaker for IEEE Circuits and Systems Society (CASS) during 2017-2018. He received numerous awards on research and industrial collaboration from Taiwan government, Academia Sinica, NTHU, Taiwan National Chip Implementation Center (CIC), the Macronix Golden Silicon Awards, and ITRI.

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Lecture #1: Next-Generation Sigma-Delta Converters: Trends and Challenges in a Digital-Driven World

This lecture presents an overview of emerging circuits and systems techniques, which are at the forefront of the state of the art in Sigma-Delta Modulators (ΣΔMs), giving rise to a new generation of data converters that will enable an efficient implementation of the so-called software-defined-electronics paradigm. A number of trends, design challenges and new approaches – like RF/GHz-range ΣΔ digitization in wireless transceivers, digital-assisted analog circuits, time/frequency-to-digital conversion and hybrid ΣΔ/Nyquist-rate Analog-to-Digital Converters (ADCs) – are discussed, as well as the implications derived from their integration in deep nanometer CMOS technologies. Main limitations and problems faced by cutting-edge designs are identified, giving a didactic explanation of them, well supported by an exhaustive statistics-based analysis of over 500 outstanding ΣΔM Integrated Circuits (ICs) in the frontiers of data conversion. Main tendencies, research opportunities and perspectives on the evolution of data converters are envisioned, highlighting how ΣΔM-based analog/digital interfaces can improve their performance and efficiency in an increasingly digital-driven world.

Tutorial #2: Designing Sigma-Delta Data Converters: From Theory Foundations to Chip Implementation

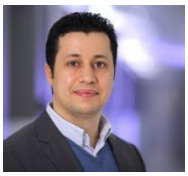
Data converters are key enablers for the feasible implementation of future cyber-physical systems connected in the so-called Internet-of-Things (IoT), where the analog/digital (A/D) interface constitutes in the majority of cases the main design bottleneck. Compared with other data converter architectures – such as SAR or Pipeline – ΣΔ ADCs cover one of the widest resolution-vs-speed conversion regions, being the most efficient solution to digitize diverse types of signals in many diverse applications – from ultra-low-power biomedical devices to ultra-wide-band communications. This versatility, together with their robustness to inaccurate analog integrated components, are some of the reasons why many engineers nowadays, in both industry and academia, consider ΣΔMs as their first choice for their designs.
This tutorial presents a systematic and practical design guide of high-performance ΣΔMs – going from specifications and system-level concepts to silicon integration, prototyping and experimental characterization. A number of demonstration vehicles, case studies, and test benches are given to illustrate practical issues and design trade-offs, covering the whole design flow of ΣΔMs – from initial theory and behavioral modeling, to transistor-level and layout design, chip implementation, and experimental measurements. The tutorial contents are structured by following a step-by-step approach, where attendees can learn many design tricks and recipes that can be applied to their own projects.

Biography

José M. de la Rosa received the M.S. degree in Physics in 1993 and the Ph.D. degree in Microelectronics in 2000, both from the University of Seville, Spain. Since 1993 he has been working at the Institute of Microelectronics of Seville (IMSE), which is in turn part of the Spanish Microelectronics Center (CNM) of the Spanish National Research Council (CSIC), where he heads a research group on micro/nanoelectronics. He is also with the Department of Electronics and Electromagnetism of the University of Seville, where he is currently a Full Professor.

His main research interests are in the field of analog and mixed-signal integrated circuits, including analysis, modeling and design automation of such circuits. In these topics, Dr. de la Rosa has participated in a number of National and European research and industrial projects, and has co-authored 5 books and more than 200 international peer-reviewed publications, including journal and conference papers and book chapters.

Dr. de la Rosa is an *IEEE Senior Member* and a member of the *Analog Signal Processing Technical Committee* of the *IEEE Circuits and Systems Society*. He serves as Deputy Editor in Chief of the *IEEE Transactions on Circuits and Systems – II: Express Briefs* (term 2016-2017) and he has served as Associate Editor for *IEEE Transactions on Circuits and Systems I: Regular Papers* since 2012 to 2015. During his term as AE of IEEE TCAS-I, he received the 2012-2013 Best Associate Editor Award, and served as Guest Editor of the Special Issue on *Custom Integrated Circuits Conference (CICC)* in 2013 and 2014. He has also served as Guest Editor of the *Special Issue of the IEEE J. on Emerging and Selected Topics in Circuits and Systems on Next-Generation Delta-Sigma Converters*. He has participated in the organizing and technical committees of a number of IEEE conferences, including ISCAS, MWSCAS, ICECS, LASCAS and VLSI-SoC, and served as TPC chair of MWSCAS'12, ICECS'12 and LASCAS'15. He has been appointed as *IEEE-CAS Society Distinguished Lecturer* for the term 2017-2018.



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Lecture #1: The Bio-Inspired Artificial Pancreas for Treatment of Diabetes

Our body is capable of glucose homeostasis through the use of insulin, a hormone secreted from an organ called the pancreas. Type 1 diabetes is an auto-immune disease that affects the pancreas by destroying the insulin-secreting beta-cells. This results in elevated glucose concentrations which in turn cause organ damage, including retinopathy leading to blindness, nephropathy leading to kidney failure, neuropathy which is irreversible nerve damage in addition to affecting quality of life. Type 1 diabetes currently affects 10% of the 285 million people suffering from diabetes and its incidence is increasing.

To intensively manage diabetes there is a need for an artificial equivalent to the pancreas which is capable of continually sensing glucose from the blood, which rises after a meal, and releasing insulin. In this talk I will present my development of the bio-inspired artificial pancreas, a closed-loop system that replicates the functionality of the biological pancreas to achieve real-time glucose control. At the heart of the device lies the silicon beta-cell, a microchip which replicates the behaviors of the beta-cells of the pancreas and when connected to a glucose sensor, calculates and continually delivers the amount of insulin needed to achieve a healthy glucose control, improving quality of life and ultimately reducing

all the secondary complications. This device is currently being worn by diabetic subjects and I will show results of our ongoing human clinical trials conducted in the UK.

Tutorial #2: CMOS Design for DNA Detection Using Ion-Sensitive Field Effect Transistors

In the last decade, we have seen application of CMOS technology in healthcare providing novel solutions for early detection, diagnosis and therapy of disease. Specifically, in the area of DNA sensing and full genome sequencing, whereby the implementation of chemical sensors called Ion-Sensitive Field Effect Transistors (ISFETs) directly in CMOS, has enabled the design of large-scale arrays of millions of sensors which can conduct in-parallel detection of DNA. Furthermore, the scaling of CMOS with Moore's law and the integration capability with microfluidics has enabled commercial efforts to make full genome sequencing affordable by companies such as Ion-Torrent and DNA electronics.
In this tutorial, I will first present the fundamentals and physical properties of DNA and how it can be detected using different modalities through the use of CMOS technology. I will then walk the audience through the design of ISFET sensors and instrumentation in CMOS working towards implementing large scale arrays which are currently being used in commercial systems. By the end of the tutorial the audience will have a good understanding of DNA and how it may be sensed in CMOS in addition to the challenges and solutions to be able to design large scale ISFET arrays for DNA detection systems.
Tutorial table of contents:

- DNA and its physical properties
- Applications of detecting DNA
- Methods of sensing DNA
- Ion-Sensitive Field Effect Transistors (ISFETs)
- Principle of operation and non-idealities
- Design of ISFETs in CMOS
- Design of Instrumentation
- State of the art ISFET arrays

Biography

Pantelis Georgiou currently holds the position of Senior Lecturer at Imperial College London within the Department of Electrical and Electronic Engineering. He is the head of the Bio-inspired Metabolic Technology Laboratory in the Centre for Bio-Inspired Technology; a multi-disciplinary group that invents, develops and demonstrates advanced micro-devices to meet global challenges in biomedical science and healthcare. His research includes ultra-low power micro-electronics, bio-inspired circuits and systems, lab-on-chip technology and application of micro-electronic technology to create novel medical devices. One of his key research areas is new technologies for treatment of diabetes such as the artificial pancreas but also develops novel Lab-on-Chip technology with application in genomics and diagnostics targeted towards infectious disease and antimicrobial resistance (AMR), in addition to wearable technologies for rehabilitation of chronic conditions.

Dr. Georgiou graduated with a 1st Class Honors MEng Degree in Electrical and Electronic Engineering in 2004 and Ph.D. degree in 2008 both from Imperial College London. He then joined the Institute of Biomedical Engineering as Research Associate until 2010, when he was appointed Head of the Bio-inspired Metabolic Technology Laboratory. In 2011, he joined the Department of Electrical & Electronic Engineering, where he currently holds an academic faculty position. He conducted pioneering work on the silicon beta cell and is now leading the project forward to the development of the first bio-inspired artificial pancreas for treatment of Type I diabetes. In addition to this, he made significant contributions to the development of integrated chemical-sensing systems in CMOS. He has pioneered the development of the Ion-Sensitive Field Effect Transistor, an integrated pH sensor which is currently being used in next generation DNA sequencing machines, demonstrating for the first time its use in low-

power weak-inversion, and its capability in a multimodal sensing array for Lab-on-Chip applications. Dr. Georgiou is a senior member of the IEEE and IET and serves on the BioCAS and Sensory Systems technical committees of the IEEE CAS Society. He is an associate editor of the IEEE Sensors and TBioCAS journals. He is also the CAS representative on the IEEE sensors council. In 2013 he was awarded the IET Mike Sergeant Achievement Medal for his outstanding contributions to engineering and development of the bio-inspired artificial pancreas.

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Lecture #1: Secured Microchip Design: Side Channel Attack and its Countermeasure

Banking, defense applications and cryptosystems often demand security features, including cryptography, tamper resistance, stealth, etc., by means of hardware approaches and/or software approaches to prevent data leakages. The side channel attacks (SCAs) have been employed to extract the secret keys of the encrypted algorithms implemented in hardware devices by analyzing their physical leakage parameters such as power dissipation, electromagnetic interference, timing and acoustic information.

Lecture #2: Randomized Modulation for Low-Harmonics Low-Noise Switched-Mode DC-DC Converters

The global market for low-power portable electronic devices is gargantuan and rapidly growing. For examples, the market for tablets and smartphones is estimated to reach more than 2.3 billion of devices by 2018, and for Internet-of-Things (IoTs) is estimated to reach more than 20 billion of devices by 2020. These devices are becoming more intelligent due to an increasing array of mixed-signal ICs, System-on-Chips, and sensors employed therein. This means more DC-DC converters
are needed to convert the battery voltage into different voltages for the various circuits and sensors. Due the limited PCB area and the small physical size constraints, it is imperative that these converters employ external passive components that are as small as possible.

Among the different converters, switched-mode DC-DC converters are widely used due to their high power-efficiencies. However, conventional switched-mode DC-DC converters based on the Pulse Width Modulation scheme (PWM) are inherently noisy, and generates strong harmonics at multiples of the switching-frequency in the input current and the output voltage spectra. The harmonics at the input current can cause conducted electromagnetic interference (EMI) noise that travels along power lines or PCB traces, and causes interference to other electronic circuits near the converter. Mitigating the harmonics can be done using larger passive filters, but this is undesirable due to the area and size constraints in portable devices.

In this seminar, we present a novel randomized modulation scheme that mitigates the switching-frequency harmonics without the need to use large passive filters. We subsequently present our proposed hybrid scheme that combines the randomized modulation with a noise-shaper to further attenuate the low-frequency noise in the frequency spectrum. We also present a novel pulse generator structure that translates the duty cycle input into

output pulses of the hybrid scheme, and show the computer simulations of a switched-mode DC-DC converter embodying the pulse generator.

Biography

Dr. Bah-Hwee Gwee received his B.Eng. degree from University of Aberdeen, UK, in 1990. He received his MEng and PhD degrees from Nanyang Technological University (NTU), Singapore in 1992 and 1998 respectively. He was an Assistant Professor and is currently an Associate Professor in NTU. He has worked on a number of research projects with research grant amounting to US$6.5M. He was the principal investigator of the research projects from The Agency for Science, Technology and Research (A*STAR) – PSF research project of US$597k, MoE Academic Research Tier-2 grant of US$860k), ASEAN-EU University Network Program grant of €200k and the Defense Science Organization grant of US$2.3M. He was also the Co-PI of NTU-Panasonic research collaboration amounting to US$800k and DARPA project of US$350k, Linkoping University – NTU joint research collaboration of US$400k, The Agency for Science, Technology and Research (A*STAR) – PSF research project of US$500k. He has published more than 100 technical papers, 6 patents (3 granted in USA) and co-founded a Start-up in 2005.

He was the Chairman of IEEE-Singapore CAS Chapter in 2005, 2006, 2013 and 2016. He is in the IEEE CAS TCs of VSA, DSP and Bio-medical CAS TC since 2004 and he is currently the TC Secretary for DSP TC. He was a member of the Steering Committee for the IEEE Asia Pacific Conference on Circuit and Systems (IEEE APCCAS) in 2005 - 2007. He was the organizing committee of the IEEE Bio-CAS 2004, IEEE APCCAS 2006, the TPC Chair of ISIC 2007, ISIC 2011 and ISIC 2016) and General Co-Chair for IEEE DSP 2018. He has also served as Associate Editors IEEE Transactions of Circuits and Systems I – Regular Papers (2012-2013), IEEE Transactions of Circuits and Systems II – Brief Express (2010-2011) and Journal of Circuits, Systems and Signal Processing (2007-2012). He was awarded Temasek Laboratories @ NTU Best Publication Award in 2012 and the Teaching Excellence Award in NTU in 2013. He is a senior member of IEEE. He was an IEEE DL in 2009/10 and 2017/18. He was awarded the Singapore Defense Technology Prize in 2016.

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Lecture #1: Structural Interpretations of Stability Tests of Linear Systems

A number of stability-test procedures for continuous-time and discrete-time linear systems have been advanced. Of these, the Routh-Hurwitz stability test for continuous-time systems and Schur-Cohn stability test for discrete-time systems are well-known, and can be found in all texts on linear systems. In this talk, we provide a unified structural interpretation of these two well-known stability tests. The basic idea behind the network interpretation is the fact that the stability of any linear system is equivalent to the stability of a related allpass system. The allpass system can be realized as a cascade of two-pair allpass (lossless) networks. The parent linear system is stable if and only if the allpass two-pair is stable.

Lecture #2: Structural Subband Decomposition: A New Concept in Digital Signal Processing

Polyphase decomposition of a sequence was advanced to develop computationally efficient interpolators and decimators, and has also been used to design computationally efficient quadrature-mirror filter banks. The polyphase decomposition represents a sequence into a set of sub-sequences, called polyphase components. However, the polyphase components do not exhibit any spectral separation. In this talk, we first review the concept of structural subband decomposition, a generalization of the polyphase decomposition, which decomposes a sequence into a set of sub-sequences with some spectral separation that can be exploited advantageously in many digital signal processing applications. We then outline some of the applications of the structural subband decomposition, such as, efficient design and implementation of FIR digital filters, development of computationally efficient decimators and interpolators, subband adaptive filtering, and fast computation of discrete transforms.

Biography

Sanjit K. Mitra is a Research Professor in the Department of Electrical & Computer Engineering, University of California, Santa Barbara and Professor Emeritus, Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles.

Dr. Mitra has served IEEE in various capacities including service as the President of the IEEE Circuits & Systems Society in 1986. He is a member of the U.S. National Academy of Engineering, a member of the Norwegian Academy of Technological Sciences, an Academician of the Academy of Finland, a foreign member of the Finnish Academy of Sciences and Arts, a foreign member of the Croatian Academy of Sciences and Arts, Croatian Academy of Engineering, and the Academy of Engineering, Mexico, and a Foreign Fellow of the National Academy of Sciences, India and the Indian National Academy of Engineering. Dr. Mitra is a Life Fellow of the IEEE.

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Lecture #1: Current Practices and Future Research Directions in Adaptive Signal Processing

While the theory and design of linear adaptive filters based on FIR filter structures is well developed and widely applied in practice, the same situation is not true for linear IIR or for nonlinear adaptive filters in general. The latter situation exists because both linear IIR structures and nonlinear structures sometimes produce multi-modal error surfaces on which stochastic gradient optimization strategies fail to reach the global minimum. This seminar begins with a concise review of state-of-the-art techniques in linear adaptive filtering, and then develops the need for nonlinear adaptive filters in applications such as nonlinear echo cancellation, nonlinear channel equalization, and acoustic channel identification. The three important evolutionary optimization algorithms will be introduced as potentially useful algorithms to deal with multimodal error surfaces. This seminar also explores how the principles of adaptive fault tolerance can be used effectively in adaptive VLSI processors that are prone to both hard and soft errors in highly integrated systems that are being scaled to smaller feature dimensions and reduced voltage thresholds.

Lecture #2: Arithmetic vs. Algorithmic Fault Tolerance for Highly Scaled VLSI Signal Processors

Adaptive fault tolerance (AFT) takes advantage of adaptive signal processing architectures that use adaptive principles to achieve automatic fault recovery. Recent work has demonstrated the capability of AFT methods to mask single and multiple stuck-at bit errors in the filter coefficients, as well as to demonstrate the capability of AFT filters to recover from transient errors. This seminar explores how the principles of adaptive fault tolerance can be used effectively in adaptive VLSI processors that are prone to both hard and soft errors in highly integrated systems that are being scaled to smaller feature dimensions and reduced voltage thresholds. This seminar also includes a discussion of arithmetic fault tolerance based on arithmetic coding, involving either hardware redundancy or multiple execution redundancy (MER) strategies designed to identify and overcome transient errors. Arithmetic techniques provide powerful low-redundancy fault tolerance properties that must be introduced at VLSI design levels, whereas MER strategies generally require higher degrees of redundancy that can be introduced at software programming levels.

Lecture #3: Design and Performance of Adaptive Systems Based on Bio-Inspired Optimization Strategies

While the theory and design of linear adaptive filters based on FIR filter structures is well developed and widely applied in practice, the same situation is not true for linear IIR or for nonlinear adaptive filters in general. The latter situation exists because both linear IIR structures and nonlinear structures sometimes produce multi-modal error surfaces on which stochastic gradient optimization strategies fail to reach the global minimum. This seminar begins with a concise review of state-of-the-art techniques in linear adaptive filtering, and then develops the need for nonlinear adaptive filters in applications such as nonlinear echo cancellation, nonlinear channel equalization, and acoustic channel identification. Several basic nonlinear adaptive structures will be discussed, including Volterra models, neural network models, and series cascade modular structures. Then three important evolutionary optimization algorithms will be introduced as potentially useful algorithms to deal with multimodal error surfaces. The three evolutionary algorithms to be considered are the simulated annealing, genetic, and particle swarm optimization (PSO) algorithms. Emphasis will be placed on the PSO techniques because they have not received much previous attention for adaptive filtering.

Lecture #4: The Wild Historical Tug-a-War: “DSP Theory versus IC Technology”

Many engineers believe that the publication in 1975 of Rabiner and Gold’s reference book “Theory and Application of Digital Signal Processing” and Oppenheim and Schafer’s text book “Digital Signal Processing” marked the beginning of modern digital signal processing as a formal academic discipline. The 20 years preceding the publication of these pioneering texts were marked with many key developments, including the digital filter, the fast Fourier Transform, the microprocessor, the digital calculator, the digital watch, etc. The first portion of this talk will describe how many of these early developments contributed to the development of the field of digital signal processing as a formal engineering discipline, and how DSP theory and IC technology “pulled and tugged” at each other and pushed the state of the art in both areas to great heights. The second part of this will focus on recent developments in area of adaptive signal processing. During the last fifty years, rapid advancements in adaptive signal processing theory and IC technologies have greatly advanced the state of the art in DSP associated with telephone communications, computer networking, digital video, wireless communications, and digital multimedia information systems.

Biography

W. Kenneth Jenkins joined Penn State University as Professor and Head of Electrical Engineering in 1999. After receiving his Ph.D. from Purdue University, Jenkins was a research scientist associate in the Communication Sciences Laboratory at the Lockheed Research Laboratory, Palo Alto, CA. In 1977 he joined the University of Illinois at Urbana-Champaign where he was a faculty member in Electrical and Computer Engineering from until 1999. Jenkins' current research interests include fault tolerant DSP for highly scaled VLSI systems, adaptive signal processing, multidimensional array processing, computer imaging, and bio-inspired optimization algorithms for intelligent signal processing. He received the IEEE CAS Society, Distinguished Service Award, the 2000 IEEE Millennium Award, the 2000 IEEE CAS Society Golden Jubilee Medal, and the 2000 George Montfiore Foundation, International Award. He is a Life Fellow of IEEE.

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Lecture #1: Multi-Step Incremental Analog-to-Digital Converters for Ultra-Low-Power Applications

Integrated sensor interface circuits require power-efficient high-accuracy data converters. Incremental A/D converters (IADCs) are often the best choice for these, since they can provide excellent energy efficiency, and are easily multiplexed, need only simple digital filtering, and allow low latency. By performing the conversion in multiple steps, the hardware can also be multiplexed among all steps. This lecture will give an overview of IADCs, with its focus on multi-step converters. Such converters may realize 16-bit operation with a single opamp and comparator.

Lecture #2: Pseudo-pseudo Differential Circuits

Pseudo-differential circuits approximate the performance of fully-differential structures, while allowing single-ended operation of the two half stages in the circuit. This requires duplication of the circuitry, with accurate symmetry needed between the two halves to cancel common-mode noise. This letter proposes a single-ended scheme which uses double sampling and time interleaving to achieve a performance comparable to that of differential circuits. It requires only half the complexity and reduced power dissipation compared to the fully- or pseudo-differential circuits.

Biography

Gabor C. Temes (SM'66–F'73–LF'98) received the undergraduate degrees from the Technical University of Budapest and Eötvös University, Budapest, Hungary, in 1952 and 1955, respectively. He received the Ph.D. degree in electrical engineering from the University of Ottawa, ON, Canada, in 1961, and an honorary doctorate from the Technical University of Budapest, Budapest, Hungary, in 1991.
He held academic positions at the Technical University of Budapest, Stanford University, Stanford, CA, and the University of California at Los Angeles (UCLA). He worked in industry at Northern Electric R&D Laboratories (now Bell-Northern Research), Ottawa, Canada, as well as at Ampex Corp. He is now a Professor in the School of Electrical Engineering and

Computer Science at Oregon State University. His recent research has dealt with CMOS analog integrated circuits and data converters. He coedited and coauthored many books; the most recent one is Understanding Delta-Sigma Data Converters (IEEE Press/Wiley, 2005). He also wrote approximately 600 papers in engineering journals and conference proceedings. Dr. Temes was Editor of the IEEE TRANSACTIONS ON CIRCUIT THEORY and Vice President of the IEEE Circuits and Systems (CAS) Society. In 1968 and in 1981, he was co-winner of the IEEE CAS Darlington Award, and in 1984 winner of the Centennial Medal of the IEEE. He received the Andrew Chi Prize Award of the IEEE Instrumentation and Measurement Society in 1985, the Education Award of the IEEE CAS Society in 1987, and the Technical Achievement Award of the IEEE CAS Society in 1989. He received the IEEE Graduate Teaching Award in 1998, and the IEEE Millennium Medal as well as the IEEE CAS Golden Jubilee Medal in 2000. He was the 2006 recipient of the IEEE Gustav Robert Kirchhoff Award, and the 2009 IEEE CAS Mac Valkenburg Award. He is member of the National Academy of Engineering.

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Lecture #1: Adapted Compressed Sensing for IoT Applications

Compressed Sensing (CS) is a technique for the acquisition of signals using a number of measurements that is potentially much smaller than the number of samples at the Nyquist rate. It can be seen as an extremely simple encoding stage allowing a low-cost compression that perfectly fits applications in which data storage and/or transmission costs are an issue while there are also stringent limits on local computation capabilities, a recurrent scenario in IoT applications.

The optimization of such systems forces a definite departure from classical “universal” CS. Rather, spectral-like information on the signal to acquire can be exploited in a well-defined design flow that maximizes compression performance while keeping the computational complexity at very low level.

The talk describes the basics of CS and introduces the ideas behind such a design flow. It then shows how to apply the method to the acquisition of few real-world signals mapping both compression and complexity reduction performances into the energy required by the task of locally acquiring a physical quantity that must be transmitted to a non-local hub.

A pointer to some fully developed software allowing experiments and design of these adapted CS solutions will be given.

Lecture #2: Zero-Cost Security for Embedded Systems by Compressed Sensing

Compressed Sensing (CS) is a technique for the acquisition of signals using a number of measurements that is potentially much smaller than the number of samples at the Nyquist rate. It can be seen as an extremely simple encoding stage allowing a low cost compression. Yet, its intrinsic structure allows its re-use as a physical level public-key encryption layer thus preventing the need of a dedicated stage whenever the level of attained security is deemed sufficient.

This often applies to non-critical embedded applications with tight resource budgets that may thus benefit from a single stage that simultaneously performs data compression and encryption.

The talk describes the basics of CS and introduces the ideas behind its reuse as a low-cost encryption. Evaluations on the power and hardware saving due to a joint lossy compression and encryption are developed with emphasis on the fact that more of one public kay can be distributed allowing the reconstruction of the signals with different level of quality.

To match the resulting resource saving with the level of security provided, a rigorous cryptanalysis is carried out. Statistical ciphertext-only attacks are analyzed as well as known-plaintext attacks to prove that, though not perfectly secure in the Shannon sense, the method still provides a quite strong computational security.

Biography

Riccardo Rovatti (M'99–SM'02–F'12) born in 1969, received the Ph.D. degree in electronics, computer science, and telecommunications from the University of Bologna, Italy, in 1996. He is now a Professor of Electronics at the University of Bologna. His research focuses on mathematical and applicative aspects of statistical signal processing and on the application of statistics to nonlinear dynamical systems. He received the 2004 IEEE CAS Society Darlington Award and the 2013 IEEE CAS Society Guillemin-Cauer Award. He has been elected Fellow in 2012 for contributions to nonlinear and statistical signal processing applied to electronic systems. He is the co-author of more than 300 peer-reviewed international publications.

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Lecture #1: Machine-learning Enhanced Biomedical Data Analytics for Point-of-care Diagnosis System

With the recent advance of microfluidic-based lab-on-a-chip integration, lensless microfluidic imaging system with super-resolution (SR) algorithm has become a promising solution to miniaturize the conventional bulky optical-lens-based flow cytometer for portable and high-throughput cell detection. The previous lensless microfluidic imaging system however requires a multi-frame-SR based image processing with limited throughput to be realized on hardware. This talk presents two single-frame super-resolution algorithms using online machine-learning for lensless microfluidic imaging. One is based on extreme-learning machine and the other one is based convolution-neuron-network. Both requires only one frame of image to correct the resolution of the lensless images and can be realized with compact hardware (ASIC chip and FPGA) to perform a real-time image processing. A corresponding contact-imaging based microfluidic cytometer prototype is demonstrated for cell recognition and counting. Compared with the commercial flow cytometer, less than 8% error is observed for absolute number of microbeads; and 0.10 coefficient of variation is observed for cell-ratio of mixed RBC and HepG2 cells in solution.

Lecture #2: CMOS Integrated Lab-on-a-chip System for Personalized DNA Sequencing

Considering the current aging society, the future personalized diagnosis requires portable biomedical devices with miniaturization of bio-instruments. The recent development of lab-on-a-chip (LoC) technology has provided a promising integration platform of CMOS integrated sensor, microfluidic channel, and MEMS. This talk will report the recent progress in CMOS integrated LoC system for personalized DNA sequencing at academia and also industry, including the recent works at NTU CMOS Emerging Technology Group (http://www.ntucmosetgp.net/). Traditional CMOS ion-sensitive-field-effect-transistor (ISFET) has poor pH detection sensitivity as well as faulty pH values. The first selected work (highlighted by IEEE VLSI-SYMP'14 and IEEE TBME'15) is about a dual-mode (chemical + optical) CMOS ISFET sensor, which can improve sequencing accuracy significantly by correlated readout of chemical pH value at location-determined microbead via optical contact imaging. The second selected work (IEEE CICC'15, VLSI-SYMP'16) will further discuss a high-sensitivity sub-threshold readout of pH value by current-to-time-to-voltage conversion (C-TVC), which can reach <1mV or 1pA resolution with fast detection time. By utilizing C-TVC readout scheme, it is possible to identify single nucleotide bases required in the 4th generation DNA sequencing system (Nanopore) with CMOS-compatible solid-state pore (Si3N4/SiO2 membrane).

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   - 1.1. Scalability of DNA Sequencing
   - 1.2. CMOS Multi-modal Sensor Platform for DNA
     - 1.2.1. CMOS Image Sensor (Illumina, PacBio)
     - 1.2.2. CMOS Impedance Sensor (ONT, Genia)
     - 1.2.3. CMOS pH Sensor (IonTorrent)
2. CMOS pH Sensor
   - 2.1. Fundamental of ISFET Sensor
   - 2.2. Pixel Level Limitation
   - 2.3. High-sensitivity ISFET Sensor Design
   - 2.4. Pixel-to-Pixel Level Limitation
   - 2.5. Dual-mode ISFET Sensor Design
   - 2.6. Chip and Measurement
3. CMOS Nano Sensor
   - 3.1. Nanoelectronics for DNA
   - 3.2. CMOS Readout for Nanopore
   - 3.3. CMOS Readout for Nanogap
   - 3.4. Chip and Measurement
4. CMOS Machine Learning On-chip for DNA Data Analytics
5. Conclusions

Biography

Dr. Yu obtained his B.S. degree from Fudan University (Shanghai China) in 1999, with 4-year first-prize Guanghua scholarship and 1-year Samsung scholarship for the outstanding student in science and engineering. After selected by mini-cuspea program, he spent some time in New York University, and obtained M.S/Ph. D degrees both from electrical engineering department at UCLA in 2007, with major of integrated circuit and embedded computing. He was a senior research staff at Berkeley Design Automation (BDA) since 2006, one of top-100 start-ups selected by Red-herrings at Silicon Valley. Since October 2009, he is an assistant professor at school of electrical and electronic engineering, and as area director of VIRTUS IC Design, VALENS Biomedical Research Center, as well as IoT Cluster Director of Energy Research Institute, Nanyang Technological University (NTU), Singapore.