David J. Allstot

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Lecture 1: Switched-Capacitor Circuits: From Maxwell to the Internet of Things

Maxwell introduced the concept of the equivalent switched-capacitor resistance in Vol. 2 of his Treatise on Electricity and Magnetism in 1873. The concept laid dormant for almost a century until it became commercially viable by exploiting the switches, native capacitors, and operational amplifiers of MOS IC technology. CMOS switched-capacitor circuits have been used in high-volume data converters and signal processing ICs for nearly four decades, and are ubiquitous in modern RF transceiver circuits and emerging as a dominant design approach in CMOS bio-medical and internet of things circuits and systems, etc.

This talk will begin with a brief history of SC circuits as applied to data converters, precision high-order filters, operational amplifiers, etc.

Next, SC circuits are described for body-area-networks (BAN) that integrate multiple sensor nodes in the portable and wearable bio-medical systems that are revolutionizing healthcare. A typical BAN comprises several bio-signal and motion sensors and uses ultra-low-power short-haul radios in conjunction with nearby smart-phones or handheld devices (with GPS capabilities) to communicate via the internet with a doctor or other healthcare professional. Higher energy efficiency is critical to the development of feature-rich, wearable and reliable personal health monitoring systems.

The amount of data transmitted to the smart-phone increases as more sensors are added to the BAN. Because the energy consumed for RF transmission is proportional to the data rate, it is advantageous to compress the bio-signal at the sensor prior to digitization and transmission. This energy-efficient paradigm is possible using compressed sensing—a sampling theory wherein a compressible signal can be acquired using only a few incoherent measurements. For ECG signals, for example, large compression factors are achievable which means similar reductions in energy consumption.

SC circuits are having a huge impact on wireless communications. A major challenge is the RF power amplifier dissipates a large fraction of the total power of a transceiver because of its low efficiency. Despite more than two decades of extensive research, the challenge of on-chip RF Pas with high efficiency in digital-friendly CMOS technologies has not been met. Switching PA topologies with relatively high efficiency have gained momentum, and relatively high output power is being delivered using power combining techniques. Supply regulation techniques have enabled higher efficiency when amplifying non-constant envelope modulated signals. The switched-capacitor RF power amplifier technique which meets many of the remaining challenges is described and some future directions are presented.

Biography

David J. Allstot received the B.S., M.S., and Ph.D. degrees from the Univ. of Portland, Oregon State Univ., and the Univ. of California, Berkeley.

He has held several industrial and academic positions including the Boeing-Egtvedt Chair Professor of Engineering at the Univ. of Washington from 1999 to 2012 and Chair of the Dept. of EE from 2004 to 2007. In 2012 he was a Visiting Professor of EE at Stanford and from 2013 to 2016, he held a three-year appointment

as the MacKay Professor in Residence in the EECS Dept. at UC Berkeley. Since June 2017, he has been a Professor in the School of EECS at Oregon State University.

Dr. Allstot has advised about 65 M.S. and 40 Ph.D. graduates, published more than 300 papers, and received several awards for outstanding teaching and research including the 1980 IEEE W.R.G. Baker Award, 1995 and 2010 IEEE Circuits and Systems Society (CASS) Darlington Award, 1998 IEEE Intl. Solid-State Circuits Conf. Beatrice Winner Award, 2004 IEEE CASS Desoer Technical Achievement Award, 2005 Semiconductor Research Corp. Aristotle Award, 2008 Semiconductor Industries Assoc. University Research Award, 2011 IEEE CASS Van Valkenburg Award, and 2015 IEEE Trans. on Biomedical Circuits and Systems Best Paper Award. He has been active in the IEEE Circuits and Systems and Solid-State Circuits Societies throughout his career.

Alyssa Apsel

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Tutorial 1: Making Sense of Low Power and Ultra Low Power Radio

Although not everyone is a wireless designer, everyone seems to want to include a wireless interface on their chip or system. With the advent and exploding interest in IoT, the emphasis on making all data communication wireless has only increased. Some of these communication interfaces are interesting from a research point of view, and some are not. When overall power consumption and efficiency are of paramount interest, however, simply adding a wireless interface onto an otherwise low power sensing or computing chip may not be straightforward. In fact, the wireless interface is likely to consume the bulk of the power of these systems and overwhelm the power budget. With the range of technologies calling themselves low power wireless interfaces, it is no surprise that uninitiated system designers often choose the wrong one. The purpose of this tutorial is to demystify some of these choices and make it easier for designers whose focus is not on the RF interface to pick the correct technology for their applications and get started with simple designs. I will introduce the basic transceiver architectures for popular wireless candidates including: wake-up radios, low power UWB radios, NFC, backscatter radios, Bluetooth, and Zigbee. I will also discuss the advantages and disadvantages as well as potential applications for each. I will compare and contrast these radios with the end goal of enabling designers to make educated and intelligent decisions about which RF transceivers make sense for their applications in sensors, body area networks, IoT, implantables, or whatever they may be. Finally, attendees will walk through case studies and simple design problems and select suitable wireless interfaces for different applications.

Lecture 1: Flexible Radios and Flexible Networks

Over the past decades the world has become increasingly connected, with communications driving both markets and social movements. Low power electronics, efficient communications, and better battery technology have all contributed to this revolution, but the cost and power required for these systems must be pushed further to make cheap, ubiquitous, seamless communication accessible to a wider community. In this talk I will discuss two engineering approaches to this problem. I will look at various approaches to drive the power down in radio networks that span across circuits and systems. I will also look at creative biologically inspired approaches to enabling very low power networks and IoT. Finally, I will discuss how by adding flexibility and building reconfigurable hardware, we can likewise build lower power and less costly consumer systems that can adapt across protocols and networks and work under changing device technologies.

Biography

Alyssa Apsel received the B.S. from Swarthmore College in 1995 and the Ph.D. from Johns Hopkins University, Baltimore, MD, in 2002. She joined Cornell University in 2002, where she is currently a Professor of Electrical and Computer Engineering. She is also holds an appointment as Visiting Professor at Imperial College, London. The focus of her research is on power-aware mixed signal circuits and design for highly scaled CMOS and modern electronic systems. Her current research is on the leading edge of ultra-low power

and flexible RF interfaces for IoT. She is a member of the IEEE SSCS working group on IoT and has authored or coauthored over 100 refereed publications including one book in related fields of RF mixed signal circuit design, ultra-low power radio, interconnect design and planning, photonic integration, and process invariant circuit design techniques resulting in ten patents. She received best paper awards at ASYNC 2006 and IEEE SiRF 2012, had a MICRO “Top Picks” paper in 2006, received a college teaching award in 2007, received the National Science Foundation CAREER Award in 2004, and was selected by Technology Review Magazine as one of the Top Young Innovators in 2004. She has also served on the Board of Governors of IEEE CAS (2014-2016) and as an Associate Editor of various journals including IEEE Transactions on Circuits and Systems I and II, and Transactions on VLSI. She has also served as the chair of the Analog and Signal Processing Technical committee of ISCAS 2011, is on the Senior Editorial Board of JETCAS, as Deputy Editor in Chief of Circuits and Systems Magazine, and as the co-founder and Chair of ISCAS Late Breaking News.

In 2016, Dr. Apsel co-founded AlphaWave IP Corporation, a multi-national Silicon IP provider focused on multi-standard analog Silicon IP solutions for the world of IOT. As Chief Technology Officer of AlphaWave, Dr. Apsel leads the company’s global research capability with offices in Silicon Valley, Toronto, and London. Dr. Apsel also drives AlphaWave’s intellectual property strategy and manages the company’s global patent portfolio.

Chip Hong Chang

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Nanyang Technological University

Lecture 1: Hardware Intrinsic Security: Challenges, Solutions and Opportunities

The illusion that hardware is more dependable and trustable than the software running on it with deterring reverse engineering cost of highly miniaturized dense monolithic integrated circuit has once and again been invalidated. Remotely activated hardware Trojan and untraceable break-ins of networking systems running on fake and subverted chips have frequently been reported by businesses and military strategists, and confirmed by forensic security experts analysing these incidents. The situation was aggravated by the geographical dispersion of chip design activities and the heavy reliance on third-party hardware intellectual properties. Counterfeit chips (such as unauthorized copies, remarked/recycled dice, overproduced and subverted chips or cloned designs) pose a major threat to all stakeholders in the integrated circuit supply chain, from designers, manufacturers, system integrators to end users, in view of the severe consequence of potentially degraded quality, reliability and performance that they caused to the electronic equipment and critical infrastructure. This seminar addresses recent development in preventive countermeasures, post-manufacturing diagnosis techniques and emerging security-enhanced hardware primitives to avert these hardware security threats in the new age of Internet of Things (IoT) and emergent systems, where the intense interactions between devices and devices, and devices and humans have introduced new vulnerabilities of embedded devices.

Tutorial 1: Physical Unclonable Functions – Past, Present and Future

Physical Unclonable Function (PUF) has emerged as an inexpensive security primitive to overcome the device identification and authentication problems by its radically different way of interrogating hardware without the permanent presence of a secret key. The security of PUF rests in the intrinsic complexity and irreproducibility of a random physical disorder system instead of a hard-to-solve mathematical problem. Device signature generated by PUF cannot be physically replicated even by the original manufacturer due to the uncontrollable nature of manufacturing process variations. As the secret information can only be generated when the PUF is powered on, active manipulation of circuit structure will cause dysfunction of its challenge-response mechanism and become tamper evident. As unique and unclonable chip identifiers, PUFs find its niche in active hardware metering, which enables chip designers to lock and unlock the circuit functionality to gain post-fabrication control of their intellectual property and clone detection. Besides, rich variety of post-CMOS technologies, such as Phase Change Memory and Spin Transfer Torque Magnetic Random Access Memory, offer new challenges and opportunities to PUF system design. Last but not least, sensors are integral parts of an IoT ecosystem for life-changing applications. Integration of PUF credentials into sensor circuitry or sensing data without compromising the original sensing operations holds strong promises in addressing forensic and security problems in IoT.

Biography

Chip Hong Chang received the B.Eng. (Hons.) degree from the National University of Singapore, in 1989, and the M. Eng. and Ph.D. degrees from Nanyang Technological University (NTU), Singapore, in 1993 and 1998, respectively. He served as a Technical Consultant in industry prior to joining the School of Electrical and

Electronic Engineering (EEE), NTU, in 1999, where he is currently an Associate Professor. He holds joint appointments with the university as Assistant Chair of Alumni of the School of EEE from June 2008 to May 2014, Deputy Director of the 100-strong Center for High Performance Embedded Systems from 2000 to 2011, and Program Director of the Center for Integrated Circuits and Systems from 2003 to 2009. He has coedited four books, published ten book chapters, around 100 international journal papers (two-thirds are IEEE) and more than 160 refereed international conference papers. His research interests include hardware security, residue and unconventional number systems, low-power arithmetic circuits, digital filter design and digital image processing. He has delivered several keynotes and more than 30 invited colloquia, including tutorials at the 2017 Asia and South Pacific Design Automation Conference (ASP-DAC 2017) and 2017 IEEE International Symposium on Circuits and Systems (ISCAS 2017). He is the recipient of the 2006 NTU Research Outstanding and Award Recognition Scheme, 2007 British High Commission Collaboration Development Award for Microelectronics and Embedded Systems and Canada Microsystems Strategic Alliance of Quebec Collaboration Development Award, co-recipient of the PrimeAsia-2010 Gold Leaf and Silver Leaf Certificates, and coauthor of the finalist of AsianHOST 2017 Cisco best paper award, ISCAS 2015 best student paper award competition and VLSI 95 best paper award.

Dr. Chang has served as Associate Editor for the IEEE Transactions on Circuits and Systems-I from 2010–2012, IEEE Transactions on Very Large Scale Integration (VLSI) Systems since January 2011, IEEE Access since March 2013, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems since January 2016, IEEE Transactions on Information Forensic and Security since January 2016, Springer Journal of Hardware and System Security since June 2016, Microelectronics Journal since May 2014, Integration, the VLSI Journal from 2013–2015, Editorial Advisory Board Member of the Open Electrical and Electronic Engineering Journal from 2007–2013, and the Editorial Board Member of the Journal of Electrical and Computer Engineering from 2008–2014. He also guest edited several journal special issues including IEEE Transactions on Circuits and Systems-I and IEEE Transactions on Dependable and Secure Computing, and served in the organizing and technical program committees of more than 50 international conferences (mostly IEEE). He is a Fellow of the IEEE and the IET.

Yo-Sung Ho

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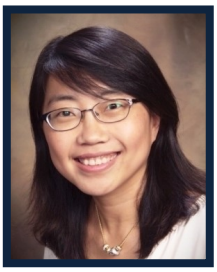
Lecture 1: 3D Video Processing for Immersive AR/VR Contents Generation

With the emerging market of AR/VR imaging products, 3D video has become an active area of research and development in recent years. 3D video is the key to provide more realistic and immersive perceptual experiences than the existing 2D counterpart. There are many applications of 3D video, such as 3D movie and 3DTV, which are considered the main drive of the next-generation technical revolution. Stereoscopic display is the current mainstream technology for 3DTV, while auto-stereoscopic display is a more promising solution that requires more research endeavors to resolve the associated technical difficulties. In this lecture, we are going to cover the current state-of-the-art technologies of 3D video capturing and processing for AR/VR applications. After defining the basic requirements for 3D realistic multimedia services, we cover various multi-modal immersive media processing techniques for immersive 360 degree video applications.

Biography

Dr. Yo-Sung Ho, a new IEEE Fellow, received his B.S. and M.S. degrees in electronic engineering from Seoul National University, Seoul, Korea, in 1981 and 1983, respectively, and the Ph.D. degree in electrical and computer engineering from the University of California, Santa Barbara, in 1990. He joined ETRI (Electronics and Telecommunications Research Institute), Daejeon, Korea, in 1983. From 1990 to 1993, he was with North America Philips Laboratories, Briarcliff Manor, New York, where he was involved in development of the Advanced Digital High-Definition Television (AD-HDTV) system. In 1993, he rejoined the technical staff of ETRI and was involved in development of the Korean DBS Digital Television and High-Definition Television systems. Since 1995, he has been with Gwangju Institute of Science and Technology (GIST), where he is currently Professor of School of Electrical Engineering and Computer Science. Since August 2003, he has been Director of Realistic Broadcasting Research Center at GIST in Korea. He has served as Associate Editors of IEEE Transactions on Multimedia (T-MM) and IEEE Transactions on Circuits and Systems Video Technology (T-CSVT). His research interests include Digital Image and Video Coding, Image Analysis and Image Restoration, Three-dimensional Image Modeling and Representation, Advanced Source Coding Techniques, Augmented Reality (AR) and Virtual Reality (VR), Three-dimensional Television (3DTV) and Realistic Broadcasting Technologies.



Hai "Helen" Li

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Duke University

Lecture 1: Brain Inspired Computing: The Extraordinary Voyages in Known and Unknown Worlds

Human brain is the most sophisticated organ that nature ever builds. Building a machine that can function like a human brain, indubitably, is the ultimate dream of a computer architect. Although we have not yet fully understood the working mechanism of human brains, the part that we have learned in past seventy years already guided us to many remarkable successes in computing applications, e.g., artificial neural network and machine learning. The recently emerged research on "neuromorphic computing", which stands for hardware acceleration of brain-inspired computing, has become one of the most active areas in computer engineering. The talk will start with a background introduction of neuromorphic computing, followed by examples of hardware acceleration schemes of learning and neural network algorithms and memristor-based computing engine. I will also share our prospects on the future technology challenges and advances of neuromorphic computing.

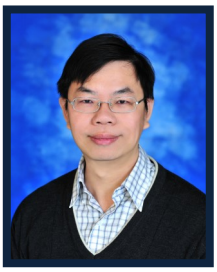
Lecture 2: Deep Learning and Neuromorphic Computing - Technology, Hardware and Implementation

As big data processing becomes pervasive and ubiquitous in our lives, the desire for embedded-everywhere and human-centric information systems calls for an intelligent computing paradigm that is capable of handling large volume of data through massively parallel operations under limited hardware and power resources. This demand, however, is unlikely to be satisfied through the traditional computer systems whose performance is greatly hindered by the increasing performance gap between CPU and memory as well as the fast-growing power consumption. Inspired by the working mechanism of human brains, a neuromorphic system naturally possesses a massively parallel architecture with closely coupled memory, offering a great opportunity to break the "memory wall" in von Neumann architecture. The tutorial will start with the evolution of neural networks, followed by the acceleration on conventional platform. I will then introduce the neuromorphic system designs including the approaches based on CMOS and emerging nanotechnologies. The latest research outcomes on hardware implementation optimization, the reliability and robustness control schemes, and new training methodologies by taking the hardware constraints into the consideration will then be presented. At last, new applications and challenges raised in deep learning and neuromorphic computing will be discussed.

Biography

Hai "Helen" Li received the B.S. and M.S. degrees from Tsinghua University, Beijing, China, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA, in 2004. She is currently Clare Boothe Luce Associate Professor with the Department of Electrical and Computer Engineering at Duke University, Durham, NC, USA. She was with Qualcomm Inc., San Diego, CA, USA, Intel Corporation, Santa Clara, CA, Seagate Technology, Bloomington, MN, USA, the Polytechnic Institute of New York University, Brooklyn, NY, USA, and the University of Pittsburgh, Pittsburgh, PA, USA. She has authored or co-authored over 200 technical papers published in peer-reviewed journals and conferences and holds 70+ granted U.S. patents. She authored a book entitled Nonvolatile Memory Design:

Magnetic, Resistive, and Phase Changing (CRC Press, 2011). Her current research interests include memory design and architecture, neuromorphic architecture for brain-inspired computing systems, and architecture/circuit/device cross-layer optimization for low power and high performance. Dr. Li serves as an Associate Editor of TVLSI, TCAD, TODAES, TMSCS, TECS, CEM, and the IET Cyber-Physical Systems: Theory & Applications. She has served as organization committee and technical program committee members for over 30 international conference series. She received the NSF CAREER Award (2012), the DARPA YFA Award (2013), TUM-IAS Hans Fisher Fellowship (2017), seven best paper awards and another seven best paper nominations. Dr. Li is a senior member of IEEE and a distinguished member of ACM.



Chia-Wen Lin

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Lecture 1: Bridging CNNs and Unsupervised Image Clustering: A Hybrid Data-Driven and Model-Based Approach (1 hour)

Given a large unlabeled set of images, how to efficiently and effectively group images into clusters based on extracted visual representations remains a challenging problem. Although convolutional neural networks (CNNs) have proven to be effective in visual representation learning, it is difficult to learn a good CNN model from unlabeled images in a data-driven manner, even with an initial model pre-trained from a large-scale image dataset such as ImageNet. To address this problem, we propose a hybrid data-driven and model-based approach to solve joint clustering and representation learning with a CNN in an iterative manner. In our method, given an input image set, we first find initial cluster centroids using a randomly initialized (or pre-trained) CNN model. To reduce complexity, mini-batch clustering is performed to assign cluster labels to individual input samples for a mini-batch of images randomly sampled from the input image set until all images have been processed. Subsequently, image samples with reliable labels are extracted from noisy cluster labels based on Laplacian graph smoothness priors to update the CNN model, and the updated model is then used to re-cluster images. The representation learning and clustering are iterated until the clustering accuracy reaches to a convergence point. Experimental results demonstrate the proposed method outperforms start-of-the-art clustering schemes in terms of accuracy and storage complexity on large-scale image sets containing millions of images.

Lecture 2: Stereo Video Retargeting: Bringing the Theater Experience into Our Home (1 hour)

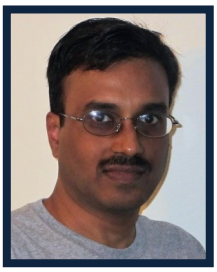
The popularity of stereo images/videos and various VR/AR display devices poses the need of resizing stereo image/video pairs. Nevertheless, traditional resizing methods like uniform scaling and cropping usually lead to annoying shape and depth distortions such as depth change and window violation. Although content-award retargeting schemers can address such problems, existing content-aware methods often incur conflicts among the requirements on shape, depth, and temporal coherency preservation, thereby failing to meet one or more of these requirements. This can significantly degrade the quality of experience when watching at 3D movie at home. In this seminar, we will introduce our recent results on how to simultaneously avoid shape and depth distortions as well as maintain the temporal coherency of shape and depth while resizing a stereo image/video to a desired size. Different from the existing methods, our method effectively avoids the conflicts among depth, shape and temporal-coherency requirements by relaxing the resizing constraints on those regions in a 3D scene that cannot be perceived by human eyes to maintain the temporal coherency of the remaining regions. Based on this new finding, our method employs depth information to derive effective temporal-coherency constraints so as to offer visually pleasing results and achieves significantly better retargeting performance than existing methods, making it possible to bring the theater experience into our home.

Tutorial 1: Visual Content Retargeting: Algorithms, Applications, and Quality Assessment (3 hours)

Video retargeting from a full-resolution video to a reduced-resolution display will inevitably cause information loss. Content-aware retargeting has proven to be an efficient means to avoid critical visual information loss while resizing an image/video. Nevertheless, retargeting a 2D/3D video can often lead to visually annoying distortions in object shape, scene depth, and temporal coherency. Preserving the shape and depth information as well as maintaining the spatio-temporal coherency of a retargeted video is very critical on visual quality. In this tutorial, we will first introduce the technical challenges and recent advances in content-aware retargeting. Then we will show how to use a panoramic mosaic to guide the scaling of corresponding regions of video frames in a video shot to ensure good spatio-temporal coherency. We will also introduce our recent results on simultaneously preserving scene depths, object shapes, and temporal coherency in stereoscopic video retargeting based on constraints relaxation. Then, we will present objective quality metrics based on geometric distortion and information loss for automatically evaluating the visual quality of a retargeted image and how to incorporate the metrics in video retargeting to improve visual quality. Finally, we will show how to construct a scalable video coder which supports content-adaptive spatial scalability (e.g., the base-layer and enhancement-layer videos are of different resolution and different aspect ratios) with good coding efficiency.

Biography

Prof. Chia-Wen Lin received his PhD degree in Electrical Engineering from National Tsing Hua University (NTHU), Hsinchu, Taiwan in 2000. He is currently a Professor with the Department of Electrical Engineering, National Tsing Hua University, Taiwan. He is also Director of the Multimedia Technology Research Center, College of Electrical Engineering and Computer Science, NTHU. His research interests include image/video processing and video networking. Dr. Lin is an IEEE Fellow. He has served as Associate Editor of IEEE Transactions on Image Processing, IEEE Transactions on Multimedia, IEEE Transactions on Circuits and Systems for Video Technology, IEEE Multimedia, and Journal of Visual Communication and Image Representation. He also served as a Steering Committee member of the IEEE Transactions on Multimedia during 2013-2015. He was Chair of the Multimedia Systems and Applications Technical Committee of the IEEE Circuits and Systems Society. He served as Technical Program Co-Chair of the IEEE ICME in 2010 and will be the TPC Chair of IEEE ICIP 2019 in Taipei. His papers won the Best Paper Award of IEEE VCIP 2015, and the Young Investigator Award of SPIE VCIP 2005.



Shanthi Pavan

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Lecture 1: Dissecting Design Choices in Continuous-time Delta-Sigma Converters

Continuous-time Delta-Sigma Modulators are a compelling choice for the design of high resolution analog-to-digital converters. Many delta-sigma architectures have been published (and continue to be invented). This leaves the designer with a bewildering array of choices, many of which seem to pull in opposite directions. Further, it is often difficult to make a clear comparison of various architectures, as they have been designed for dissimilar specifications, by different design groups, and in different technology nodes. This paper examines various design alternatives for the design of power efficient continuous-time delta sigma converters, and helps the designer navigate this maze.

Tutorial 1: Linear Periodically Time Varying Circuits and Systems Demystified

An analog/mixed-signal designer encounters time varying circuits everywhere - sample-and- holds, chopper stabilised amplifiers, mixers, switched-capacitor amplifiers and filters, discrete and continuous-time delta sigma modulators, N-path filters. The analysis of signals and noise in these circuits is often associated with messy mathematics and algebra. This talk aims to demystify linear (periodically) time varying circuits. Starting from first principles, intuition behind various aspects of time-varying circuits and systems will be given. This intuition is illustrated with case studies of practical circuits and systems, like chopper-stabilised amplifiers and continuous-time delta-sigma modulators. We also discuss the important class of LPTV networks with sampled outputs, and the use of reciprocity in the analysis of such systems. As an application of the principles learned in this seminar, we will analyze the N-path filter, and show how the analysis of signals and noise can be greatly simplified.

Tutorial table of contents :

- Time-invariant and time-varying systems basics
- LPTV systems and the Zadeh expansion
- N-Path systems part : Time and frequency-domain intuition.
- Sampled-LPTV systems and equivalence with a time-invariant sampled LTI system
- Reciprocity and inter-reciprocity in time invariant and time varying networks
- Application of interreciprocity to a cont. time delta sigma modulator
- Analysis of chopped amplifiers as LPTV systems, noise folding.
- N-path filter analysis based on sampled LPTV approach
- Noise in N-path filter

Biography

Shanthi Pavan obtained the B.Tech degree in Electronics and Communication Engg from the Indian Institute of Technology, Madras in 1995 and the M.S and Sc.D degrees from Columbia University, New York in 1997 and 1999 respectively. From 1997 to 2000, he was with Texas Instruments in Warren, New Jersey, where he worked on high speed analog filters and data converters. From 2000 to June 2002, he worked on microwave

ICs for data communication at Bigbear Networks in Sunnyvale, California. Since July 2002, he has been with the Indian Institute of Technology-Madras, where he is now a Professor of Electrical Engineering. His research interests are in the areas of high speed analog circuit design and signal processing.

Dr. Pavan is the recipient of many awards, including the IEEE Circuits and Systems Society Darlington Best Paper Award (2009), the Shanti Swarup Bhatnagar Award (2012) and the Swarnajayanthi Fellowship (2009) (from the Government of India). He is the author of *Understanding Delta-Sigma Data Converters* (second edition, with Richard Schreier and Gabor Temes). Dr. Pavan has served as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems: Part I - Regular Papers, and on the editorial boards of both parts of the IEEE Transactions on Circuits and Systems. He has served on the technical program committee of the International Solid State Circuits Conference, and been a Distinguished Lecturer of the Solid-State Circuits Society. He is a fellow of the IEEE, and the Indian National Academy of Engineering (INAE), and is a Distinguished Lecturer of the IEEE Circuits and Systems Society.

Gabriel A. Rincón-Mora

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Lecture 1: Energizing and Powering Microsystems

Networked wireless microsensors can not only monitor and manage power consumption in small- and large-scale applications for space, military, medical, agricultural, and consumer markets but also add cost-, energy-, and life-saving intelligence to large infrastructures and tiny devices in remote and difficult-to-reach places. Ultra-small systems, however, cannot store sufficient energy to sustain monitoring, interface, processing, and telemetry functions for long. And replacing or recharging the batteries of hundreds of networked nodes can be labor intensive, expensive, and oftentimes impossible. This is why alternate sources are the subject of ardent research today. Except power densities are low, and in many cases, intermittent, so supplying functional blocks is challenging. Plus, tiny lithium-ion batteries and super capacitors, while power dense, cannot sustain life for extended periods. This talk illustrates how emerging microelectronic systems can draw energy from elusive ambient sources to power tiny wireless sensors.

Lecture 2: Tiny Energy-Harvesting Piezoelectric Chargers

Wireless microsensors and other miniaturized electronics cannot only monitor and better-manage power consumption in emerging small- and large-scale applications (for space, military, medical, agricultural, and consumer markets) but also add energy-saving and performance-enhancing intelligence to old, expensive, and difficult-to-replace infrastructures and tiny contraptions in difficult-to-reach places (like the human body). The energy these smart devices store, however, is often insufficient to power the functions they incorporate (such as telemetry, interface, processing, and others) for extended periods. Still more, replacing or recharging the batteries of hundreds of networked nodes is costly, and invasive in the case of the human body. Harvesting ambient kinetic energy in motion to continually replenish a battery is therefore an appealing alternative, even if relevant technologies are still the subject of ardent research today. This talk discusses the state of the art in miniaturized piezoelectric chargers that draw kinetic energy from motion to charge a battery.

Lecture 3: Light-Harvesting Photovoltaic Charger–Supplies

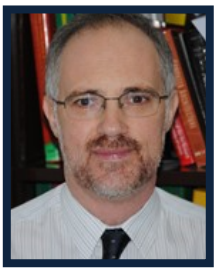
A fundamental challenge wireless microsystems face is size, and in consequence, lifetime because tiny batteries exhaust quickly. Although small fuel cells and atomic sources store more energy than lithium-ion batteries and super capacitors, they supply less power, so they cannot power as many functions. Small batteries and capacitors, however, cannot sustain life for long. Thankfully, the environment holds vast amounts of energy. And of typical sources like light, motion, temperature, and radiation, sunlight produces the highest power density, but only when available. Combining photovoltaic (PV) cells with tiny batteries or capacitors can therefore be more compact, reliable, and longer lasting than any one of these technologies alone. Managing a hybrid system of this sort to supply a milliwatt application, however, requires an intelligent, low-loss charger-supply system. This talk describes how smart PV-sourced microsystems can draw power from tiny PV cells and supplementary power from small batteries to supply a load and replenish the battery with excess PV power.

Lecture 4: Tiny Inductively Powered Battery Chargers

Although wireless microsystems today require less power than ever before, they still cannot fit large enough batteries to sustain them for months or years at a time. Ambient energy is appealing in this respect, but only when an ambient source is available, which is often not the case for structurally embedded microsensors and biomedical implants. Transmitting power wirelessly is often the only practical alternative in these applications. Unfortunately, tiny power receivers capture a small fraction of the power that a wireless source can deliver. So output power is low and its effects on the transmitting coil are barely noticeable. Power receivers should therefore draw as much power as possible, but only as much as breakdown voltages and power losses allow. This talk discusses the state of the art in inductively coupled power receivers that draw power from tiny coils that are millimeters to centimeters away from their transmitting sources.

Biography

Prof. Gabriel A. Rincón-Mora is Fellow of the American National Academy of Inventors (NAI), Institute of Electrical and Electronics Engineers (IEEE), and Institution of Engineering and Technology (IET). He worked for Texas Instruments in 1994-2003, was an Adjunct Professor at the Georgia Institute of Technology (Georgia Tech) in 1999-2001, has been professor at the Georgia Institute of Technology since 2001, and has been visiting professor at National Cheng Kung University in Taiwan since 2011. His scholarly products include 9 books, 4 book chapters, 42 patents, over 170 articles, over 26 commercial power-chip designs, and over 130 international speaking engagements. He was inducted into Georgia Tech's Council of Outstanding Young Engineering Alumni and named one of "The 100 Most Influential Hispanics" by Hispanic Business magazine. He received the National Hispanic in Technology Award from the Society of Hispanic Professional Engineers, Charles E. Perry Visionary Award from Florida International University, Commendation Certificate from the Lieutenant Governor of California, Orgullo Hispano and Hispanic Heritage awards from Robins Air Force Base, IEEE Service Award from the IEEE Circuits and Systems Society (CASS), IEEE Certificate of Appreciation from IEEE CASS, and two Thank a Teacher Certificates from Georgia Tech. He has served as Distinguished Lecturer, General Chair and Co-Chair, Technical Program Chair and Co-Chair, Associate Editor, Guest Editor and Co-Editor, Chapter Chair and Vice-Chair, International Liaison, Steering Committee Member, and Advisory Panel Member on multiple occasions for many IEEE and other international conferences and workshops.



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Lecture 1: Modular Arithmetic based Circuits and Systems for Emerging Technologies and Applications: Deep Neural Networks and Cryptography

Energy efficiency and limited power consumption are key aspects for the next-generation of integrated circuits and systems. Thus, together with the increase of performance, they should drive the design of new architectures and arithmetic units. Unconventional number systems, namely Residue Number Systems (RNS), may hold the answer to these emerging challenges. RNS relies on use of modular arithmetic to perform additions, subtractions and multiplications in parallel without any dependency between the RNS-digits. Due to a few limitations such as conversion overheads and division, only recently RNS have experienced a significant number of advances in its application to new domains, such as Deep Convolutional Neural Networks (DCNN) and cryptography. In this seminar we present a state-of-the-art overview concerning the use of the RNS not only to improve the performance of public-key algorithms but to make them more resistant to attacks. RNS for emerging post-quantum algorithms, namely the ones supporting lattice based cryptosystems (LBCs), and Homomorphic Encryption (FHE) are also covered in this seminar. The potential of RNS for matrix multiplication and the application for the high-performance implementation of deep convolutional neural networks (DCNNs) is unveiled.

Tutorial 1: Modeling Performance and Energy-Efficiency of Multi-Cores: The Cache-Aware Roofline Approach and The Intel Advisor

As architectures evolve towards more complex multi-core designs, deciding what optimizations provide the best trade-off between performance and efficiency is becoming a prominent issue. To help in this decision process, a set of fundamental Cache-aware Roofline Models (CARMs) are presented in this tutorial, which allow characterizing the upper bounds of contemporary parallel architectures for performance, power, energy and energy-efficiency (i.e., multi-core CPU and GPU architectures). These models evaluate how key micro-architectural aspects, such as accessing different functional units or different memory hierarchy levels, affect the attainable performance, power and energy-efficiency.

Recently, the performance CARM was integrated by Intel as a fully supported feature into their proprietary Intel Advisor software tool, and it is described as “an incredibly useful diagnosis tool (...) that developers can use to guide them (in the application optimization process), ensuring that they can squeeze the maximum performance out of their code with minimal time and effort". The proposed models are also rigorously validated on different CPU and GPU architectures by relying on hardware counters and specifically developed performance/power monitoring tools. Experimental results show a very high accuracy of the proposed models, and their ability to provide more intuitive and useful guidelines than the state-of-the-art approaches, when characterizing real-world applications from standard benchmark suites.

Biography

Leonel Sousa received the Ph.D. degree in electrical and computer engineering from the Instituto Superior Técnico (IST), Universidade de Lisboa (UL), Lisbon, Portugal, in 1996. He is currently a Full Professor and

Chair of the Electrical and Computer Engineering Department at the IST and a Senior Researcher with the INESC-ID, an R&D Institute owned by IST, Lisbon, Portugal. Prof. Sousa spent two months in Japan at the beginning of 2016 with a prestigious JSPS Invitation Fellowship for Research, and he has been a Visitant Professor of The Carnegie Mellon University (CM) in the fall semester of 2016/2017. As a professor, he has lectured several undergraduate and graduate courses, in the area of computer architecture, embedded systems and digital systems design and supervised 15 Ph.D. Theses. His research interests include high performance computing, computer architectures, computer arithmetic and multimedia systems. He had offered more than 30 keynotes, invited talks and tutorials, he has authored or co-authored more than 250 papers appearing in international journals and conferences and edited five special issues of international journals. He served in the organization of several international conferences and he is an Associate Editor of the IEEE Transactions on Multimedia, IEEE Transactions on Circuits and Systems for Video Technology, IEEE Access, Springer Journal of Real-Time Image Processing, IET Electronics Letters, and he is Editor-in-Chief of the Springer Journal on Embedded Systems. He was the recipient of several awards, including the DASIP'13 Best Paper Award, the SAMOS'11 "Stamatis Vassiliadis" Best Paper Award, the DASIP'10 Best Poster Award, and several Honorable Mention Awards from the Universidade Técnica de Lisboa/Santander Totta (2007, 2009) and the Universidade de Lisboa/Santander (2016) for the quality and impact of his scientific publications. Prof. Sousa is a member of the Management Committee, and leader of the Working Group 1, of EU COST Action NESUS, member of the IFIP WG10.3 on concurrent systems, Senior Member of IEEE, Fellow of the IET, and a Distinguished Scientist of the ACM.

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Lecture 1: Modeling Cascading Failure in Power Systems from a Network Perspective

This talk will focus on a network approach to model and analyze cascading failures in power systems. Historical data of blackouts in North America (1996 and 2003) provide real failure propagation profiles which contain some stereotypical features. Our network-based model, combining a deterministic physical model for power flow simulation and stochastic methods for estimating failure dynamics, is able to reproduce cascading failure dynamics that capture key features of realistic blackouts. The 2016 Ukranian blackout, however, was confirmed to have been triggered by cyber attacks. It is thus highly relevant to consider a cybercoupled power system model, which can be conveniently obtained from extending the network-based model, resulting in an effective simulation model that can be used to capture key features of the dynamics of failure propagation in cyber-coupled power systems.

Lecture 2: How did Facebook grow? Did Twitter, LinkedIn, WeChat and others grow in the same way? — A Network-Based Universal Growth Law

The growth of the user population of a newly launched product or service is often considered as being controlled by multiple factors like deployment of appropriate business strategy, quality of the product, market readiness, and luck! Recent research in network science has provided convenient access to the construction of models that can describe collective human behaviour. Here, we discuss a model, based on construction of a networked community and two fundamental behaviour of decision making, that can universally describe the growth of the user population of any newly launched product or service. This model leads to a universal growth equation that describes dynamically the size of the user population in terms of the prospective market size and the extents of peer influence and personal choice. We analyse 22 sets of realworld historical growth data of a variety of products and services, and show that they all follow the universal growth equation. The numerical procedure for finding the model parameters allows the market size, and the relative effectiveness of customer service and promotional efforts to be estimated from the available historical growth data. This model can be extended to a variety of practical growth applications. This talk will highlight the role of data, combined with the use of appropriate theory, in many areas of applied research.

Biography

Chi K. Michael Tse graduated with BEng(Hons) and PhD degrees from Melbourne University in 1987 and 1991. He is presently Chair Professor of Electronic Engineering at Hong Kong Polytechnic University, where he served as Head of Electronic Engineering from 2005 to 2012 and on the University Council and Board of Trustees from 2013-2015. Prof. Tse's research interest covers power electronics, nonlinear systems, communications and complex network applications. He was recipient of a number of research prizes including a few Best Paper Prizes from IEEE and other journals, as well as two Gold Medals in the International Inventions Exhibition in Geneva and a Silver Medal in International Invention Innovation Competition in Canada. In 2005 and 2010, he was selected as IEEE Distinguished Lecturer. He serves and has served as Editor in-Chief of IEEE Transactions on Circuits and Systems II, IEEE Circuits and Systems Magazine and NOLTA; as Editor of

International Journal of Circuit Theory and Applications, and as associate editor of a few other IEEE journals. He has served on a number of IEEE committees including the IEEE Fellows Committee and the IEEE Awards Committee. He has been appointed to honorary professorship and distinguished fellowship by a few Australian, Canadian and Chinese universities, including the Chang Jiang Scholar Chair with Huazhong University of Science and Technology and Distinguished Professor-at-Large with the University of Western Australia. He is currently serving on panels of Hong Kong Research Grants Council, Innovation Technology Fund and as steering member of Hong Kong Quality Education Fund. He is a Board Member of the Hong Kong Sinfonietta, a publicly funded flagship orchestra in Hong Kong. Back in his own university, he chairs the culture and art committee which organises events in visual art, theatre and music with public participation. He is an IEEE Fellow and an IEAust Fellow.