



Low Power Methodologies, Techniques and Tools

Date:

September 7th-8th, 2017

Time:

09:00 to 16:00

Location:

**Electronics Engineering School,
Instituto Tecnológico de Costa Rica (TEC)
Central Campus
Cartago, Costa Rica**

Space is limited

To reserve your seat,
please RSVP to
cas.costarica@ieee.org

For details, please visit:
www.sites.ieee.org/costarica-cas/lowpower

This 2-day tutorial will focus on low power design circuits and systems, including techniques, tools and methodologies.

Topics:

- Low Power Design, Systems and Applications.
- Low Power Features of IC and Systems.
- Low Power Design Methodologies
- Power Integrity of Boards and Interconnects

Speakers:

- Dr. Elkim Roa, Onchip UIS, Colombia, "5-10 Gb/s low-power SOC Interfaces based on RISC-V"
- Dr. Alfredo Arnaud, UCU Uruguay, "Ultra Low Power VLSI Analog Design for IMDs"
- Maria J. Quiros, Intel Costa Rica, "Low Power Essentials"
- Jose E. Campos Murillo/Marco Espinoza, Intel Costa Rica, "Power management features in Intel processors"
- Juan M. Sanchez Corrales, Intel Costa Rica, "Scalable methodology to measure power on a HPC cluster"
- Martin Peterburg, Julio Soto, Intel Costa Rica, "Power Integrity Techniques for Optimized Power Consumption & Performance"

Investment: \$200, IEEE Members \$60, IEEE-CASS \$40, Students \$50, IEEE Students \$30 (Coffee breaks included).

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