

IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS

CALL for PAPERS

Low-Power, Adaptive Neuromorphic Systems: Devices, Circuit, Architectures and Algorithms

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Scope and Purpose

The recent success of “Deep neural networks” (DNN) has renewed interest in bio-inspired machine learning algorithms. DNN refers to neural networks with multiple layers (typically two or more) where the neurons are interconnected using tunable weights. Though these architectures are not new, availability of lots of data, huge computing power and new training techniques (such as unsupervised initialization, use of rectified linear units as the neuronal nonlinearity, regularization using dropout or sparsity, etc.) to prevent the networks from over-fitting have led to its great success in recent times. DNN has been applied to a variety of fields such as object or face recognition in images, word recognition in speech or even natural language processing and the success stories of DNN keep on increasing every day.

However, the common training method in deep learning, such as back propagation, tunes the weights of neural networks based on the gradient of the error function, which requires a known output value for every input. It would be difficult to use such supervised learning methods to train and adapt to real-time sensory input data that are mostly unlabeled. In addition, training and classification phases of deep neural networks are typically separated, such that training occurs in the cloud or high-end graphics processing units, while their weights or synapses are fixed during deployment for classification. However, this makes it difficult for the neural network to continuously adapt to input or environment changes in real-world applications. By adopting unsupervised and semi-supervised learning rules found in biological nervous systems, we anticipate to enable *adaptive* neuromorphic systems for many real-time applications with a large amount of unlabeled data, similar to how humans analyze and associate sensory input data. Energy-efficient hardware implementation of these adaptive neuromorphic systems is particularly challenging due to intensive computation, memory, and communication that are necessary for online, real-time learning

and classification. Cross-layer innovations on algorithms, architectures, circuits, and devices are required to enable adaptive intelligence especially on embedded systems with severe power and area constraints.

Topics of Interest

This special issue invites submissions relating to all aspects of *adaptive* neuromorphic systems across algorithms, devices, circuits, and architectures. Possible scalability to human brain-scale computing level with energy-efficient online learning is desired. Submissions are welcome in the following topics or other related topics:

- Spin mode adaptive neuromorphics with devices such as spin transfer nano-oscillator, domain wall memory, tunneling magnetic resistance, inverse spin hall effect, etc.
- Memristive technology based learning synapse and neurons
- Neuromorphic implementations of synaptic plasticity, short-term adaptation and homeostatic mechanisms
- Self-learning synapses (STDP and variants) and self-adaptive neuromorphic systems
- High fan-in scalable interconnect fabric technologies mimicking brain-scale networks
- Circuits and systems for efficient interfacing with post-CMOS memory based learning synapses
- Design methodology and design tools for adaptive neuromorphic systems with post-CMOS devices
- Algorithm, device, circuit, and architecture co-design for energy-efficient adaptive neuromorphic hardware

Important Dates

1. Manuscript submissions due: ~~April 30, 2017~~ May 14, 2017 (**extended deadline**)
2. First decision: July 15, 2017
3. Revised manuscripts due: August 15, 2017
4. Final Decision: October 15, 2017
5. Final manuscripts due: November 15, 2017

Request for Information

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