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Call for Papers

Energy-Quality Scalable Circuits and Systems for Sensing and Computing: from Approximate, to Communication-Inspired and Learning-Based

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Scope and purpose

The historical **100X/decade energy down-scaling** is currently being threatened by the slowing down of Moore's law, and the limited prospective energy gains from approaches that have been already exploited extensively (e.g., heterogeneous systems, ultra-low voltage, parallelism). Major shifts from traditional sensing/processing paradigms are now mandatory, and new design dimensions and tradeoffs that enable further energy reductions need to be explored.

As design dimension to continue the exponential energy down-scaling, ample opportunities have been recently demonstrated in **energy-quality (EQ) scalable circuits and systems**, which dynamically and explicitly trade off energy and quality from sensor to circuit, architecture, algorithm, and up to system level. Energy-quality scalable designs minimize energy at run time, based on the actual quality target that is set by the specific task, the context (e.g., recent events, power/energy availability), and the specific dataset at hand (e.g., more/less complex or noisy data). EQ scalable systems indeed reduce energy by treating quality as an explicit knob, eliminating the **quality slack** that is traditionally imposed by worst-case design across different applications, contexts, datasets, and the pessimistic design margin to counteract process/voltage/temperature variations. However, such "just-enough" or "on-demand" quality management cannot be pursued based on traditional metrics that are only vaguely related to quality, or are application unspecific (e.g., error rate).

Thanks to their inherent resiliency against noise/errors/inaccuracies/approximations and hence strong potential for EQ scaling, prominent examples of **relevant applications** are multimedia, motion sensing/wearables, smart bio-sensors, smart sensors for the Internet of Things (IoT), machine learning (e.g., deep learning), computer vision, audio processing, speech recognition, physical data aquisition/processing, data analytics, among many others. Being application-dependent, the **quality** is quantified differently in each application domain through well-established metrics, such as accuracy/sensitivity/specificity in machine learning, PSNR (or other perceptive metrics) in video processing, false alarm rate in IoT sensors, misclassification rate in signal classification, SNR in signal processing, mean error distance in approximate digital circuits, perplexity in unsupervised learning, entropy in random key generation, effective resolution in analog-to-digital conversion, tracking length in visual object tracking, missed event detection rate in implantables and bio-medical circuits, among the others.

From the **state of the art** viewpoint, various concepts and demonstrations that save energy at degraded quality have been proposed within the general framework of EQ-scalable circuits and systems, and have been mostly focused on processing. Some examples are approximate computing (e.g., precision adjustment, gate pruning), communication-inspired approaches (e.g., algorithmic noise tolerance, voltage/frequency overscaling), stochastic and probabilistic computing (e.g., probabilistic CMOS, emerging devices), learning-based approaches (e.g., adaptation via background or foreground on-chip training). Furthermore, we are witnessing an interesting **convergence of EQ scalable systems and machine learning**, where the noise resilience and the learning ability of machine learning circuits/algorithms can be leveraged to achieve graceful quality degradation (i.e., wider opportunities for energy saving), and allow significant circuit/architectural simplifications and imperfections by compensation with on-chip training. Also, various demonstrations on EQ-scalable System on Chip (SoC) building

blocks with substantial energy reductions have also been presented, such as memories, analog-to-digital converters, microprocessors, accelerators for vision, and engines for machine learning.

At this juncture, several **challenges** need to be addressed to extract the energy gains expected from EQ scaling, while systematically and efficiently design truly scalable systems. For example, new methods and techniques to inexpensively insert EQ knobs in all SoC components are needed, from analog and sensor interfaces to processing, power management, algorithms, and software. As other challenges, quality needs to be inexpensively sensed at low area and energy/power penalty, to retain the potential energy advantages offered by EQ scaling. Methods and techniques are also needed to make the quality degradation graceful, to extend the energy savings when operating at lower quality. Novel design paradigms and optimization methodologies are also needed to supervise the energy-quality control, based on an underlying application-to-hardware framework. Novel frameworks are also needed to make EQ scaling techniques more generally applicable (e.g., general-purpose platforms), spanning multiple levels of abstraction (e.g., circuit, architecture, algorithm, software) and sub-systems. In addition, innovative frameworks and techniques are needed to minimize the overall energy via true adaptation (e.g., on-chip learning), while keeping quality within bounds in a real-time and context-aware fashion.

The above challenges require a highly inter-disciplinary collective effort, as they lie at the intersection of circuits and systems, solid-state circuits, CAD, architectures, machine learning, signal processing (e.g., computer vision, audio), and the related communities. Accordingly, the authors of this special issue will be invited to submit their **paper contributions** on the following and other topics related to energy-quality scalable systems:

- sensors and circuits (analog, digital, power management) with the capability to dynamically trade off energy and quality
- lightweight methods for quality enhancement and graceful degradation, from circuits (e.g., variation-resilient design, intentional under-design), to architectures (e.g., approximate), algorithms (e.g., quality-aware termination of iterative algorithms), and systems (e.g., context-aware systems for relaxed quality requirement)
- run-time quality sensing, control and adaptation at different levels of abstraction (e.g., circuit, architecture) and in different sub-systems (e.g., analog, digital, power management)
- relaxed sensor and circuit design via compensation of non-idealities through off/on-chip learning
- architecture/algorithm/software overdesign elimination through "just-enough" quality assurance
- dynamically scalable approximate, communication-inspired, stochastic, learning-based circuits and systems
- HW/SW co-design approaches to adaptively manage the energy-quality tradeoff
- design methodologies, programming models, language abstractions and compiler support for structured and disciplined energy-quality scaling in computation, communication and data transfer, including quality control and recovery from over-approximation
- quality-aware middleware at all processing layers, from low-level runtime to high-level scheduling
- quality modeling, monitoring and run-time adaptation in general-purpose and application-specific hardware
- approximate, communication-inspired and learning-based frameworks that adapt the quality to the dataset, task, context and application
- innovative case studies and emerging applications leveraging energy-quality scaling, with significant time- and energy-to-solution reduction (e.g., machine learning).

Important dates

- Manuscript submissions due: December 15th, 2017
- First round of reviews completed: February 15th, 2018
- Notification to authors: February 22nd, 2018
- Revised manuscript submissions due: March 22nd, 2018
- Second round of reviews completed: May 15th, 2018
- Notification of acceptance: June 15th, 2018
- Final manuscripts due: July 1st, 2018
- Target publication date: September 2018.

Submission Guidelines

All submitted manuscripts must (i) conform to JETCAS formatting requirements and page-count limits (from 8 to 14 pages – see guidelines at http://ieee-cas.org/pubs/jetcas/submit-manuscript); (ii) incorporate no less than 50% of new (previously unpublished) material; (iii) be submitted online at https://mc.manuscriptcentral.com/jetcas. Please note that you need to select "Special Issue on Energy-Quality Scalable Circuits and Systems for Sensing and Computing" when you submit a manuscript to this journal issue.