

Lecture abstract(s) and speaker biographies (in alphabetical order of speaker last name)

Ramachandra Achar (achar@doe.carleton.ca):

Department of Electronics, Carleton University, Ottawa, Canada

Lecture #1: Meeting the Signal Integrity Challenges of High-Speed Designs

The intense drive for signal integrity has been at the forefront of rapid and new development in CAD algorithms focused on high-speed circuits and systems. With increasing demands for high signal speeds coupled with decreasing feature sizes, interconnect effects such as signal delay, distortion and crosstalk become the dominant factors limiting the performance of high-speed systems. On the other hand, interconnect structures can be diverse and present at any of the hierarchical packaging levels including integrated circuits, printed circuit boards, multi-chip modules and backplanes. If not considered during the design stage, interconnect effects can cause failed designs. Since extra iterations in the design cycle are costly, accurate prediction of these effects is a necessity in high-speed designs. Although conventional CAD tools such as SPICE are used routinely by many engineers for simulation and general circuit analysis, these tools do not handle adequately the new emerging challenges of interconnect effects.

In this talk, high-frequency issues and signal integrity in high-speed designs will be discussed. Advanced signal integrity modeling/simulation strategies applicable to various levels of system hierarchy will be described. Also the underlying concepts leading to high-frequency effects, signal parameters and time-frequency relations will be reviewed. Particular emphasis will be placed on distributed, long and large coupled interconnects. Efficient modeling strategies based on matrix rational approximation (MRA) and delay extraction based passive macromodeling technique (DEPACT) to handle long delays in signal paths will be described. Simulation difficulty arising due to large number of coupled lines will be addressed via parallel and order reduction based algorithms. Modeling approaches to handle high-frequency current distribution related effects, such as skin, proximity and edge effects will be considered. Particular emphasis will be placed on preserving the macromodel properties, such stability, causality and passivity during model generation.

Various levels of interconnect modeling will be considered and the applications cover wide spectrum of on-chip, multichip, packages, printed circuit boards, backplanes/connectors. Unlike conventional simulators, the new methods not only guarantee the stability of transient simulations by preserving macromodel properties such as causality and passivity, but also provide several orders of speed-up.

Lecture #2: Advanced Modeling and Simulation Strategies for Power Integrity in High-Speed Designs

Preserving power integrity has become one of the most challenging tasks facing designers of modern multifunction and miniature electronic circuits and systems. As devices scale and more transistors are integrated into a single integrated circuit, the power and current levels are expected to increase with a corresponding decrease in voltage. With gigabit signals being propagated through the package and board, the ability to supply clean power to the transistor circuits becomes very critical. Voltage variations may lead to reduced noise margins and may increase propagation delays. Reduced noise margins can cause false switching of gates whereas increased delays may lead to timing errors and impede the overall operating speed of the chip. These issues make the design of robust and reliable power distribution networks (PDNs), consisting of chips, packages and printed circuit boards, essential to the success of the high-speed and high-density products.

Modeling of power grids based on RC extraction has been popular; however, the demand for including inductance has been growing in the recent years. However, modelling of PDNs in modern VLSI circuits leads to large circuits, often consisting of millions of circuit elements. Hence, the simulation of PDNs becomes computationally expensive and time consuming. Typically, direct solvers offer speed-ups over iterative solvers for power grid analysis. However, they suffer from high memory consumption and are unyielding to implementation in parallel domains. Iterative solvers, on the other hand, converge very slowly but are memory efficient.

In this talk, components of power distribution networks, power delivery mechanisms, power integrity issues and the underlying concepts will be reviewed. Efficient methodologies will be discussed for modeling and simulation of modern PDNs. Comparative merits of RC and RLC based models and their impact on simulations will be discussed. Methods based on waveform relaxation (WR) approaches to combine the merits of both direct and indirect solvers will be presented. Novel partitioning schemes based on block row partitioning and fast convergence mechanisms will be described. Also CPU and memory efficient parallelization schemes for power grid analysis based on physical and time-domain partitioning will be presented. Design and optimization case studies will be presented to demonstrate the applicability of the new methods, which yield significant speedup compared to existing techniques.

Speaker's biography: Prof. Achar is an active researcher contributing to the advancement of computer-aided design tools and methodologies for analysis of high-frequency integrated circuits and systems. He pioneered several milestone algorithms and methodologies for signal and power integrity modeling and analysis. He has published over 150 peer-reviewed articles in international transactions/conferences, six multimedia books on signal integrity and five chapters in different books. Dr. Achar received several prestigious awards, including Carleton university research achievement award (2004) & (2010), NSERC (Natural Science and Engineering Research Council) doctoral medal (2000), University Medal for the outstanding doctoral work (1998), Strategic Microelectronics Corporation (SMC) Award (1997) and Canadian Microelectronics Corporation (CMC) Award (1996). He was also a co-recipient of the IEEE advanced packaging best transactions paper award (2007). Several of his contributions have already been implemented by leading industries, such as Analog Devices, Boston, IBM, T. J. Watson Research Center, NY, CST, Germany, etc.

He serves as the chair of the joint chapters of CASS/SSCS/EDS societies of the IEEE Ottawa section (since 2005). Under his leadership, Ottawa CASS chapter was awarded the best chapter award for year 2009 (region 1-7). He currently serves as the general co-chair for EPEPS 2010 & 2011, as a member of the Steering Committee of EDAPS and also as a TPC member and track chair of several leading IEEE conferences such as EPEPS, SPI, EDAPS, IWMS and MNRC etc. He also previously served as the chair of interconnect and circuit simulation subcommittee of ICCAD TPC (2007-2008). He is a regular consultant, panelist, reviewer and organizer on computer-aided design, signal integrity and high-speed issues. Dr. Achar has delivered over 40 invited talks worldwide, on above topics.

Dr. Achar received the B. Eng. degree in electronics from Bangalore University (90), M. Eng. degree in micro-electronics from BITS, Pilani (92) and the Ph. D. degree from Carleton University (98). He is currently a professor at Carleton University. Prior to joining Carleton faculty, he served in various capacities in leading research labs, including T. J. Watson Research Center, IBM (95), L&T Ltd., Mysore (92), Central Electronics Engineering Research Institute, Pilani, (92) and Indian Institute of Science, Bangalore (90). Further information can be found at <http://www.doe.carleton.ca/~achar/>.

Charles J Alpert(alpert@us.ibm.com)

BM Corp, Research Division, Yorktown Heights, NY, USA

Lecture # 1 Physical Synthesis: The Good, the Bad, and the Ugly

A decade ago, physical synthesis emerged as a design aid to address the problem of optimization after cell placement caused by increasingly high wire delays. Early physical synthesis tools were fairly simplistic scripts wrapped around traditional placement and logic synthesis optimizations. Advances and technology have put increasing pressure on physical synthesis tools not only to perform timing takedown with increasingly aggressive frequencies but also to manage many additional design constraints like power management, routability, and variability. Trying to solve all aspects of physical implementation simultaneously creates massive complexity for both the tool and the designer. This talk overviews the basics of physical synthesis and describes how physical synthesis flow weaves together its key components to perform timing and routing closure. It explains how the complexity of physical synthesis and corresponding designs have mushroomed to create design problems that are not just bad, but sometimes downright ugly.

Lecture # 2 What Makes a Design Difficult to Route

Traditionally, the goal of physical synthesis has been to produce a physical realization of the input netlist that meets its timing constraints with minimum area. However, design routability has migrated from a secondary objective to potentially the primary objective, in no small part due to the myriad of rules and constraints that emerge with each successive technology. This work overviews the complexities with modeling congestion during physical synthesis and discusses how strategies in buffering, placement, layer assignment and synthesis that can provide some relief.

Speaker's biography: Charles (Chuck) Alpert was born in Bethesda, Maryland in 1969. He received a B.S. Degree in Math and Computational Sciences and a B.A. degree in History from Stanford University in 1991. Upon receiving a Department of Defense Fellowship, he enrolled the UCLA Computer Science department and received his doctoral degree in 1996. Upon graduation, Chuck joined IBM's Austin Research Laboratory (ARL) where he remains still. In 2005 he was made the technical lead of the tools group, and in 2007 he was appointment manager of the Design Productivity Group. The mission of his team of 12 researchers is to develop design automation tools and methodologies to improve designer productivity and reduce design cost. Chuck is the proud husband to his wife Cheryl and their three girls Candice, Ciara, and Charlie. Chuck was named IEEE Fellow in 2005. He has published over 100 conference and journal publications. He has received three Best Paper Awards from the Design Automation Conference. He is a co-author of the Handbook of Physical Design Automation. He has filed for 55 patents and 30 have been issued, and he recently was named an IBM Master Inventor. He has served as the general chair for the Tau Workshop on Timing Issues, the International Symposium on Physical Design, and CANDE. He has served as an associate editor of IEEE Transactions on Computer-Aided Design since 2003. For his mentoring work, he received the Semiconductor Research Corporation's Mahboob Khan Mentor Award in 2001 and 2007. Chuck was selected to attend the 2010 National Academy of Engineering's FOE meeting, which is a forum for top engineers in the country between the ages of 30-45. Chuck has a strong algorithmic background in combinatorial optimization and graph theory, and his research interests are primarily related to applying these techniques to solve problems in the design closure space, especially related to physical synthesis.

Magdy Bayoumi(magdy1112@yahoo.com)

University of Louisiana at Lafayette, Lafayette, Louisiana, USA

Lecture # 1 Wireless Sensors Networks: Current and Future Challenges

Computers, communication, and sensing technologies are converging to change the way we live, interact, and conduct business. Wireless sensor networks reflect such convergence. These networks are based on collaborative efforts of a large number of sensor nodes. They should be low-cost, low-power, and multifunction. These nodes have the capabilities of sensing, data processing, and communicating. Sensor networks have a wide range of applications, from monitoring sensors in industrial facilities to control and management of energy applications to military and security fields. Because of the special features of these networks, new network technologies are needed for cost effective, low power, and reliable communication. These network protocols and architectures should take into consideration the special features of sensor networks such as: the large number of nodes, their failure rate, limited power, high density, etc. In this talk the impact of wireless sensor networks will be addressed, several of the design and communication issues will be discussed, and a case study of a current project of using such networks in drilling and management off-shore oil and natural gas in the gulf region will be given.

Lecture # 2 Towards Green Circuits and Systems

Many of microelectronics devices and digital systems, especially wireless sensors networks, represent environment hazards. The promise of "Green systems" will depend on the following characteristics:

- * Minimizing the amount of energy required to actually operate the involved circuits.
- * minimizing the number of required devices and their associated interconnections.
- * Using a true battery-free devices, by utilizing energy harvesting devices that can utilize energy harvested directly from the environment;e.g. light, motion, and vibration.
- * Developing efficient cooling techniques.

In this talk, developing Green circuits and systems will be addressed, several of the design and communication issues will be discussed, and a case study of a current project of developing green wireless sensors networks will be given.

Speaker's biography: Prof. Magdy A. Bayoumi is Director of The Center for Advanced Computer Studies (CACS) and Department Head of the Computer Science Department at the University of Louisiana at Lafayette (UL Lafayette). He is, also, the Loflin Chair Professor of Computer Science. Dr. Bayoumi has been a faculty member in CACS since 1985. He received the B.Sc. and M.Sc. degrees in Electrical Engineering from Cairo University, Egypt; M.Sc. degree in Computer Engineering from Washington University, St. Louis; and the Ph.D. degree in Electrical Engineering from the University of Windsor,

Canada. Dr. Bayoumi's research interests include VLSI Design Methods and Architectures, Low Power Circuits and Systems, Digital Signal Processing Architectures, Parallel Algorithm Design, Computer Arithmetic, Image and Video Signal Processing, Neural Networks, Wideband Network Architectures, and Wireless Sensor Networks.

Dr. Bayoumi is leading a research group of 15 Ph.D. and 10 M.Sc. students in these research areas. He has graduated 43 Ph.D. and about 125 M.Sc. students. He has published over 350 papers in related journals and conferences. He edited co-edited and coauthored 5 books in his research interest. He was the guest editor of five special issues in VLSI Signal Processing and VLSI Design, the latest was on "SoC Design", IEEE Proceedings. Dr. Bayoumi has one patent on "On-Chip Learning." And two on "Low Power Circuits Design". He has given numerous invited lectures and talks nationally and internationally. He has consulted in industry.

Dr. Bayoumi was the vice president for technical activities of the IEEE Circuits and Systems (CAS) Society and then the VP for conferences of CAS. Where he has served in many editorial, administrative, and leadership capacities. He is one of the founding members of the VLSI Systems and Applications (VSA) Technical Committee (TC) and was the past chair. He was the founder of the CAS TC on Circuits and Systems for Communication. He was the chair of the Signal Processing Society TC on Design and Implementation of Signal Processing Systems. He was the general (or Co-general) chair of The Midwest Symposium on Circuits and Systems, 1994 in Lafayette and 2003 in Cairo, SiPS 2000 in Lafayette and SiPS 2011 in Beirut, 1998 Great Lakes Symposium in Lafayette, VLSI 2004 in Lafayette, Computer Architecture for Machine Perception 1993 in New Orleans and Montreal in 2007, ISCAS 2007 in New Orleans, and ICIP 2009 in Cairo.

Eugenio Culurciello (eugenio.culurciello@yale.edu):

Associate Professor, Electrical Engineering, Yale University, New Haven, Connecticut, USA

Lecture # 1: Modeling the human visual system in hardware

In this talk I will present our state-of-the-art work on neuromorphic hardware models of the mammalian visual system. In particular, I focus on modeling retinal pre-processing and the ventral visual pathway, with the goal of categorizing tens of objects from multi-megapixel cameras. We have designed and tailored multiple generation of bio-mimetic artificial retinas that can extract motion and contour information from the scene. We are developing light-invariant representations of the visual information for use in a hierarchical model of the ventral pathways, in particular V1, V2, V4 and IT. We have designed and implemented an innovative data-flow graphic-processing unit (GPU) – called VPU – Vision Processing Unit, that can instantiate very large neural networks (several million neurons), learn from data, and perform in real time and faster! We will show our implementation of convolutional neural networks in programmable digital hardware (FPGA) and on custom micro-chips (ASIC).

Applications are in advanced modeling, neuroscience hypothesis testing, robotics, security, monitoring, cognitive hardware and sensor networks – to name a few.

Speaker's biography: Eugenio Culurciello received the Laurea (M.S.) degree in Electronics Engineering from the University of Trieste, Italy, in July 1997. His MS thesis work was developed at the Johns Hopkins University with professor Ernst Niebur. He joined professor Andreas G. Andreou laboratory in January 1998 as a graduate student. He received a second M.S. degree in Electrical and Computer Engineering from the Johns Hopkins University, Baltimore. In September 2004 he received the Ph. D. degree in Electrical Engineering at The Johns Hopkins University. In July of 2004, Mr. Culurciello joined the Department of Electrical and Computer Engineering at Yale University where he currently is an associate professor and directs Yale's 'e-Lab', a VLSI laboratory. His research aims at extending the performance of CMOS circuits by means of advanced VLSI technologies. He focuses on topologies and circuits that take advantage of the native properties of devices to augment their computational and communication capabilities.

His research interests originate from the identification of the physical limitations of current integrated circuits technologies. These limitations suggest efficient algorithms to encode information in ways that are compatible with the physical medium where computation and communication is performed. His research interests include: analog and mixed-mode integrated circuits with applications to biomedical instrumentation, biological sensors and interfaces, implantable sensors, telemetry sensors, biomimetic sensors. Bio-inspired vision sensory systems and application in Sensor Networks, efficient communication systems, event-based communication and processing. Silicon on Insulator and Silicon on Sapphire circuit

design, models of devices, analog-to-digital conversion, radio circuits, radiation tolerant design and isolation amplifiers. He is the author of the book "Silicon-on-Sapphire Circuits and Systems, Sensor and Biosensor interfaces" published by McGraw Hill in 2009.

Ralph Etienne-Cummings(retienne@jhu.edu):

Johns Hopkins University, USA

Lecture #1: Distinguished Lectures in Neuromorphic Engineering

Imagine having a car that is able to drive itself or a robot that is able to perform tasks ranging from the tedious (e.g. housekeeping) to the dangerous (flying military aircrafts) and even to the difficult (building space stations) without human supervision. This is the stuff of science fiction. Today's robots make certain tasks easier but still require remote supervision and control by humans [1]. Intelligent robots need to be able to interact with objects in their surroundings with minimal human involvement. This involves three steps: (1) detecting the presence of the object, (2) recognizing the object – determining whether it is an obstacle to be avoided, an item to be retrieved, or perhaps a tool required for a particular task [2], and (3) tracking the trajectory of the object – determining how and when to react to it. While these steps are computationally difficult, humans and other primates are able to perform them easily. They are able to rapidly and effortlessly identify and categorize diverse objects in cluttered scenes under widely varying viewing conditions, such as changes in position, rotation and illumination. Although the density of processing elements in engineered systems have approximated, in some cases surpassed, those of biological systems, they are still unable to match the level of proficiency and speed of biological visual systems. Substantial research is still needed at the computational architecture level to move the performance of engineered systems towards that of biology. The work I will present takes some strides in that direction. We are working towards the development of an autonomous, continuous-time visual system that emulates visual information processing in the primate visual cortex. This multi-stage system will utilize large-scale arrays of identical silicon neurons to build a biologically-plausible model of its biological counterpart. In this talk, I will describe (1) the design a neural array transceiver with neurons and synapses that more closely mimic biology, (2) implement silicon facsimiles of cortical simple cells, complex cells, and composite feature cells according to the hierarchical model of primate visual cortex of proposed by Riesenhuber and Poggio, and (3) focus on recent research on modeling the spinal cord locomotion networks in silicon, and speculate about what the future holds for this research, particularly in the area of fully neurally integrated prosthetic limbs and biomorphic robots.

Speaker's biography: Ralph Etienne-Cummings received his B. Sc. in physics, 1988, from Lincoln University, Pennsylvania. He completed his M.S.E.E. and Ph.D. in electrical engineering at the University of Pennsylvania in December 1991 and 1994, respectively. Currently, Dr. Etienne-Cummings is a professor of electrical and computer engineering, and computer science at Johns Hopkins University (JHU). He is the former Director of Computer Engineering at JHU and the Institute of Neuromorphic Engineering (currently administered by University of Maryland, College Park). He is also the Associate Director for Education and Outreach of the National Science Foundation (NSF) sponsored Engineering Research Centers on Computer Integrated Surgical Systems and Technology at JHU. He has served as Chairman of the IEEE Circuits and Systems (CAS) Technical Committee on Sensory Systems and on Neural Systems and Application, and was re-elected as a member of CAS Board of Governors from 1/2007 – 1/2009. He was also the General Chair of the IEEE BioCAS 2008 Conference. He was also a member of Imagers, MEMS, Medical and Displays Technical Committee of the ISSCC Conference from 1999 – 2006. He is the recipient of the NSF's Career and Office of Naval Research Young Investigator Program Awards. In 2006, he was named a Visiting African Fellow and a Fulbright Fellowship Grantee for his sabbatical at University of Cape Town, South Africa. He was invited to be a lecturer at the National Academies of Science Kavli Frontiers Program, held in November 2007. He has also won publication awards, including the 2003 Best Paper Award of the EURASIP Journal of Applied Signal Processing and "Best Ph.D. in a Nutshell" at the IEEE BioCAS 2008 Conference, and has been recognized for his activities in promoting the participation of women and minorities in science, technology, engineering and mathematic. His research interest includes mixed signal VLSI systems, computational sensors, computer vision, neuromorphic engineering, smart structures, mobile robotics, legged locomotion and neuroprosthetic devices. He has published ~175 technical articles, 1 book, 7 book chapters and holds 3 patents on his work in these subjects.

Ling Guan(lguan@ee.ryerson.ca):

Ryerson University

Lecture #1: Optimal Resource Allocation for Video Streaming over Distributed Communication Systems

Recent years have witnessed a dramatic growth in multimedia applications. Many multimedia applications involve real-time video communications over distributed systems. Distributed systems share two common characteristics. Firstly, each node only knows of its neighbors and is lacking of global knowledge. Secondly, there is typically no centralized controller that can coordinate the behaviors of every node. Examples of such distributed systems are Peer-to-Peer (P2P) networks, wireless ad hoc networks, and wireless sensor networks. In this lecture, we present our recent achievements in maximizing the performance of video and multimedia streaming over distributed visual communication networks through optimally allocating resources using distributed algorithms. We will begin with a brief introduction to convex optimization and the associated duality properties. Then, we will reveal how this optimization principle can be applied to resource allocation in distributed video communication infrastructures, for systems including a) a hybrid-forwarding Peer-to-Peer Video-on-Demand architecture to fully utilize buffer and storage resources, and the maximization of throughput by optimal link rate allocation; b) a distributed cross-layer optimization method to jointly optimize the source rate, the routing scheme and power allocation by using hierarchical dual decompositions in video streaming over wireless ad hoc networks; and c) a distributed algorithm to maximize network lifetime in wireless visual sensor networks by mutually optimizing the source rates, the encoding powers and the routing scheme. Simulation results will be provided to demonstrate the effectiveness of this optimization framework. In the last portion of this tutorial, we extend the optimization framework onto another key problem in asynchronous P2P (A-P2P) video streaming, the streaming capacity problem. This problem is defined as the maximal streaming rate that every user can receive. Due to the upload bottleneck, the streaming capacity in the A-P2P system is limited. In solving the problem, we introduce helpers in the A-P2P system, and then optimize helper resources to improve the streaming capacity by using a distributed algorithm to optimize the link rates. Simulation results show that our A-P2P system with optimized helpers can obtain a much higher streaming capacity compared to the conventional A-P2P systems.

Lecture #2: Methods and Techniques for Multimodal Information Fusion

The rapidly developing world of digital technologies continues to profoundly change the way we access information and communicate. These technologies can affect learning and education, accessing services, conducting business and creating entertainment, creating new media artworks, and providing health-care. As the digitization and encoding of data become more affordable, computers and web-based database systems store and manipulate voluminous digital data from multiple sensors or multimodal data sources. However, our ability to deal with information from different sources coherently has not kept pace. This lecture will begin with a comparison of information systems using unimodal sources and those using multimodal sources from an information theoretic viewpoint. Practical examples will be discussed to illustrate the importance of fusion of multimodal data in our everyday life. The three levels of information fusion will be covered: feature level, score level and decision level. The pros and cons of each of these three will be discussed. Feature level fusion combines the features extracted from the source data, it is a simple approach and may suffer from "curse of dimensionality." With a proper normalization scheme, fusion at score level may provide satisfactory results by combining the scores generated from multiple classifiers using multiple modalities. Decision level fusion generates final results based on the decisions from multiple modalities or classifiers using methods such as majority voting. We will then turn to the design of multimodal fusion systems which is critically dependent on the characteristics of data as well as the requirement of the application. For example, a multimodal biometric system can utilize the physical traits such as face, fingerprint, and behavioral (gaits and emotion) in isolation or through a combination. We will highlight the sets of points that need to be considered in designing fusion systems, such as, information sources, feature extraction method, fusion level and architecture, and if any background knowledge needs to be embedded. Several cases in multimodal fusion will be presented, including a) Image/video retrieval; b) Human emotion/intention recognition; c) Fusion of complimentary information for robust speech recognition; and d) Integration of information from emotion, gait, and hand gestures to help elderly and physically disabled people in community houses or their homes.

Speaker's biography: Ling Guan is a Professor of Electrical Engineering and a Tier I Canada Research Chair in Multimedia at Ryerson University, Canada. He was on the Faculty of Engineering at the University of Sydney, Australia from 1993 to 2000, and held visiting positions at British Telecom (1994), Tokyo Institute of Technology (1999), Princeton University (2000),

Microsoft Research Asia (2002, 2009), National ICT Australia (2007) and Hong Kong Polytechnic University (2008-2009). Prof. Guan is a leading expert in image and multimedia signal processing and communications, having made seminal contributions to modeling and recognition of human skills and activities, semantic image and multimedia retrieval, and optimal resource allocation in distributed visual communication networks. He has authored more than 300 scientific publications, including seven books, 77 journal papers and two patents, and has been invited to present keynote, plenary and invited speeches, and tutorials at various international conferences, government agencies and research centers. Prof. Guan has served as associate editor and guest editor for Proceedings of the IEEE, IEEE Transactions on Multimedia, IEEE Transactions on CSVT, IEEE Transactions on Neural Networks, IEEE Transactions on Evolutionary Computation, IEEE Signal Processing Magazine, IEEE Computational Intelligence Magazine and eight other international journals. He has led the organization of many international conferences, including the General Chair of the 2006 IEEE International Conference on Multimedia and Expo, the General Co-Chair of the 2008 ACM Conference on Image and Video Retrieval, the Founding General Chair of the IEEE Pacific-Rim Conference on Multimedia in 20 the Founding General Chair of the IEEE Symposium on Computational Intelligence for Image and Signal Processing in 2007 and 00 . Prof. Guan is an IEEE Fellow, a Fellow of the Engineering Institute of Canada and the recipient of numerous prestigious awards, including the Best Paper Award from the Pacific-Rim Conference on Multimedia(2007), the Best Paper Award from IEEE Transactions on Circuits and Systems for Video Technology (2005), the Ontario Distinguished Researcher Award (2002), an Invitation Fellowship from Australian Academy of Sciences/Japan Society for the Promotion of Sciences (1999) and a British Telecom Visiting Fellowship (1994).

Jaeseok Kim(jaekim@yonsei.ac.kr)

Yonsei University, Korea

Lecture #1: Modem SoC design for IEEE 802.11n WLAN systems

IEEE 802.11n WLAN system is a breakthrough technology that enables Wi-Fi networks to deliver at least 100 Mbps throughput at the MAC SAP (more than 200~300 Mbps data rate at physical layer) by utilizing OFDM & MIMO technologies. There are two parts in the IEEE 802.11n standard: PHY (Physical layer) and MAC (Medium Access Control layer). In order to increase the data rate at PHY, MIMO and SDM technologies are employed and new frame aggregation schemes are adopted to improve data transfer efficiency at the MAC layer. The design of this modem chip which uses the above technologies is a big challenge for design engineers in the circuit and system field. This lecture will introduce a SoC design methodology and provide an overview of the design process for a high-speed wireless communication modem like IEEE 802.11n WLAN system. Then, it will focus on the major issues in algorithm and hardware design for PHY and MAC parts, respectively. Finally, it will cover the test environments of these designs followed by some concluding remarks. The detailed contents of this lecture are as follows:

1. SoC design methodology & process
2. Overview of IEEE 802.11n WLAN modem design process.
 - (1) IEEE 802.11n standard & system specification
 - (2) Algorithm design procedure
 - (3) Channel & system modeling issues
 - (4) Hardware design procedure
 - (5) Test & verification plan
3. Design of PHY(physical layer) part
 - (1) Description of standard feature
 - (2) PHY system architecture
 - (3) MIMO and SDM technologies
 - (4) MIMO detection schemes
 - (5) Algorithm design & Performance evaluation
 - (6) Hardware design of functional blocks
 - (7) Top level integration & verification
4. Design of MAC part
 - (1) Description of standard feature
 - (2) MAC protocol & system architecture
 - (3) Algorithm design & Performance evaluation

- (4) H/W & S/W partitioning issues
- (5) H/W & S/W design and co-verification
- (6) Top-level verification
- 5. Test environments.
 - (1) Testing environment
 - (2) FPGA implementation and testing
 - (3) Chip fabrication & testing
- 6. Concluding remarks

My research team developed an IEEE 802.11n modem (PHY & MAC) SoC using 3x3 MIMO technology with some patented ideas in 2009. This newly developed technology & IP were transferred to industries in the same year. Now we are focusing on the development of new algorithms and architectures for Gbps-level WLAN and LTE-advanced modem SoC.

Lecture #2: Low-power modem SoC design for WiMedia UWB systems

The WiMedia UWB system has been proposed for a WPAN which can support data rates up to 480Mbit/s for short-ranges (within 10m) at very low energy levels by using a large portion of the radio spectrum (528MHz). Most applications of the UWB system are data collection from wireless sensors, wireless USB, wireless monitors and printers, and precision locating and tracking applications. FCC authorizes the unlicensed use of UWB in the range of 3.1 to 10.6 GHz. The FCC power spectral density emission limit for UWB emitters operating in the UWB band is -41.3 dBm/MHz. This limit requires low-power architecture design techniques for modem SoC combined with RF circuit design.

This lecture will provide some guidances for the low power architecture design for WPAN, low-complexity implementation of DCM demodulation and collision avoidance techniques that are needed in the UWB system. This lecture will introduce a SoC design methodology and provide an overview of the design process for a wireless personal area network (WPAN) like the UWB system. Then, it will focus on the major issues in algorithm and hardware design for PHY and MAC parts, respectively. Finally, it will cover the test environments of these designs followed by some concluding remarks.

The detailed contents of this lecture are as follows:

- 1. SoC design methodology & process
- 2. Overview of WPAN UWB modem design process.
 - (1) WiMedia UWB standard & system requirements
 - (2) Algorithm design procedure
 - (3) Channel modeling issues
 - (4) Low power architecture design issues
 - (5) Test & verification plan
- 3. Design of PHY part.
 - (1) Description of standard feature
 - (2) PHY system architecture
 - (3) Time-synchronization technologies
 - (4) DCM demodulation techniques
 - (5) Algorithm design & Performance evaluation
 - (6) Low power hardware design
 - (7) Top level integration & verification
- 4. Design of MAC part.
 - (1) Description of standard feature
 - (2) MAC protocol & system architecture
 - (3) Collision avoidance techniques
 - (4) Algorithm design & Performance evaluation
 - (5) H/W & S/W partitioning issues

- (6) H/W & S/W design and co-verification
 - (7) Top-level verification 5. Test environments.
 - (8) Testing environment
 - (9) FPGA implementation and testing
6. Concluding remarks

My research team developed an UWB modem (PHY & MAC) SoC using some patented ideas in 2008. Now we are focusing on the development of new algorithms and architectures for Gbps-level UWB and low-rate IR-UWB modem SoCs.

Speaker's biography: Professor Jaeseok Kim received the B.S. degree in electronic engineering from Yonsei University, Seoul, Korea in 1977, M.S. degree from KAIST, Korea in 1979, and Ph.D. degree in EE from RPI, NY, USA in 1988. From 1988 to 1993, he was a Member of Technical Staff at the AT&T Bell Labs., Murray Hill, NJ, USA. In 1992, He received an "excellence of quality" award from AT&T Bell Labs. From 1993 to 1996, He was director of VLSI Architecture Design Lab. of ETRI which is a government-funded research institute in Korea. He is currently a professor of the electrical and electronic engineering department at Yonsei University, Seoul, Korea, and also serves as director of IT SoC Research Center which is funded by Korea government and industries.

He was the best research achievement professor of year 2006 at Yonsei University and received the best brain award in Korea semiconductor technology area in 2005. He served as general chairman of ISOCC (International SoC design conference) in 2006 and as organizing committee chair of ICEIC (International conference of electronics, information, and communication) in 2008. He also served as vice-chairman of IEEK (Institute of Electronics Engineers of Korea) in 2008 & 2009.

He has published 79 journal papers, 73 international conference proceedings, and 95 Korea domestic conference proceedings with publications of five text books in electrical engineering area. He holds 24 patents and has transferred 3 patents to eight companies during last five years.

His current research interests include modem SoC design for wireless communication systems (WLAN, WPAN, 4G), high performance Multimedia codec (H.264, NGVC) design, e-health SoC design, and SoC platform architecture.

Yusuf Leblebici (yusuf.leblebici@epfl.ch):

Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland

Lecture #1 Subthreshold Source-Coupled Circuit Design for Ultra-Low Power

In this talk, a novel approach is presented for implementing ultra-low-power digital and mixed-signal components and systems using source-coupled logic (SCL) circuit topology, operating in weak inversion (subthreshold) regime. Minimum size pMOS transistors with shorted drain-substrate contacts are used as gate-controlled, very high resistivity load devices. Based on the proposed approach, the power consumption and the operation frequency of logic circuits can be scaled down linearly by changing the tail bias current of SCL gates over a very wide range spanning several orders of magnitude, which is not achievable in subthreshold CMOS circuits. Measurements in conventional digital technologies show that the tail bias current of each gate can be set as low as 10 pA, with a supply voltage of 300 mV, resulting in a power-delay product of less than 1 fJ (Femto-Joule) per gate. Complex digital blocks such as parallel / pipelined adders and multipliers designed by using the STSCL topology will be presented – as well as some examples of mixed-signal blocks, e.g. ultra-low power A/D converters. The presented circuit techniques offer the possibility of operating in the extreme-low-power.

Speaker's biography: Yusuf Leblebici received his Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign (UIUC) in 1990. Between 1991 and 2001, he worked as a faculty member at UIUC, at Istanbul Technical University, and at Worcester Polytechnic Institute (WPI) – where he established and directed the VLSI Design Laboratory. Since 2002, Dr. Leblebici has been a Chair Professor at the Swiss Federal Institute of Technology in Lausanne (EPFL), and director of Microelectronic Systems Laboratory. He is a coauthor of 4 textbooks, namely, "Hot-Carrier Reliability of MOS VLSI Circuits" (Kluwer Academic Publishers, 1993), "CMOS Digital Integrated Circuits: Analysis and Design" (McGraw Hill, 1st Edition 1996, 2nd Edition 1998, 3rd Edition 2002), "CMOS Multichannel Single-Chip Receivers for

Multi-Gigabit Optical Data Communications” (Springer, 2007) and “Fundamentals of High-Frequency CMOS Analog Integrated Circuits” (Cambridge University Press, 2009), as well as more than 150 articles published in various journals and conferences.

Yiannos Manoli(ymanoli@imtek.uni-freiburg.de):

University of Freiburg IMTEK, Freiburg, Germany

Lecture #1: Energy Harvesting – from Devices to Systems

Energy harvesting (also known as power harvesting or energy scavenging) is the process by which energy is derived from external sources (e.g., solar power, thermal energy, wind energy, salinity gradients, and kinetic energy), captured, and stored. Frequently, this term is applied when speaking about small, wireless autonomous devices, like those used in wearable electronics and wireless sensor networks. (<http://www.wikipedia.org>) The talk covers both the transducer concepts and devices used to convert ambient energy into electrical power and also the circuits required to drive these components at the right operating point to achieve a high efficiency. The introduction explores the applications and systems where energy harvesting can be applied to power autonomous devices with functions such as readout of remote sensors, observation of the environment, surveillance of buildings and industrial plants. Some systems convert kinetic energy from motions and vibrations by using piezoelectric, electrostatic and electromagnetic concepts. The result is an AC output power. Electrostatic or capacitive harvesting is based on the effect that vibrations separate the plates of a variable capacitor, thus converting mechanical into electrical energy. Mechanical strain on piezoelectric devices can generate electrical current or voltage and vibrating magnets moving past a coil can be used to gather electrical power. Other concepts use electrochemical, photovoltaic or thermoelectric concepts to provide a DC energy source using fuel cells, light radiation or heat gradients. Thermoelectric generators, for example, are built up as a junction of two different materials. By connecting many devices in series a usable voltage can be achieved at the presence of thermal gradients. These power sources deliver low levels of usable energy, thus any system will have to seek ways to maximize the effectiveness. So diverse the energy sources are, even more wide ranging are the transduction principles that can be applied to convert the available energy to electrical power. Each one of these schemes will require a different circuit technique for achieving an optimal conversion. This adaptive control has to be intelligent enough to always find the optimum without itself requiring too large amounts of energy. Here lies a major challenge for low-power and low voltage electronics.

Speaker’s biography: Yiannos Manoli received the B.A. degree (summa cum laude) in physics and mathematics from Lawrence University in Appleton, Wisconsin, in 1978, the M.S. degree in electrical engineering and computer science from the University of California, Berkeley, in 1980, and the Dr.-Ing. Degree in electrical engineering from the Gerhard Mercator University in Duisburg, Germany, in 1987. In 1985, he joined the newly founded Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany. From 1996 to 2001, he held the Chair of Microelectronics as full professor with the Department of Electrical Engineering, University of Saarland, Saarbrücken, Germany. In July 2001, he was appointed Chair of Microelectronics, Department of Microsystems Engineering (IMTEK), University of Freiburg, Germany. Since May 2005, he also serves as one of the three directors at the “Institute of Micro and Information Technology” of the “Hahn-Schickard Gesellschaft” (HSG-IMIT), Villingen-Schwenningen, Germany. His current research interests are the design of low-voltage/low-power mixed-signal CMOS circuits, electronics for energy harvesting and embedded microsystems, sensor read-out circuits as well as A/D-converters. In 2000, he had the opportunity to spend half a year on a research project with Motorola (now Freescale) in Phoenix, AZ. In 2006, he spent his sabbatical semester with Intel, Santa Clara, CA. Prof. Manoli received the Best Paper Award from the European Solid-State Circuits Conference (ESSCIRC 1988) for the paper “A Self-Calibration Method for Fast High-Resolution A/D and D/A Converters.” His group has received awards at PowerMEMS 2006, at MWSCAS 2007, and at the IEEE International Conference on Microelectronic Systems Education (MSE-2007). The last award was dedicated to Spicy VOLTsim (www.imtek.de/svs) a web-based application for the animation and visualization of analog circuits which also received the Multi-Media-Award of the University of Freiburg in 2005. When the Technical Faculty introduced the Best Teaching Award in 2008 Professor Manoli was the first to receive this honor. Professor Manoli has served on the committees of a number of conferences such as ISSCC, ESSCIRC, DATE and ICCD, and was Program Chair (2001) and General Chair (2002) of the IEEE International Conference on Computer Design (ICCD). He is a member of Mortar Board, Phi Beta Kappa, IEEE, VDE and of the Editorial Board of the “Journal of Low Power Electronics”

Pramod Kumar Meher(pkmeher@i2r.a-star.edu.sg):

Embedded Systems Department, Institute for Infocomm Research, Singapore

Lecture #1:: Memory-Based Computing Systems for DSP Application

Semiconductor memory has become progressively cheaper, faster and more power-efficient. Transistor packing density for SRAM is higher, and increasing faster than that of logic devices. Specialized memories are developed to meet the needs of application environments, and integrated with logic devices. The integration of RAM and ROM with logic elements allows them to be used as lookup-table (LUT) that functions either as a part or whole of an arithmetic unit or to replace the time and power-consuming combinational blocks. Memory-based structures are more regular compared to logic elements, and have many other advantages. They have significant potential to satisfy the conflicting challenges of emerging wireless systems, e.g., low-power consumption, high computational-bandwidth for multimedia communication, and reconfigurability for seamless communication across the globe. Memory-based functional units are faster because they usually perform their functions through LUT access followed by a few additions. They consume less dynamic power due to less bit-switching. Moreover, if they are implemented by RAMs, they can be easily reconfigurable. Memory-based structures are well-suited for DSP algorithms, which often involve multiplications with a fixed set of coefficients, and generation of non-linear functions.

With a brief introduction to the key developments in memory technology, this lecture will cover the techniques for optimization of LUT-size, along with minimization of overall area-delay product and energy-consumption. It will cover the LUT addressing schemes, bit-level optimization, and word-level optimization techniques like odd-multiple storage, input coding, and antisymmetric output coding techniques for LUT multipliers, along with high-precision LUT-based multiplication, proposed recently by the nominee. It will present a brief note on combining LUT-based approach with multiple constant multiplications methods. Besides, it will cover the recent work on algorithms and architectures involving memory-based implementation of FIR filter and various orthogonal transforms proposed by the nominee and other researchers. It will also cover the state of the art of memory-based systems for generation of sinusoidal functions, evaluation of logarithms and anti-logarithms, estimation of hyperbolic tangent, squaring and square-root, etc. The list of the work of the nominee related to this topic is available at <http://www1.i2r.a-star.edu.sg/~pkmeher/>

Lecture #2: Algorithm-Architecture Co-Design for DSP Application

Over the years as the digital signal processing (DSP) functionalities are subjected to more demanding and stringent specifications, a lot of hardware-friendly algorithms and architectures have been proposed for their implementation. The recent trend in heterogeneous system design and emerging 3-D chips, however, has presented new opportunities and challenges, which necessitate the tailoring of algorithms to different platforms. Accordingly, attention is directed to platform-specific algorithm design, along with the partitioning and distribution of problem among those platforms and the layers of 3-D circuits. There are also initiatives on algorithm-architecture co-design, considering the choice of platforms and 3-D models, while taking the severity of constraints and requirements of deployment-environment into account.

This lecture will begin with observations on conflicting behavior of design constraints and the current trend in microelectronics. It will highlight the impact of interconnect-delay in nanostructure system design and the scope of 3-D solutions. It will also show the impact of increasing leakage current and the need of a decision of right operating voltage to minimize the energy consumption. It will briefly discuss various attributes of algorithm, e.g., sequential/parallel, localized/distributed, compute/communication-bound, locally/globally-recursive or non-recursive, etc., and the algorithm design for 3-D architectures with different processing units in different layers, which might be optimized in terms of memory, register files, I/O, interconnects, control, and arithmetic circuits.

Co-design will be viewed as a multidimensional optimization problem for a given specification of throughput, latency, chip-area and energy-consumption for the desired implementation solution, most likely a heterogeneous combination of DSP, FPGA and ASIC, where the performance of hardware depends heavily on the algorithm as well as the implementation platforms. The lecture will show examples of iterative algorithm-architecture co-design where the algorithm design and partitioning could be modified and architecture could be co-optimized hierarchically down to arithmetic circuits and combinational logic from different macro-blocks of functional units and from system level optimization. It will show some example architectures proposed the presenter and other researchers on algorithm-architecture co-design for communication and video processing applications.

Speaker's biography: Pramod Kumar Meher received the B.Sc. and M.Sc. degrees in Physics from Sambalpur University,

Sambalpur, India, in 1976 and 1978, respectively. He was awarded with the Ph.D. degree by the same university in 1996 for his work on VLSI signal processing.

He has a wide scientific and technical background covering Physics, Electronics, and Computer Engineering. Currently, he is working as a Senior Scientist with the Institute for Infocomm Research, Singapore and Adjunct Associate Professor in the School of Computer Engineering in Nanyang Technological University, Singapore. Prior to this assignment he was a visiting faculty with the School of Computer Engineering, Nanyang Technological University, Singapore. He was a Professor of Computer Applications with Utkal University, Bhubaneswar, India, from 1997 to 2002, a Reader in Electronics with Berhampur University, Berhampur, India, from 1993 to 1997, and a Lecturer in Physics with various Government Colleges in India from 1981 to 1993.

His research interest includes design of dedicated and reconfigurable architectures for computation-intensive algorithms pertaining to signal processing, image processing, communication, bio-informatics, and intelligent computing. He has published two book chapters and nearly 150 technical papers in various reputed journals and conference proceedings. Besides, he has delivered invited lectures in many universities in UK, Australia, Taiwan, and India.

Currently, he is serving as member of editorial board of IEEE Transactions on Circuits and Systems-II: Express Briefs, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, and Journal of Circuits, Systems, and Signal Processing as associate editor. Dr. Meher is a Senior Member of IEEE, a Fellow of the Institution of Engineering and Technology (IET, UK), and a Fellow of the Institution of Electronics and Telecommunication Engineers (IETE), India. He was the recipient of the Samanta Chandrasekhar Award for excellence in research in engineering and technology for the year 1999.

Antonio Petraglia (Antonio@pads.ufrj.br)

Federal University of Rio de Janeiro, Rio de Janeiro, Brazil

Lecture #1: Analog Multirate Signal Processing and IC Implementaion

Multirate digital signal processing techniques were introduced in the 70's to appropriately accommodate different signal sampling rates to bandwidth variations along the signal path. The basic technique has also been applied to other signal processing approaches, such as charge-coupled devices, switched-currents and switched-capacitors, which are also discrete in time, but the signal amplitudes are represented in analog form, leading to the development of analog multirate signal processing techniques.

Fueled in part by the advances in integrated circuit fabrication processes, allowing mixed analog-digital systems to co-exist in monolithic realizations, and in part by the development of modern telecommunication systems, alternative schemes have been proposed to combine the benefits of both digital and analog multirate signal processing, to achieve high efficiency in silicon and power consumption by reducing spread in device dimensions and relaxing amplifier settling time. Applications include decimation filters to effectively sample analog signals and alleviate A/D converter specifications, interpolation filters to improve resolution in D/A conversion, time-interleaved A/D converters and the generalization of its concept by using hybrid filter banks. The lecture begins with a review of basic concepts of mixed analog-digital multirate systems and signals. Then practical issues and multirate design solutions are addressed. A design example, from the project specifications to device dimensioning, is discussed to illustrate important tradeoff considerations. A view of the state of the art is also provided by a study of specific design techniques reflecting the most recent advances in the area.

Lecture #2: Automatic Placement of Capacitor Arrays and Embedded Measurement of Capacitance Matching

Capacitance matching is a critical issue in several analog and mixed-signal designs such as switched-capacitor filters, A/D and D/A converters. The use of identical unit capacitors in parallel to implement each capacitor in the design, combined with a careful layout, is the best technique to achieve a good capacitance matching. Common-centroid geometry is the most widely employed layout technique for matching capacitors, because this placement improves the immunity against process gradients. However, not yet well-known by IC designers, the common centroid geometry is not the only possible placement that has this feature. In fact, other placements can be found, which are not only immune to process gradients, but also able to meet other requirements, such as compactness and simplicity of routing interconnections. Moreover, these geometries are suitable alternatives for layouts whose number of unit capacitors does not allow a perfect common-centroid placement. Since finding such layouts is a very difficult task, automated methods that enable designers to achieve the optimal placement for arrays of unit capacitors is a useful design tool.

The lecture starts with considerations on the conditions capacitor arrays of unit capacitances must satisfy to be insensitive to process gradients, and minimize the overall variance of all unit capacitance averages. Then an automated approach that finds placements of such capacitor arrays is addressed. Design examples are carried out to illustrate the technique. Finally, an embedded circuit design technique for accurate measurements of on-chip capacitance ratios, from which the matching properties of capacitor arrays can be verified in the laboratory, is presented.

Speaker's biography: Antonio Petraglia (S'89–M'91–SM'99) received the Engineer and M. Sc. degrees from the Federal University of Rio de Janeiro (UFRJ), Brazil, in 1977 and 1982, respectively, and the PhD degree from the University of California, Santa Barbara (UCSB), in 1991, all in electrical engineering. In 1979, he joined the Faculty of UFRJ as an Associate Professor of electrical engineering, where he served as a Co-Chair in the Department of Electronic Engineering from 1982 to 1984. During the second semester of 1991, he was a post-Doctoral researcher with the Department of Electrical and Computer Engineering at UCSB. From March 2001 through March 2002 he was a Visiting Scholar with the Electrical Engineering Department at the University of California, Los Angeles. He served as an Associate Editor for the IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing in 2002-2003 and the Analog Integrated Circuits and Signal Processing in 2007-2008. He is currently serving as an Associate Editor for the Circuits, Systems and Signal Processing Journal. Dr. Petraglia's teaching and research activities lie in the areas of analog and digital signal processing and integrated circuit design. He has been involved in the design of multirate mixed-signal processing, hybrid filter banks and automated layout design techniques for analog integrated circuits. He is co-author of several journal and conference papers on these subjects.

Ruchir Puri (ruchir@us.ibm.com):

Lecture #1: Will 22nm be our catch 22! Design and CAD Challenges

With the impact of cost crunch in every industry including semi-conductor industry across the world, complexities of 22nm CMOS may appear to be way out in the distance future. However, more than the technology complexity, the new era of financial restraint will impose unprecedented productivity requirements on future design flows. This presents a significant opportunity as well as a complex challenge for the EDA industry. In addition, with semiconductor industry's march towards 32nm CMOS technology and introduction of new technologies such as 3D ICs in sight for 22nm nodes, it is crucial for the IC design and CAD community to understand the challenges posed by these potential technology changes. This talk will cover these challenges and outline the opportunities including those in physical design domain. The advanced device and interconnect structures and materials including 3D technology that could be introduced at 22nm node have significant impact on the direction of the CAD industry. We will also discuss the design methodology and CAD implications of these technology changes.

Lecture #2: From "Custom" Mars to "Synthesis" Venus: Visions

Due to ever increasing cost of doing design, design productivity and more specifically, cost of design has become a major bottleneck in large scale design projects. Due to the cost crunch, automated synthesis techniques have been gaining ground on manual and cost intensive (although potentially yielding higher quality of results) custom techniques. The push towards system level performance with multiple lower performance cores as opposed to single high performance core is also making the pursuit of frequency at any cost meaningless. Synthesis vs Custom has traditionally been a lively debate in microprocessor companies but now it is becoming more widespread with the desire of fabless companies to more fully utilize the technology node in order to compete with IDMs by utilizing more custom techniques. Custom hotshots argue that we cannot afford to leave performance or power on table when you are spending 3billion \$s in fabs. Industry needs to get maximum benefits possible. Synthesis fanatics will argue that designers should get over the last few ps and last few nW, as time to market, cost, and system performance are the new drivers and synthesis can not only meet the challenge but beat it many times with lower power solutions. This debate, the related issues and a vision of the future will be presented in this lively talk.

Speaker's biography: Ruchir Puri is Manager of the Logic and Physical Synthesis group at the IBM T J Watson Research Center which he joined in 1995. He has been responsible for logic and physical synthesis strategy for IBM's high performance designs and microprocessors and has received several IBM outstanding accomplishment awards and corporate recognitions for his research. He received the Ph.D. degree in computer engineering from University of Alberta, Canada in

1994 and a degree in electrical engineering from Indian Institute of Technology (IIT), Kanpur, India in 1990. Dr. Puri received 1993 ACM/IEEE Design Automation Scholarship and the 1992 and 1993 Alberta Microelectronics research scholarships for his doctoral research. He has also been an adjunct assistant professor in the Department of Electrical Engineering at Columbia University, New York where he taught VLSI design and Circuits. He has served on program committees as committee chair and member of most major VLSI Design Automation conferences, NSF and SRC panels and has been an invited speaker at numerous conferences such as ISSCC, DAC, and ICCAD. He is the inventor of over 30 U.S. patents and has authored over 90 publications on the design and synthesis of low-power and high-performance circuits. He has been an Associate Editor of IEEE Transactions on Circuits and Systems I, as well as IEEE Transactions on Circuits and Systems II. He serves on ACM SIGDA Physical Design Technical committee as well as Logic Synthesis Subcommittee. Ruchir was elected an IEEE Fellow in 2006 for contributions to automated logic and physical design of electronic circuits. He is an ACM Distinguished speaker and was recently elected to IBM Academy of Technology, a select group of IBM leading technologists.

Hanspeter Schmid (hanspeter.schmid@fhnw.ch):

Institute of Microelectronics (IME), University of Applied Sciences Northwestern Switzerland (FHNW), Windisch, Switzerland

Lecture #1: The Current-Mode Story

When Barrie Gilbert coined the term “current mode”, he did not envision that this would spawn a complete field of study that would try to separate itself from traditional circuit design.

In this talk, I show what current mode is and how the research concepts of current mode have led to very successful circuits: for example to current-feedback OpAmps (which are still extensively used as line-driver circuits for xDSL modems), techniques for building very fast Gm-C filters, or log-domain circuits. The audience will receive an introduction into the field and hear about advantages and disadvantages of doing circuits and systems “the current-mode way”.

Then I tell the story about how the current-mode world developed, how research groups separated from the main stream, how numerous writers managed to broadcast rationally unfounded [sic!] technical statements for years, and then how the community all but disappeared. The point of all this is not to show how bad the current-mode idea was: for this is exactly the way all research ideas develop. I will use it as an example to introduce Ludwik Fleck’s captivating theory of thinking styles and thinking constraints to the audience.

Lecture #2: Electrical and Human feedback

In this talk, I will give a technical introduction into feedback systems and into advantages and disadvantages of feedback. I will argue that if any electrical feedback is made in a system, then two other systems will also be connected in a feedback loop: the system of all engineers working together in that project, and the system of the designer interacting with all design tools used in the project’s tool chain.

The first example mainly shows the technical side of this: the design of an output driver for a micro-electrode array chip (the full-chip design was done by Simon Neukom and Yue-Li Schrag, CSEM Zürich) where the circuit was built on purpose with as little feedback as possible in order to get sufficient results in minimum time. This made it possible to do the electrical design to specifications of a sixteen-channel output block (including Monte-Carlo and corner simulations of noise, dynamic offset, harmonic distortion, crosstalk and settling behaviour) and the layout within ten working days, and doing it so successfully that the circuit worked first time right, and could be used with very few modifications on three different ASICs, and be ported with low effort to a different technology for a fourth one.

The second example mainly discusses the socio-psychological side of feedback: we look at the development of a sigma-delta sensor system, and how the electrical feedback caused feedback through the three design teams involved, how this loop became unstable, and through what measures it could be stabilized. Essentially, I will argue that excessive loop delay destabilizes both a sigma-delta system and a distributed team, and I will talk about how mutual trust can be built up and maintained in a distributed team.

Speaker's biography: Hanspeter Schmid received the diploma in electrical engineering in 1994, the post-graduate degree in information technologies in 1999, and the degree Doctor of Technical Sciences in 2000, all from the Swiss Federal Institute of Technology (ETH Zürich), Switzerland.

He joined the Signal and Information Processing Laboratory of the ETH Zürich as a teaching assistant in 1994 and became a research assistant and junior lecturer in the field of analogue integrated filters. During this time, he also studied some Philosophy of Science.

From 2000-2005, he was an analog-IC designer with Bernafon AG, Switzerland, where he was part of a design team who developed a new IC platform for hearing aids. In this team, he mainly worked on audio low-noise amplifiers, voltage regulators, and a wireless transceiver, and he was also responsible for full-system signal integrity.

Now he is a Research Fellow at the Institute of Microelectronics of the University of Applied Sciences Northwestern Switzerland (IME/FHNW) and a senior lecturer at ETH Zürich (Analog Signal Processing and Filtering). His main research interests are fast low-power circuits (mainly for sensor electronics), signal integrity in analog signal processing, sigma-delta conversion and mixed-analog-digital signal processing. He also does consulting in industry projects.

In addition to performing technical work, he has done training in conflict management and communication, occasionally works as a conflict moderator or facilitator, and he gives communication courses and conflict prevention courses for engineers and for laymen.

Hanspeter Schmid was Analog Signal Processing Technical Committee Co-Chair from 2008-2010; he currently is an Associate Editor of TCAS-I and a member of the ESSCIRC technical committee.

Wee Ser (ewser@ntu.edu.sg):

Nanyang Technological University, Singapore

Lecture #1: Wearable Respiratory Monitoring: Algorithms and System Design

More than 15% of the population suffers from some forms of respiratory disorders (e.g. Asthma, Bronchitis, Sleep Apnea, etc.) and some of such disorders can be acute. Currently, physicians perform such diagnosis by listening to lung sound using a stethoscope. The problem of this existing approach is that, the history of occurrence is important and yet patients' descriptions are often erroneous. Furthermore, auscultation with stethoscope is subjective and cannot be used for long-duration monitoring too. The emerging trend is therefore to monitor respiratory disorders in a home setting through the use of a wearable system. This lecture will focus on presenting the findings generated from a joint research program undertaken by the lecturer and his engineering team at NTU and the physicians at the National University Hospital (Singapore). In particular, the monitoring of two types of respiratory disorders: wheeze based (e.g. Asthma) and snore based (e.g. Sleep Apnea disorder) will be discussed. In addition to presenting the typical characteristics of such signals, the lecture will also address the problems imposed by the wearable constraint and discuss the algorithms and system solutions to these problems. The development of algorithms and the associated circuits and systems has evolved through three generations of designs. The problems faced and the findings obtained for these designs will be shared at the lecture. A demonstration of the effectiveness of some of these techniques and designs will be given during the lecture too.

Lecture #1: Near-field Microphone Array: Algorithms and System Design

With an aging population, there is an increasing need for daily activity monitoring for the ages in a home setting. Some of the current solutions include employing care-takers to look after the ages at home or sending the ages to daycare centers. A technological approach is to put in place sensors and processing systems in the home so that the daily activity of the ages can be monitored automatically and alerts can be activated should any abnormalities occur. One key enabler to such monitoring need is sound based technology and microphone array is a promising alternative. This lecture presents the findings obtained from a research program funded on the design of microphone array systems for daily activity monitoring. In particular, the lecture will focus on the problems and designs associated with near-field microphone array algorithms and systems. It is well known that, as the array aperture becomes larger (e.g. using a large array system), the signal model will become more near-field. This near-field property can be exploited to enable the suppression of interferences and noise

arriving from the same direction. This is not possible when using conventional far-field based array system structure. The lecture will dwell in some details on the algorithms reported in two recent papers published in the IEEE TCAS I and II. The lecture will also describe the design of a large microphone array system built by the lecturer and his team, which is unique and probably the largest in the world. Some demonstration sound effects will be played during the lecture to illustrate the problems faced and the effectiveness of the design too.

Speaker's biography: Associate Professor Wee Ser received his B.Sc. (Hon) and Ph.D. degrees both in EEE from the Loughborough University, UK, in 1978 and 1982 respectively. He joined the Defence Science Organization (DSO) in 1982 and became Head of the Communications Research Division in 1993. In 1996, he was appointed Technological Advisor to the CEO of DSO National Laboratories. In 1997, he joined the Nanyang Technological University (NTU) and has since been appointed Director of the Centre for Signal Processing. Wee Ser is currently the associate editors for the IEEE Communications Letters and the Journal of Multidimensional Systems and Signal Processing (Springer). He is a senior IEEE member and a member of a TC in the IEEE Circuit and System Society. He has served in the RCM of ISCAS 2009 and ISCAS 2010, as Chair of the local IEEE Signal Processing Chapter, and in the local IEEE Communications Chapter. He has served as track chair of several international conferences and has served in the International Advisory Committee of an IEEE Signal Processing Workshop on DSP and as a panel chair of an International DAB Symposium. More recently, he was invited as a keynote speaker for ICSIPA'09 (IEEE Conference of Signal and Image Processing Applications). He has also served in several national advisory and technical committees. He is a board director of a public listed company and an honour advisor to the Seattle Technology. He has published about 120 research papers in refereed international journals and conferences. He holds six patents (including 4 US patents) and is a co-author of four book chapters. He is the Principal Investigator of several research projects (with about US\$2m of grants from the Ministry of Education, A*STAR, DSO National Laboratories, and the industries). He has been shortlisted for the EEE Teaching Excellence Award from 2007 to 2009. Wee Ser was a recipient of the Colombo Plan scholarship and the PSC postgraduate scholarship. He was awarded the IEE Prize during his studies in UK. While in DSO, he was a recipient of the prestigious Defence Technology (Individual) Prize 1991 and the DSO Excellent Award 1992. His research interests include microphone array research, wearable signal processing system design; integrated audio-video based monitoring system design, signal classification techniques, and channel estimation and equalization.

Fernando Silveira (silveira@fing.edu.uy):

Universidad de la República, Montevideo, Uruguay

Lecture #1: Intuitive and power optimized analog and RF CMOS design based on gm/ID and drain current density

This lecture addresses transistor level design of analog and RF CMOS circuits.

First, the design methodology based on the transconductance to current ratio (gm/ID) and the drain current density is reviewed [1,2,3]. It is shown the role of gm/ID ratio as a key variable with variation in a small range that allows to efficiently explore the MOS transistor design space in all regions of inversion (weak, moderate and strong) and to select the size and bias point, while considering the trade-offs regarding power – bandwidth – precision (matching, gain) – signal range and noise.

The result is a very didactical approach to CMOS analog and RF design that allows to minimize the trial and error iterations on the design by giving the designer a clear view on how to move in the design space. This quality made that the method has been adopted in various universities worldwide. The key relationship applied for the design (between gm/ID and current density) can be obtained from analytical models, simulation or measurements, making the approach particularly suitable for nanometer and non-standard technologies where an analytical model is complex or unavailable.

The lecture is illustrated with the design and power optimization of analog and RF circuits in technologies down to below 100nm channel length applying this method.

1. F. Silveira, D. Flandre, P.G.A. Jespers, "A gm/ID Based Methodology for the Design of CMOS Analog Circuits and its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA", IEEE Journal of Solid State Circuits, Vol. 31, No. 9, Sept. 1996, pp. 1314 – 1319.
2. F. Silveira, D. Flandre, Low Power Analog CMOS for Cardiac Pacemakers. Design and Optimization in Bulk and SOI Technologies. Kluwer Academic Publishers, The Kluwer International Series in Engineering and Computer Science, Boston, Dordrecht. 2004.

3. P.G.A. Jespers, "The gm/ID Methodology, A Sizing Tool for Low-voltage Analog CMOS Circuits", Springer 2010.

Lecture #2: Ultra low power analog integrated circuits for implantable medical devices

This lecture introduces the requirements and design techniques of ultra low power (ULP) analog CMOS integrated circuits, based on the framework of its application to implantable medical devices.

The talk has three parts. In the first part, the main characteristics and needs of implantable medical devices, particularly from the point of view of the analog circuit designer, are presented. The second part presents the field of ULP analog CMOS design by considering the aspects of device modeling, circuit design techniques and architectures. Finally, the last part, discusses perspectives in the fields of ULP analog CMOS and implantable medical devices.

Speaker's biography: Fernando Silveira (S'89- M'90- SM'03) received the Electrical Engineering degree from Universidad de la República, Uruguay in 1990 and the MSc. and PhD degree in Microelectronics from Université catholique de Louvain, Belgium in, respectively, 1995 and 2002. He is Professor at Universidad de la República, Uruguay. His research interests are in design of ultra low-power analog and RF integrated circuits and systems, in particular with biomedical application. In this field, he is co-author of one book and many technical articles and advised Masters and PhD thesis. He has acted as invited plenary speaker at various events, several of them which were sponsored by CASS, among others: EAMTA (Argentinian School of Micro-nanoelectronics, Technology and Applications) from 2006 to 2009 (in 2010 he is one of the General Chairs of this event); Ibersensors 2006, Uruguay; CAS Tour in Bahia Blanca, Argentina (2004) and in Lima, Peru (2005); TAISA 2003, Belgium; SIM 2002, Brazil and he presented a tutorial on "Design of Ultra Low Power Analog Integrated Circuits for Implantable Medical Devices" at the XVIII Symposium on Integrated Circuits and Systems Design, Florianópolis, Brasil, 2005. He has served as reviewer of the following journals and conferences: IEEE Transactions on Circuits and Systems I, IEEE Design and Test, Solid State Electronics, Journal of Integrated Circuits and Systems (Brazilian Microelectronics Society), Symposium on Integrated Circuits and Systems Design, Brasil (since 1997), Iberchip Workshop (since 2001), IEEE International Symposium on Circuits and Systems.

He has multiple industrial activities with CCC Medical Devices and NanoWattICs, including leading the design of an ASIC for implantable pacemakers, applied in industrial production and designing analog circuit modules for implantable devices for various companies worldwide (USA, Israel, Europe and Canada) that are part of medical devices which are currently under human clinical evaluation, mainly related to the cardiovascular and neural fields. Dr. Silveira is a member of the Technical Advisory Board of GTronix, Inc, USA and received the "Ingeniero Destacado" (Distinguished Engineer) award by the Uruguayan Association of Engineers in 2007.

Chi (Michael) K. Tse (encktse@polyu.edu.hk):
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Lecture #1: Applications of Complex Networks Research: From Science, Engineering, Arts to Finance

In the past decade, complex networks have attracted a great deal of attention from researchers across a variety of disciplines including mathematics, science, engineering and humanities. Certain classes of complex problems, arising from many different disciplines, have been analyzed from a networking viewpoint. The many discoveries that man-made and natural networks display a power-law degree distribution and small-world property have clearly indicated a high level of relevance of the study of complex networks with real-world applications.

Results generated from such network-based analyses often yield new insights into the basic structure of the system under study as well as the way in which the various subsystems interact. The basic foundation of the analysis is that the system can be broken down into a large number of basic units or subsystems which are interconnected with one another, and specifically, the way in which connections are distributed over the entire system plays an important role in determining the behavior of the whole system. The basic units or subsystems can be identical or different. Although a considerable amount of fundamental findings have been reported in complex networks, such as the general scale-free and small-world properties of networks arising from human interactions, man-made and natural networks, the progress of applying complex network analysis to practical problems is still relatively slow. In this talk we review a few interesting applications. Our purpose is to

show some possible pathways through which practical problems may be tackled from a network viewpoint, yielding entirely new insights into the problems.

A network is a collection of “nodes” connected by “links” or “edges”. For the purpose of this talk, we do not impose any restriction on the way a node should be defined. Basically, a node can be any basic element that can be identified in a system which is being considered as a network. Such basic nodes are usually very numerous in quantity and are interconnected via physical couplings or abstract connections. A simple example is a human community, where people can be regarded as nodes. If two persons know each other, we put a link connecting these two persons. Then, a network can be constructed for this community. In this network, nodes are people, and links are some sorts of relationship. The resulting network topology will depend on how we actually define the links. As another example, if we are studying the transmission of avian influenza among the birds in different cities or locations, we may consider a city or place as a node where outbreak of the disease occurs. We may then define a criterion for the purpose of connecting any two nodes. For instance, we put a link between two cities if outbreaks occur in these two cities within a certain distance in both space and time. Then, the resulting network represents a kind of “map” of transmission of the disease. Finally, consider a piece of music. Suppose we wish to construct a network for a given piece of music. We may define a node as a musical note and the way in which individual musical notes are connected together defines a particular piece of work. One straightforward way to define a link is co-occurrence, i.e., two musical notes are connected if they appear adjacent to each other. Thus, a music score can be represented by a network and we may study music in terms of the property of this network. We may further conceive that any complex system can be considered as a complex network by defining nodes and links appropriately. The number of links emerging from and converging at a node is called the “degree” of that node, usually denoted by k . So, we have an average degree for the whole network. The key concept here is the distribution of k . This concept can be mathematically presented in terms of probability density function. Basically, the probability of a node having a degree k is $p(k)$, and if we plot $p(k)$ against k , we get a distribution function. This distribution tells us about how this network of nodes are connected. For instance, if we see a normal distribution of $p(k)$ with mean k_m , that means most nodes are having an average degree k_m , some having less and some having more, following a Gaussian type of spread about k_m . Recent research has provided concrete evidence that networks with man-made couplings and/or human connections follow power-law distributions, i.e., $p(k)$ vs k being a straight line whose gradient is the characteristic exponent. Such networks are termed scalefree networks.

On the basis of the networks as models of complex systems, we present several examples of applications including telephone traffic analysis, coding, disease transmission dynamics, music composition and stock market fluctuation. Our purpose is to expose the network perspective of complex system analysis and its potential use in solving real-world problems.

Speaker’s biography: Chi K. Tse received the BEng degree with first class honors and the PhD degree from the University of Melbourne, Australia, in 1987 and 1991, respectively. He is a Fellow of IEEE and also a Fellow of the Institution of Engineers Australia.

He is presently Chair Professor of Electronic Engineering and Head of Department of Electronic and Information Engineering at the Hong Kong Polytechnic University, Hong Kong. His research interests include complex network applications, power electronics and nonlinear systems. He is the author of the books *Linear Circuit Analysis* (London: Addison-Wesley, 1998) and *Complex Behavior of Switching Power Converters* (Boca Raton: CRC Press, 2003), co-author of *Chaos-Based Digital Communication Systems* (Heidelberg: Springer-Verlag, 2003), *Digital Communications with Chaos* (London: Elsevier, 2006), *Reconstruction of Chaotic Signals with Applications to Chaos-Based Communications* (Singapore: World Scientific, 2007) and *Sliding Mode Control of Switching Power Converters: Techniques and Implementation* (Boca Raton: CRC Press), and co-holder of 3 US patents and 2 other pending US patents.

Prof. Tse received the L.R. East Prize from the Institution of Engineers, Australia, in 1987, the Best Paper Award from IEEE TRANSACTIONS ON POWER ELECTRONICS in 2001, Dynamics Days Europe Presentation Prize in 2002, and the Best Paper Award from International Journal of Circuit Theory and Applications in 2003. While with the Hong Kong Polytechnic University, he received the President’s Award for Achievements in Research in 1997 and 2000, the Faculty Best Researcher Award in 2000, the Faculty Research Grant Achievement Award in 2004, and a few other teaching awards. In 2005 he was named an IEEE Distinguished Lecturer. In 2007, he was awarded the Distinguished International Research Fellowship by the University of Calgary, Canada. In 2009, he and his co-inventors won the Gold Medal with Jury’s Commendation from the

International Exhibition of Inventions of Geneva, Switzerland, for a novel driving technique for LEDs. He has been appointed as Advisory/Guest Professor by a number of universities in China including Beijing Jiaotong University, Wuhan University, Northeastern University, etc. In 2010, he has been appointed by the Ministry of Education, China, as Chang Jiang Scholars Chair Professor (2009) at Huazhong University of Science and Technology, China.

Prof. Tse was/is an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART I — FUNDAMENTAL THEORY AND APPLICATIONS from 1999 to 2001 and again from 2007 to 2009. He has also been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 1999. Currently he also serves as Deputy Editor-in-Chief for the IEEE Circuits and Systems Magazine and Editor-in-Chief of IEEE Circuits and Systems Society Newsletter, and Associate Editor of the International Journal of Systems Science, and also on the Editorial Board of the International Journal of Circuit Theory and Applications and International Journal and Bifurcation and Chaos. He also served as Guest Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART I — FUNDAMENTAL THEORY AND APPLICATIONS in 2003, Guest Associate Editor for the IEICE Transactions on Fundamentals of Electronics, Communications and Computers in 2004–2006, and Guest Editor for Circuits, Systems and Signal Processing in 2005

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Lecture #1: Analysis of Internet Topologies

Discovering properties of the Internet topology is important for evaluating performance of various network protocols and applications. The discovery of power-laws and the application of spectral analysis to the Internet topology data indicate a complex behavior of the underlying network infrastructure that carries a variety of the Internet applications. In this paper, we present analysis of datasets collected from the Route Views project. The analysis of collected data shows certain historical trends in the development of the Internet topology. While values of various power-laws exponents have not substantially changed over the recent years, spectral analysis of the normalized Laplacian matrix of the associated graphs reveals notable changes in the clustering of Autonomous System (AS) nodes and their connectivity.

Lecture #1: Mining Network Traffic Data

Mining and statistical analysis of network data are often employed to determine traffic loads, analyze patterns of users behavior, and predict future network traffic. In this talk, we analyze traffic data collected from three deployed networks: a cellular wireless network used by public safety agencies (E-Comm), a satellite network used by Internet service providers (ChinaSat), and the Internet. We describe analysis of network log data collected from E-Comm, a public safety trunked radio network that utilizes circuit-switched cellular wireless technology. We examine statistical distributions and autocorrelation functions of call inter-arrival and call holding times during busy hours. Our findings indicate that traditional Erlang models used for voice traffic may not be suitable for evaluating the performance of trunked radio networks. We also describe collection of traffic data, characterization of traffic loads, and distribution of packet sizes in ChinaSat, a hybrid satellite-terrestrial system. We investigate long-range dependence as the traffic patterns vary, propose a traffic model for the Transmission Control Protocol (TCP) connections, and use data from billing records to predict future traffic loads. Since discovering network topology is important for analyzing routing protocols and network robustness and resilience, we also examine datasets from the Route Views and RIPE projects and identify important properties of Internet graphs. Our current traffic measurement project deals with traffic collection from BC.Net, the Vancouver Lower Mainland Gigabit Ethernet network. Data collected from BC.Net will be used to analyze behavior and performance of the Border Gateway Protocol (BGP).

Speaker's biography: LJILJANA TRAJKOVIC received the Dipl. Ing. degree from University of Pristina, Yugoslavia, in 1974, the M.Sc. degrees in electrical engineering and computer engineering from Syracuse University, Syracuse, NY, in 1979 and 1981, respectively, and the Ph.D. degree in electrical engineering from University of California at Los Angeles, in 1986. She is currently a Professor in the School of Engineering Science at Simon Fraser University, Burnaby, British Columbia, Canada. From 1995 to 1997, she was a National Science Foundation (NSF) Visiting Professor in the Electrical Engineering and Computer Sciences Department, University of California, Berkeley. She was a Research Scientist at Bell Communications Research, Morristown, NJ, from 1990 to 1997, and a Member of the Technical Staff at AT&T Bell Laboratories, Murray Hill,

NJ, from 1988 to 1990. Her research interests include high-performance communication networks, control of communication systems, computer-aided circuit analysis and design, and theory of nonlinear circuits and dynamical systems. Dr. Trajkovic served as 2007 President of the IEEE Circuits and Systems Society. She was a member of the Board of Governors of the IEEE Circuits and Systems Society (2001 – 2003 and 2004 – 2005). She serves as Vice President Long-Range Planning and Finance of the IEEE Systems, Man, and Cybernetics Society (2008-2009) and served as a Member at Large of its Board of Governors (2004-2006). She is Chair of the IEEE Circuits and Systems Society joint Chapter of the Vancouver/Victoria Sections. She was Chair of the IEEE Technical Committee on Nonlinear Circuits and Systems (1998). She was Technical Program Co-Chair of ISCAS 2005 and served as Technical Program Chair and Vice General Co-Chair of ISCAS 2004. She served as an Associate Editor of the IEEE Transactions on Circuits and Systems (Part I) (2004 – 2005 and 1993 – 1995), the IEEE Transactions on Circuits and Systems (Part II) (1999 – 2001 and 2002 – 2003), and the IEEE Circuits and Systems Magazine (2001 – 2003). She is a Fellow of the IEEE.

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Lecture #1: Reliability and Yield of MOS Devices and Circuits

With the shrinking below 100 nm, new phenomena starts playing a role on the reliability of MOS devices. As a consequence, performance and reliability become influenced also by factors other than physical dimensions. Circuits with minimum geometry transistors, as for instance memories, are usually the first ones to be affected. Variability and uncertainty in devices parameters and electrical behavior impose challenges on all levels of the design process, as well as on the overall system reliability. Furthermore, the variations of parameters over time (aging and transient effects such as noise and soft errors) may lead to dramatically increased overhead in the timing budget, as well as on test procedures. Sources that play a major role on the reliability of today digital and analog designs will be discussed, as well as sources that are expected to become relevant in future technologies. Among the sources discussed, the major ones are: – Parametric variability due to effects such as random dopant fluctuations and line edge roughness. – Aging effects such as Bias Temperature Instability (BTI), Hot Carrier Injection (HCI) and Time Dependent Dielectric Breakdown (TDDB). – Radiation Effects as Single Event Transients (SET) and Single Event Upsets (SEU). – Device intrinsic noise, with focus on the Random Telegraph Signal (RTS). Besides its importance for analog design, as a source of low-frequency noise, RTS is also becoming a concern in digital circuits, as for instance in SRAM and flash memories. RTS may be modeled as momentary changes in threshold voltage, meaning that circuit behavior may change between two logic operations of a digital circuit. Different modeling approaches will be discussed, focusing on operation conditions relevant for digital and analog design, including cyclo-stationary operation. Design techniques to improve yield and resilient computing techniques will also be addressed.

Speaker's biography: Gilson I. Wirth received the B.S.E.E and M.Sc. degrees from the Universidade Federal do Rio Grande do Sul, Brazil, in 1990 and 1994, respectively. In 1999 he received the Dr.-Ing. degree in Electrical Engineering from the University of Dortmund, Dortmund, Germany. He is currently a full professor at the Electrical Engineering Department at the Universidade Federal do Rio Grande do Sul – UFRGS (since January 2007). From 2000 to 2002 he worked as lecturer and researcher in the field of microelectronics at the Informatics Institute, Universidade Federal do Rio Grande do Sul (UFRGS). From July 2002 to December 2006 he was professor and head of the Computer Engineering Department, Universidade Estadual do Rio Grande do Sul (UERGS). He founded the research group in micro- and nano-electronics at UERGS. In July, August and December 2001 he was at Motorola, Austin, Texas, leading the team working in CMOS process technology transfer to CEITEC, Porto Alegre, Brazil. The technology transfer was funded by FAPERGS under grant number 01/1093.3 (first phase of technology transfer) and 01/1628.9 (second phase of technology transfer). In February and March 2002 he was at the Corporate Research Department of Infineon Technologies, Munich, Germany, working as guest researcher on low-frequency noise in deep submicron MOS devices. His research interests include low-frequency noise, radiation effects, variability and design for yield of digital, analog and mixed-signal circuits. An updated list of publication may be found at <http://lattes.cnpq.br/1745194055679908>.

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