Automatic Placement of Capacitor Arrays and Embedded Measurement of Capacitance Ratios

A. Petraglia
Universidade Federal do Rio de Janeiro
EPOLI/PEE/COPPE
If the capacitance ratios $C_2/C_1$, $C_3/C_1$, ..., $C_K/C_1$ are implemented with high accuracy, then $C_1$, $C_2$, ..., $C_K$ are very well matched.

Applications where Capacitance Matching is Critical:
- A/D and D/A Converters
- Switched-capacitor Filters

Sources of Capacitance Mismatch in CMOS IC’s:
- Process Gradients
- Random Errors

Successful Techniques used to Improve Capacitance Matching in CMOS:
- Identical Unit Capacitors are used in Parallel to Implement each Capacitor
- Unit Capacitors are Placed in Common Centroid Geometry
Introduction

• Example of a unit capacitor array:

\[
\begin{array}{cccccccc}
A & B & B & C & B & B & A \\
A & B & C & D & C & B & A \\
A & B & B & C & B & B & A \\
\end{array}
\]

\[C_A = 16C, \quad C_B = 14C, \quad C_C = 4C, \quad C_D = C\]
Introduction

• **Problems:**
  – Finding a placement with common centroid symmetry is not a simple task when the number of identical unit capacitors is large
  – A placement with a common centroid is not always possible
  – When possible, there are several different placements with common centroid symmetry

• **Objectives:**
  – Develop an Automatic Tool for Unit Capacitor Placement
  – Help the Layout Designer to find the best placement among several different possibilities
  – Find optimal placements when a common centroid arrangement is not possible
  – Verify experimentally capacitance matching in the arrays developed with the proposed method
Problem Presentation

- Capacitance ratios implemented with identical unit capacitors in parallel:

\[
\frac{C_A}{C_B} = \frac{\sum_{i=1}^{N} C_i}{\sum_{j=1}^{M} C_j} = \frac{N}{M} \cdot \frac{\frac{1}{N} \cdot \sum_{i=1}^{N} C_i}{\frac{1}{M} \cdot \sum_{j=1}^{M} C_j}
\]

- The optimal matching condition is:

\[
\frac{1}{N} \cdot \sum_{i=1}^{N} C_i = \frac{1}{M} \cdot \sum_{j=1}^{M} C_j
\]
Mismatch Caused by Process Gradients

- Computation of the average unit capacitance of each capacitor in the array using the linear process gradient model:

\[ C_{xy} = C + \alpha x + \beta y \]

\[
\begin{align*}
\langle C_{xy} \rangle_A &= \frac{1}{16} \cdot [16 C + 48 \alpha + 32 \beta] = C + 3 \alpha + 2 \beta \\
\langle C_{xy} \rangle_B &= \frac{1}{14} \cdot [14 C + 42 \alpha + 28 \beta] = C + 3 \alpha + 2 \beta \\
\langle C_{xy} \rangle_C &= \frac{1}{4} \cdot [4 C' + 12 \alpha + 8 \beta] = C' + 3 \alpha + 2 \beta \\
\langle C_{xy} \rangle_D &= C + 3 \alpha + 2 \beta
\end{align*}
\]
Mismatch Caused by Process Gradients

- Example of a placement without common centroid symmetry, but insensitive to process gradient:

\[
\langle C_{xy} \rangle_A = \frac{1}{16} \cdot [16C + 48\alpha + 32\beta] = C + 3\alpha + 2\beta
\]

\[
\langle C_{xy} \rangle_B = \frac{1}{14} \cdot [14C + 42\alpha + 28\beta] = C + 3\alpha + 2\beta
\]

\[
\langle C_{xy} \rangle_C = \frac{1}{4} \cdot [4C + 12\alpha + 8\beta] = C + 3\alpha + 2\beta
\]

\[
\langle C_{xy} \rangle_D = C + 3\alpha + 2\beta
\]
Mismatch Caused by Process Gradients

- How to find insensitive placements when the number of unit capacitors is too large?
Mismatch Caused by Random Errors

- **Variances:**
  \[ VAR \left[ \frac{1}{N} \cdot \sum_{i=1}^{N} C_i \right] = \frac{\sigma_A^2}{N}, \quad VAR \left[ \frac{1}{M} \cdot \sum_{j=1}^{M} C_j \right] = \frac{\sigma_B^2}{M} \]

- **Pelgrom’s Rule:**
  \[ \sigma^2 (C_{i,j}) = \frac{A_P^2}{WL} + S_P^2 D_x^2 \]

- **Conclusions:**
  - Unit capacitors close to each other in the layout will present lower variance than the ones placed far from each other.
  - If \( M > N \):
    - the unit capacitors belonging to \( C_A \) should be placed close to each other to decrease their variance.
    - the unit capacitors belonging to \( C_B \) can be placed far from each other because the larger \( M \) will compensate the increase in variance.
Optimal Placement

- Find the optimal placement of the unit capacitors belonging to capacitance ratios:

\[
\frac{C_2}{C_1}, \frac{C_3}{C_1}, \frac{C_4}{C_1}, \ldots, \frac{C_K}{C_1}
\]

- Using Constrained Simulated Annealing with the following cost function:

\[
F_C(L, \lambda) = f_c(L) + \lambda \cdot \mathcal{E}_M(L)
\]
Optimal Placement

• Cost function to be minimized:

\[ f_c(L) = \sum_{x=0}^{M-1} \sum_{y=0}^{N-1} M_{xy} \left[ (x - x_o)^2 + (y - y_o)^2 \right] \]

• Function inspired in the Inertia Momentum
  
  – \( x_o \) and \( y_o \) are the coordinates of the array center
  – \( M_{xy} \) is the “mass” of a unit capacitor
  – Unit capacitors that appear in smaller number are made “heavier” than unit capacitors that appear in larger number
  – Minimizing the Inertia Momentum places unit capacitors that appear in smaller number close to each other around the center of the array
Optimal Placement

- The constraint is the total error caused by process gradients (using the same linear model):

\[ \mathcal{E}_M(L) = \frac{1}{2(K-1)} \cdot \sum_{k=2}^{K} \left( \varepsilon_k|_{\alpha=0} + \varepsilon_k|_{\beta=0} \right) = 0 \]

- Where the error of each capacitance ratio caused by linear process gradients is:

\[ \varepsilon_k = \left| \frac{C_k/C_1 - \hat{C}_k/\hat{C}_1}{C_k/C_1} \right|, \; k = 2, 3, \ldots, K \]
Examples

• Example I:
  – Array where each capacitor is implemented with a prime number of unit capacitors in parallel
  – In this case, an arrangement with common centroid symmetry is not possible, but an insensitive placement was found

\[
\begin{array}{ccccccc}
1 & 1 & 1 & 2 & 2 & 1 & 1 \\
1 & 2 & 1 & 3 & 2 & 2 & 1 \\
1 & 2 & 4 & 3 & 4 & 2 & 1 \\
1 & 2 & 2 & 3 & 2 & 2 & 1 \\
1 & 2 & 2 & 1 & 1 & 1 & 1 \\
\end{array}
\]

\[C_1 = 17C\]
\[C_2 = 13C\]
\[C_3 = 3C\]
\[C_4 = 2C\]
Examples

- **Example II:**
  - In this example is not possible to find a placement with common centroid symmetry nor with insensitivity to linear process gradients
  - In this case, the error caused by linear gradients is minimized and the placement found has some symmetry

\[ C_1 = 16C \]
\[ C_2 = 12C \]
\[ C_3 = 4C \]
\[ C_i = C, \ i=4,\ldots,7 \]
Accurate estimate of the fabricated capacitance ratios can be obtained with the following discrete-time filter:

\[ F(z) = \frac{z^{-1} + a}{1 + az^{-1}} \]

where \( a = \frac{C_A}{C_B} \) is the capacitance ratio of interest.
The result is a third-order elliptic filter, whose notch frequency occurs at

$$\omega_n = \cos^{-1}\left(\frac{a - 1}{2a}\right)$$

Examples:
On-Chip Measurement of Capacitance Ratios

- Implementation of $F(z)$ by a structurally allpass filter, using a switched-capacitor technique:

$$F(z) = \frac{z^{-1} + C_A/C_B}{1 + (C_A/C_B)z^{-1}}$$
On-Chip Measurement of Capacitance Ratios

- Complete circuit:

\[ H(z) = \frac{1}{2} \left( \frac{z^{-2} + a}{1 + az^{-2}} + z^{-1} \right) \quad a = \frac{C_A}{C_B} \]

- It is necessary that \( a > 1/3 \), so that the transfer function zeros are imaginary
Observability Properties

• For large capacitance ratio values, the notch frequency becomes less sensitivity to variations of $C_A/C_B$: 

![Plot](image)
Effects of the Amplifier Finite Gain

- Sufficiently low operation frequency can be chosen to make amplifier finite bandwidth effects negligible.
- However, process variations tend to reduce the amplifier dc gain, which may influence the depth and frequency of the notch, and hence affect capacitance ratio measurements.
Circuit Layout

Process: 0.35 μm CMOS
Dimensions: 900mmx200mm
Unit Capacitance: 100 fF
Power Consumption: 18.1 mW
Switching Frequency: 1 MHz
Dinamic Range: 67.5 dB @ 100 kHz, 2Vpp
Monte Carlo Analysis

\[ C_A/C_B: 0.5 \]
\[ (C_A = 800 \text{ fF}; C_B = 1.6 \text{ pF}) \]

Gradients and mismatch effects on transmission zero (kHz):

Ideal: 333.50
Cadence – Verilog-A: 333.41
Cadence – Schematic: 333.50
Conclusions

- Using placements with common centroid symmetry is not the only way to improve capacitance matching against process variations;
- The proposed method was able to find placements insensitive to linear process gradients even when arrangements with common centroid symmetry are not possible;
- In cases where insensitive layouts are not possible, the proposed method finds the placement that minimizes the error caused by process gradients;
- A technique based on a switched-capacitor filters that allows accurate on-chip estimates of capacitance ratios was presented.