



Advanced Modeling and Simulation Strategies for Power Integrity in High-Speed Designs

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AGENDA

- **Introduction – Power Distribution Networks**
- **Power-Grid Modeling/Analysis Challenges**
- **Advanced Analysis Methods**
 - ➔ **Partitioning**
 - ➔ **Wave-form Relaxation**
 - ➔ **Initial-guess generation**
 - ➔ **Parallelization Schemes**
- **Numerical Results**
- **Conclusions**

Power Delivery System

A PDS consists of:

- **Voltage Regulator Modules (VRMs)**
 - **Decoupling or Bypass Capacitors on the PCB and packages**
 - **Printed Circuit Board (PCB) power planes**
 - **Package power planes**
 - **Chip power distributions**
- ➔ Most of the digital ICs require a PDS to deliver a voltage with a tolerance defined in datasheet.**

Power Integrity in High-Speed Designs

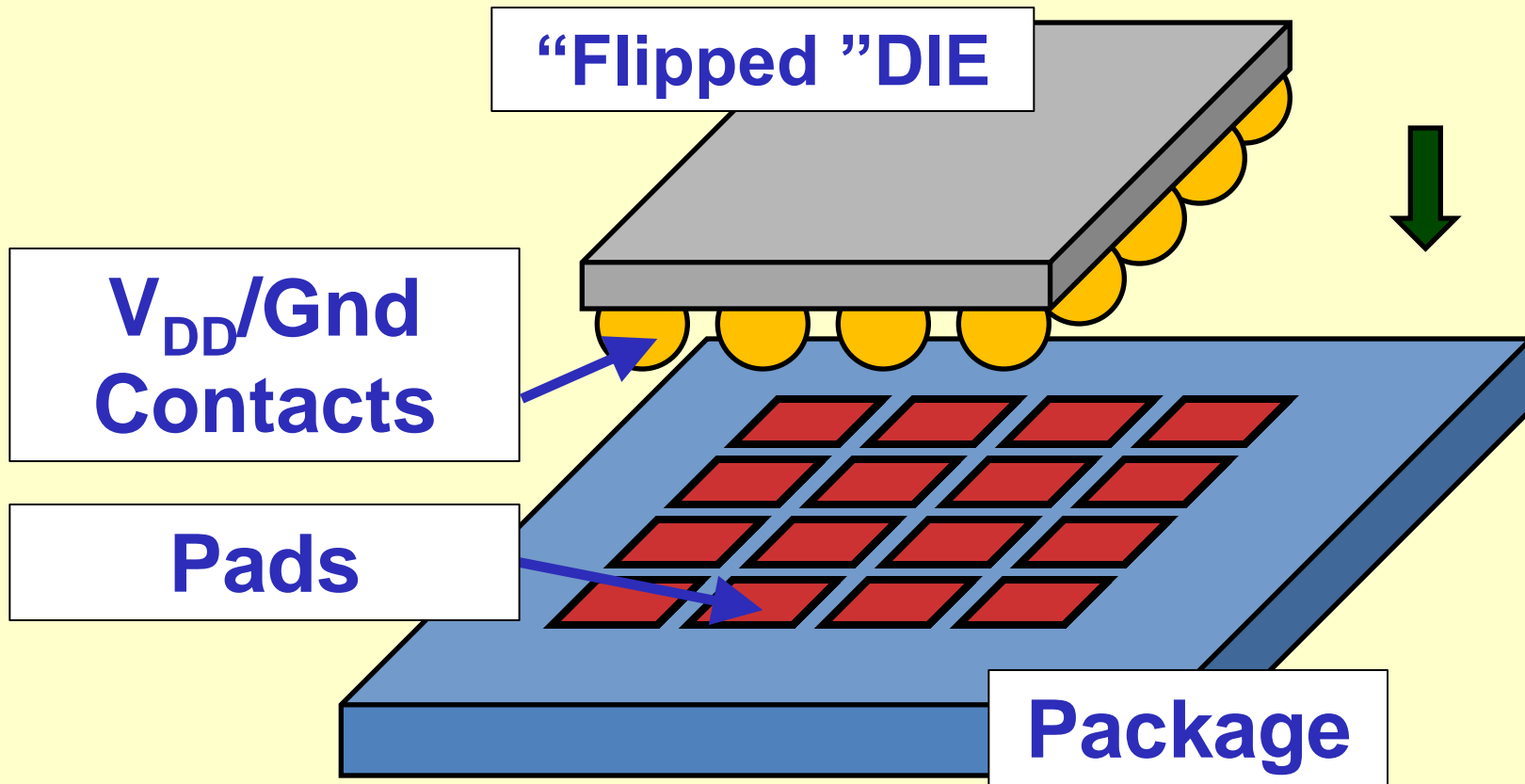
Trends

- **Decreasing Feature Size**
- **Increasing Frequency**
- **Mixed-domain integration (RF, optical, MEMs)**
- **Low Power**

Issues

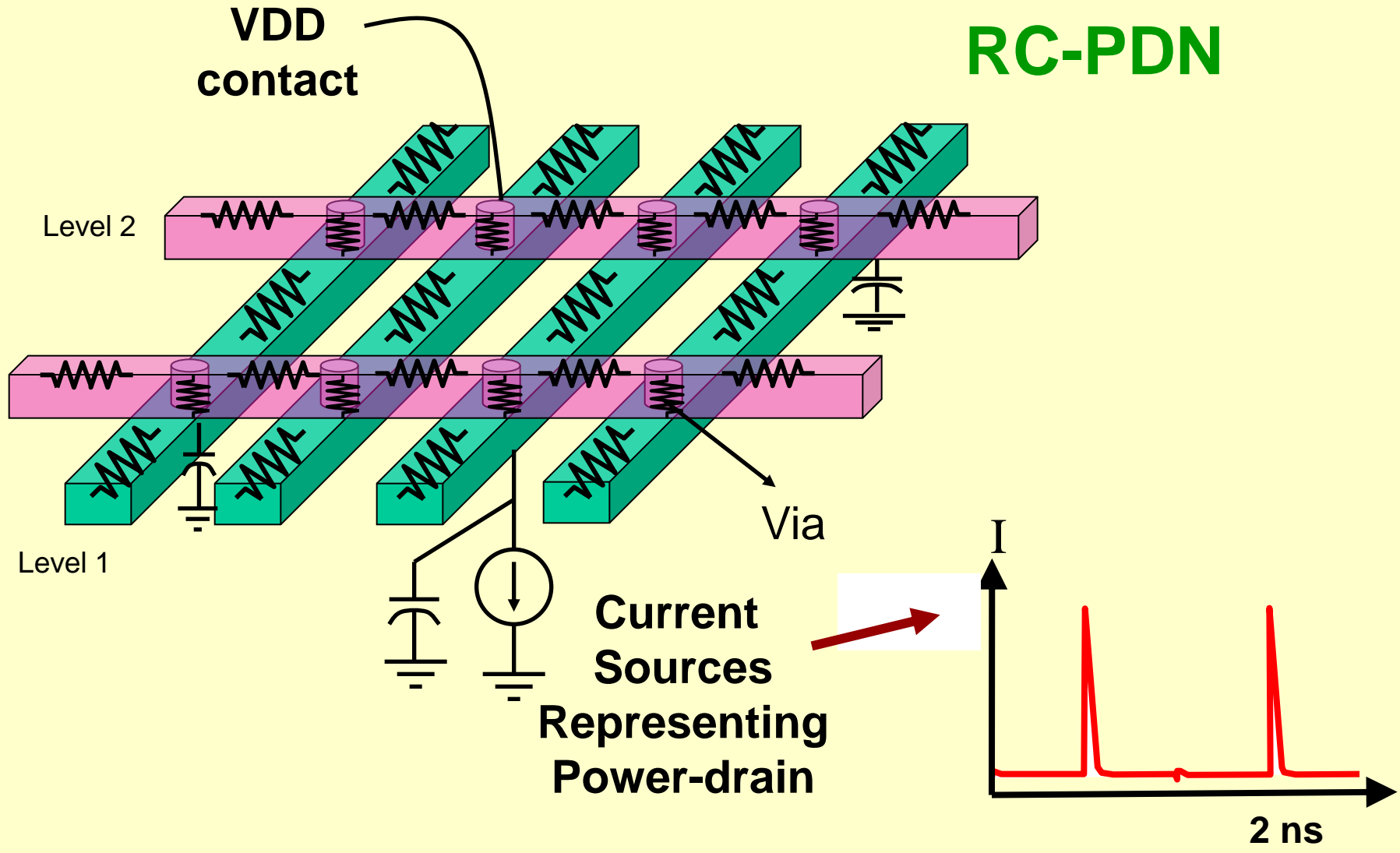
- **Increased sensitivity to Supply variations**
- **Reduced noise margins**
- **Timing errors, Failed Designs**

On-Chip PDNs: Flip Chip



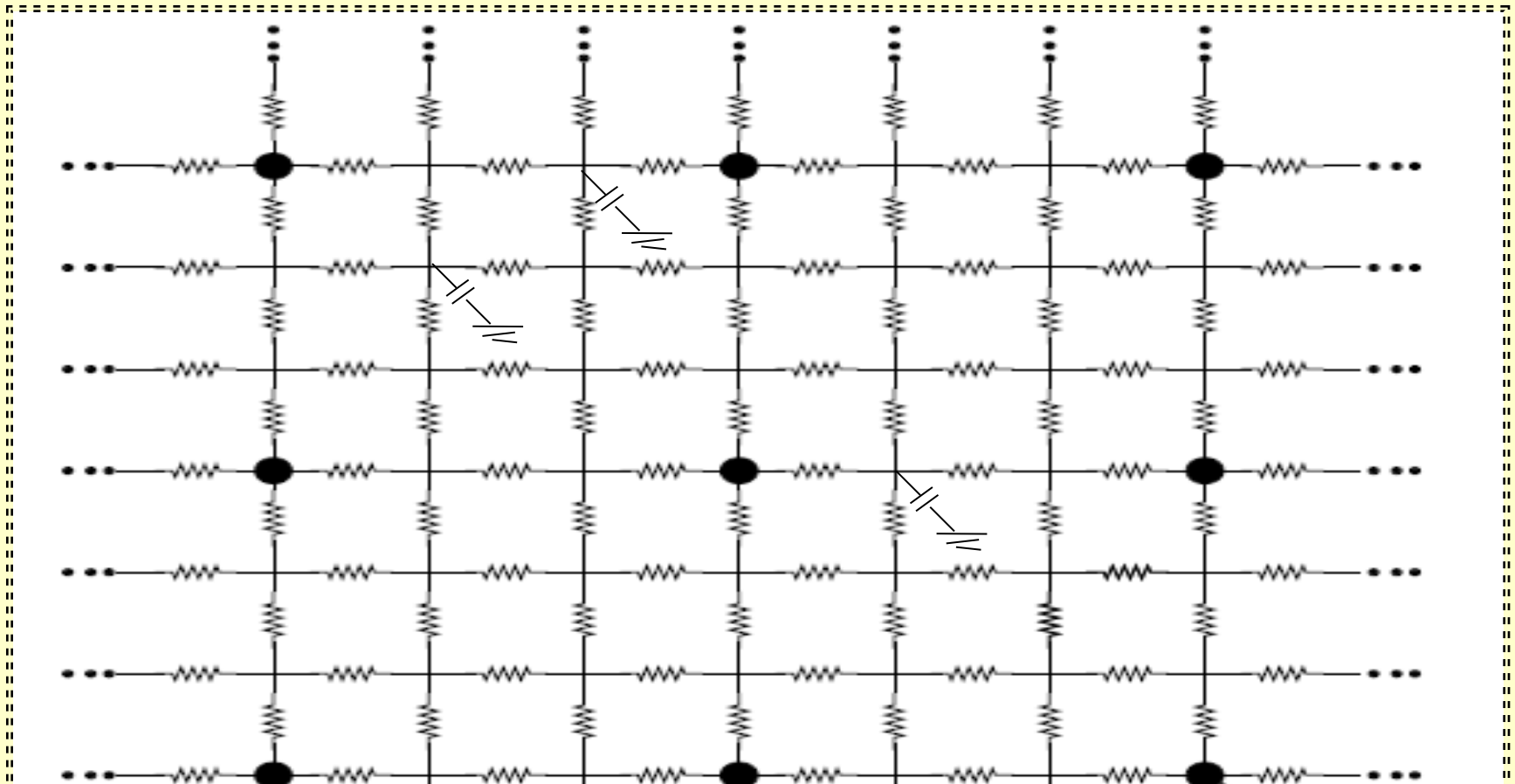
- **Uniform distribution of power**
- **Shorter contacts: reduced parasitics**
- **More widely used**

Flip Chip PDN: Modeling



Leakage + Switching Current

Flip Chip PDNs: “Large Power Grids”



- **Can contain millions of nodes!**
- **Existing solvers too slow or inaccurate**
- **Can't exploit the parallel platforms**

Power Grid Analysis: In the literature.....

Direct Methods

- **Multigrid** [Najm et. al., TCAD 2002]
- **Hierarchical** [Blaauw et. al., TCAD 2002]
- **MOR** [He et. al., DAC 2002]
- **and many more...**

Iterative Methods

- **Krylov-subspace** [Chen et. al., DAC 2001]
- **Successive Over-relaxation** [Wong et. al., ICCAD 2007]
- **Random Walks** [Nassif et. al., TCAD 2005]
- **and many more...**

In the literature.....

Direct Methods

→ Fast

~~→ Memory Inefficient~~

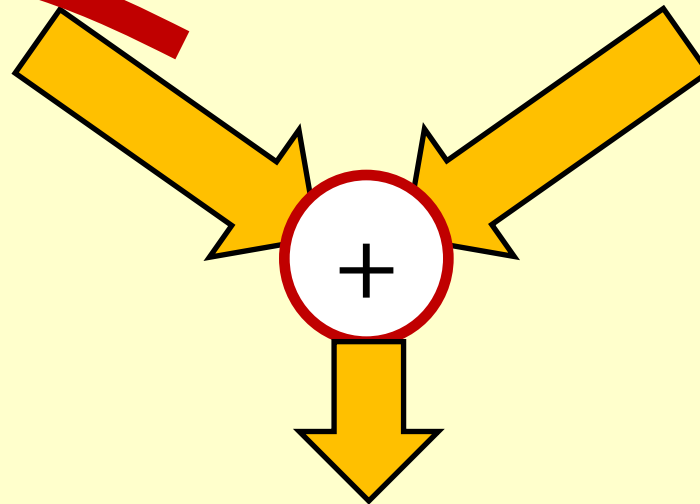
~~→ Sequential Process~~

Iterative Methods

~~→ Slow~~

→ Memory Efficient

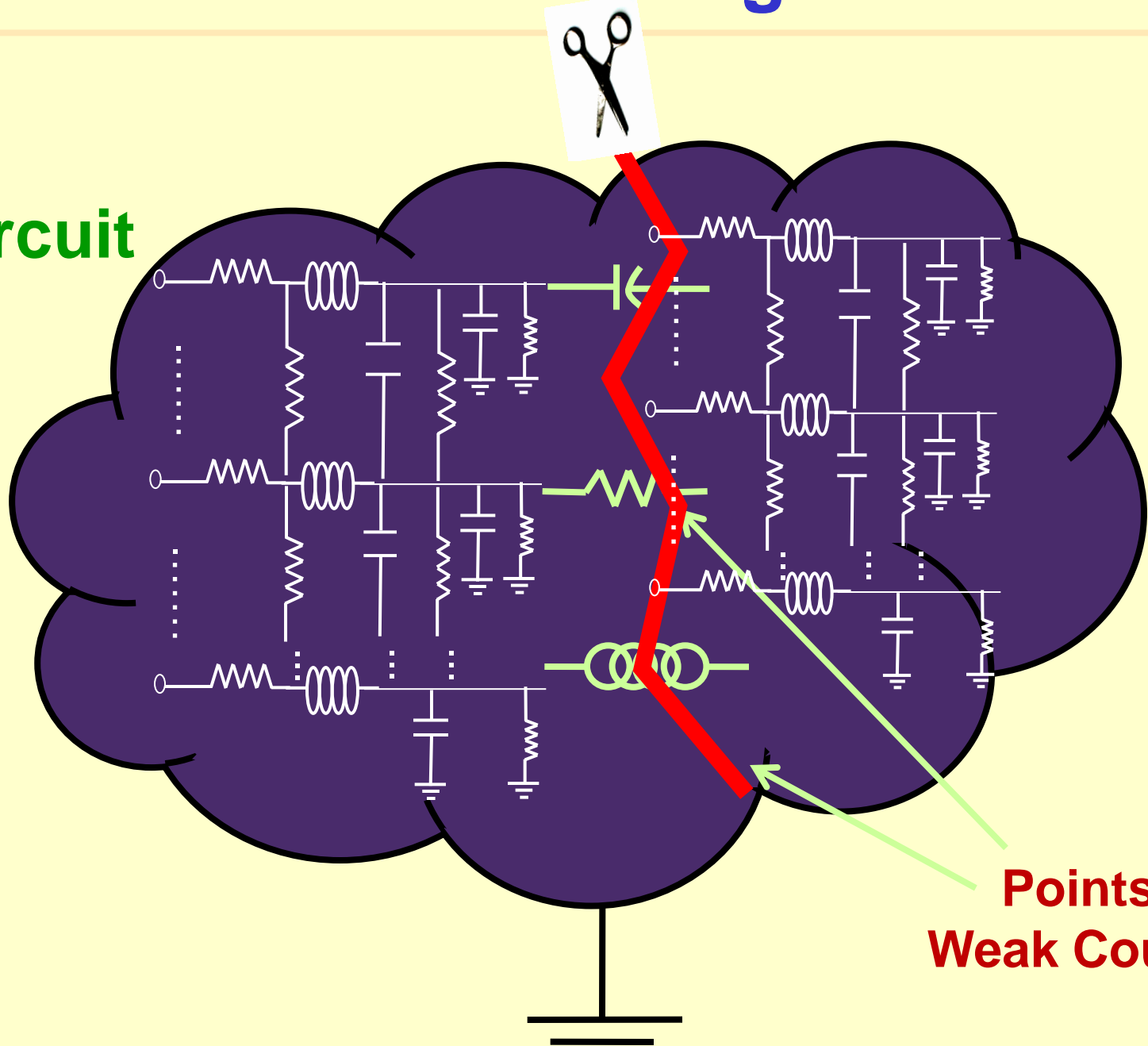
→ Parallelizable



→ **Waveform Relaxation based Power Grid Analysis**

WR Overview- Partitioning

Circuit



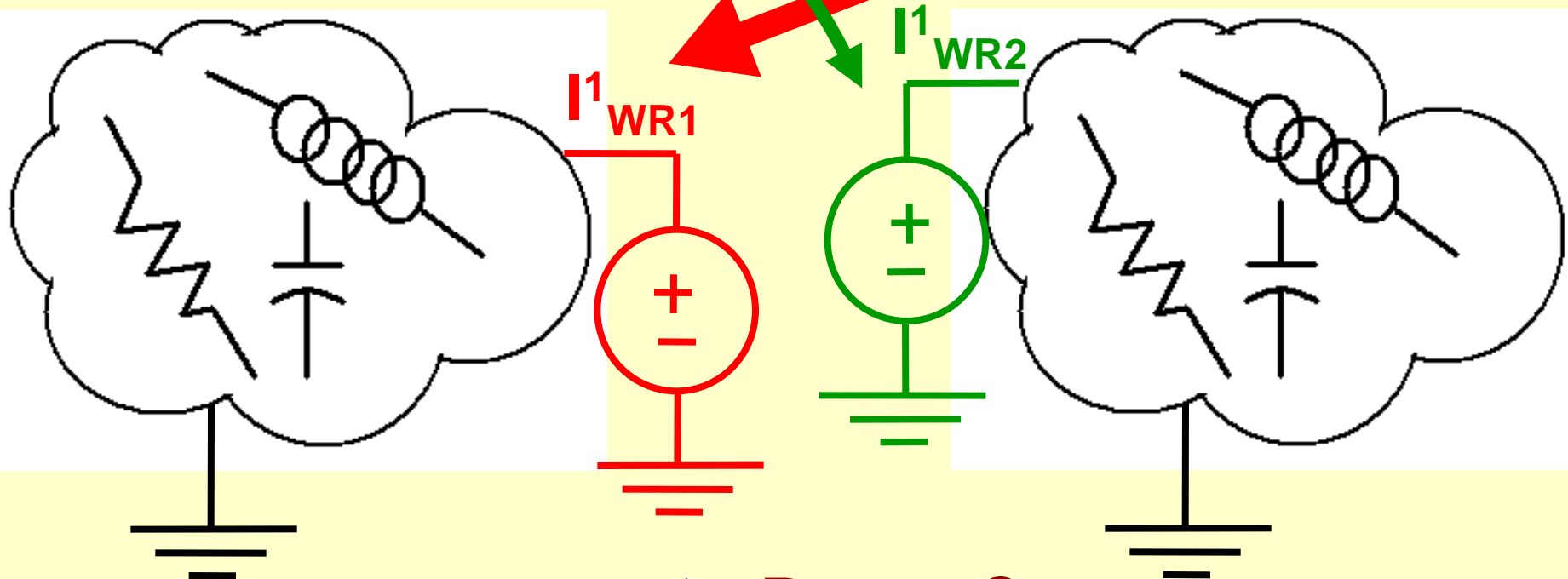
Points of Weak Coupling

WR Overview - Relaxation

Gauss Seidel

$\{V_1, I_1\}$

$\{V_2, I_2\}$



- **Better Convergence**
- **Memory Efficient**

WR for High-Speed Applications

Recent work:

→ Dense Coupled Interconnects

N. Nakhla, A. Ruehli, M. Nakhla and R. Achar, “*Simulation of coupled interconnects using waveform relaxation and transverse partitioning,*” *TAdvP*, pp.78-87, Feb. 2006.

→ Dense Coupled Interconnects with FD parameters

N. Nakhla, A. Ruehli, M. Nakhla, R. Achar & C. Chen, “*Waveform Relaxation Techniques for Coupled Interconnects with Frequency-Dependent Parameters*”, *IEEE TAdvp*, 2007.

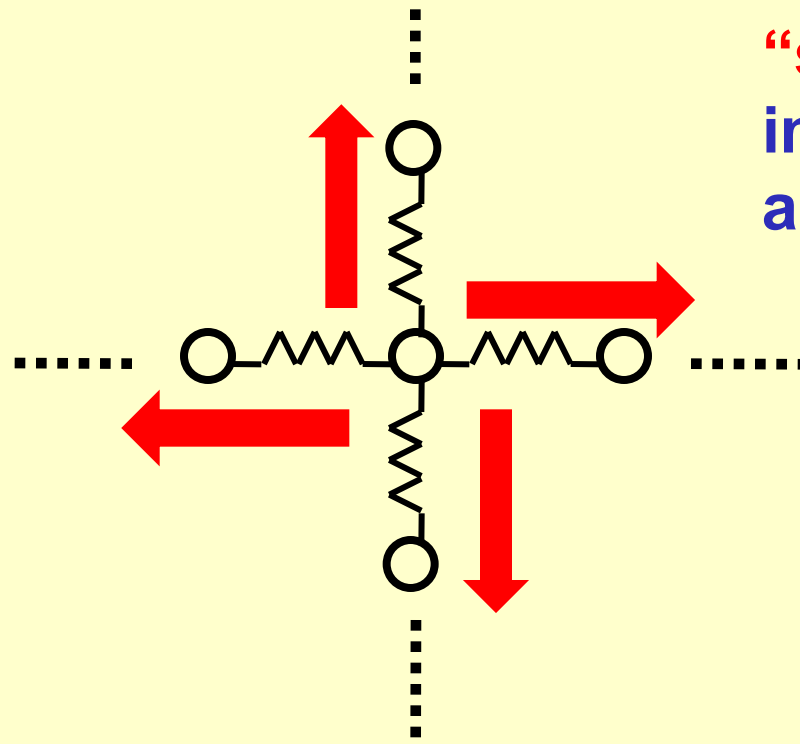
→ Large Multiport Networks

N. Nakhla, M. Nakhla and R. Achar, “*Sparse and Passive Reduction of Massively Coupled Large Multiport Interconnects,*” *ICCAD-2007*

WR for Power Grid Transient Analysis

- **Efficient Partitioning Schemes**
- **Improved initial-guess computation**
- **CPU efficient parallelization**

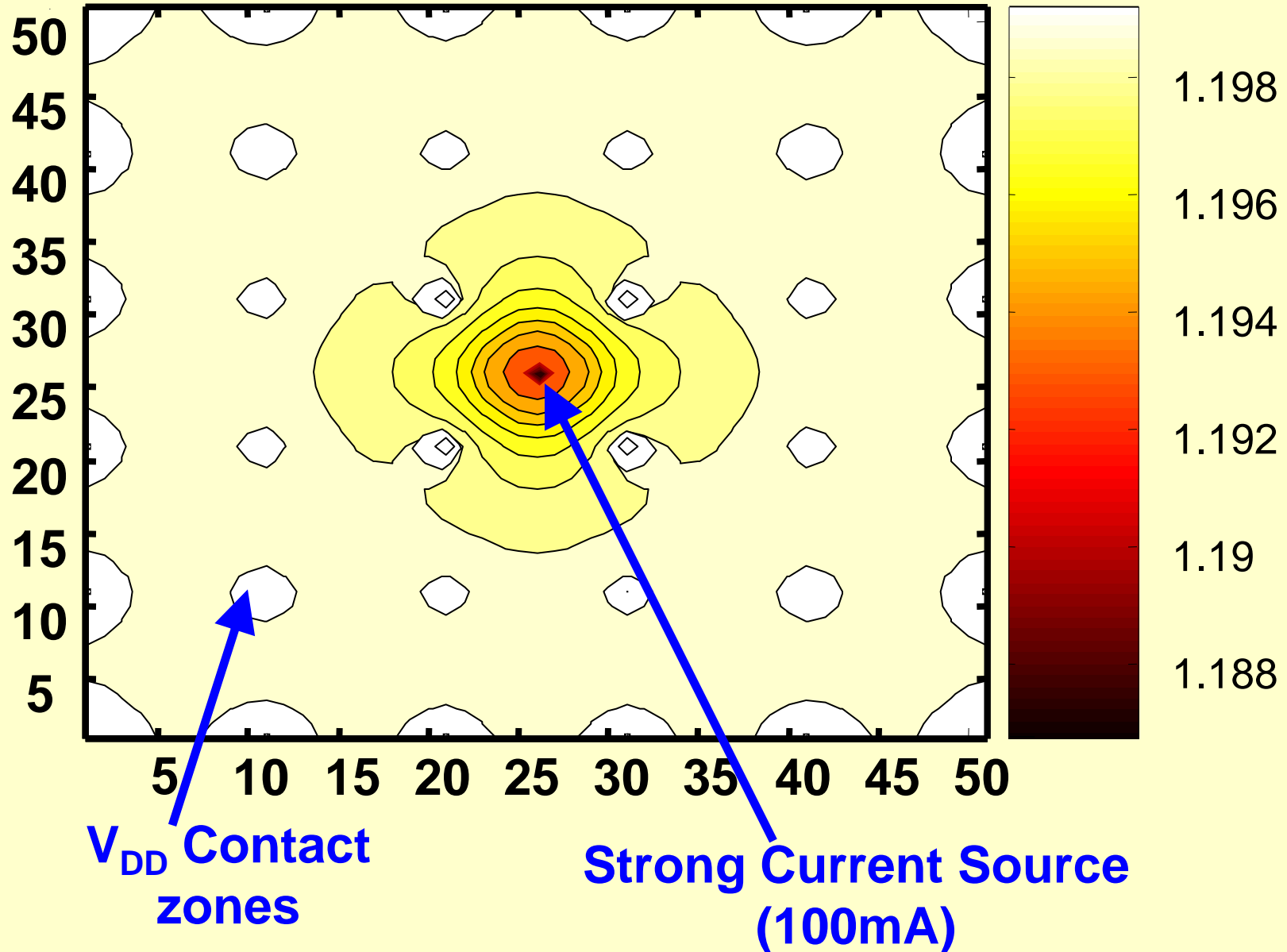
Partitioning



“strong” coupling
in all directions in
a Power Grid

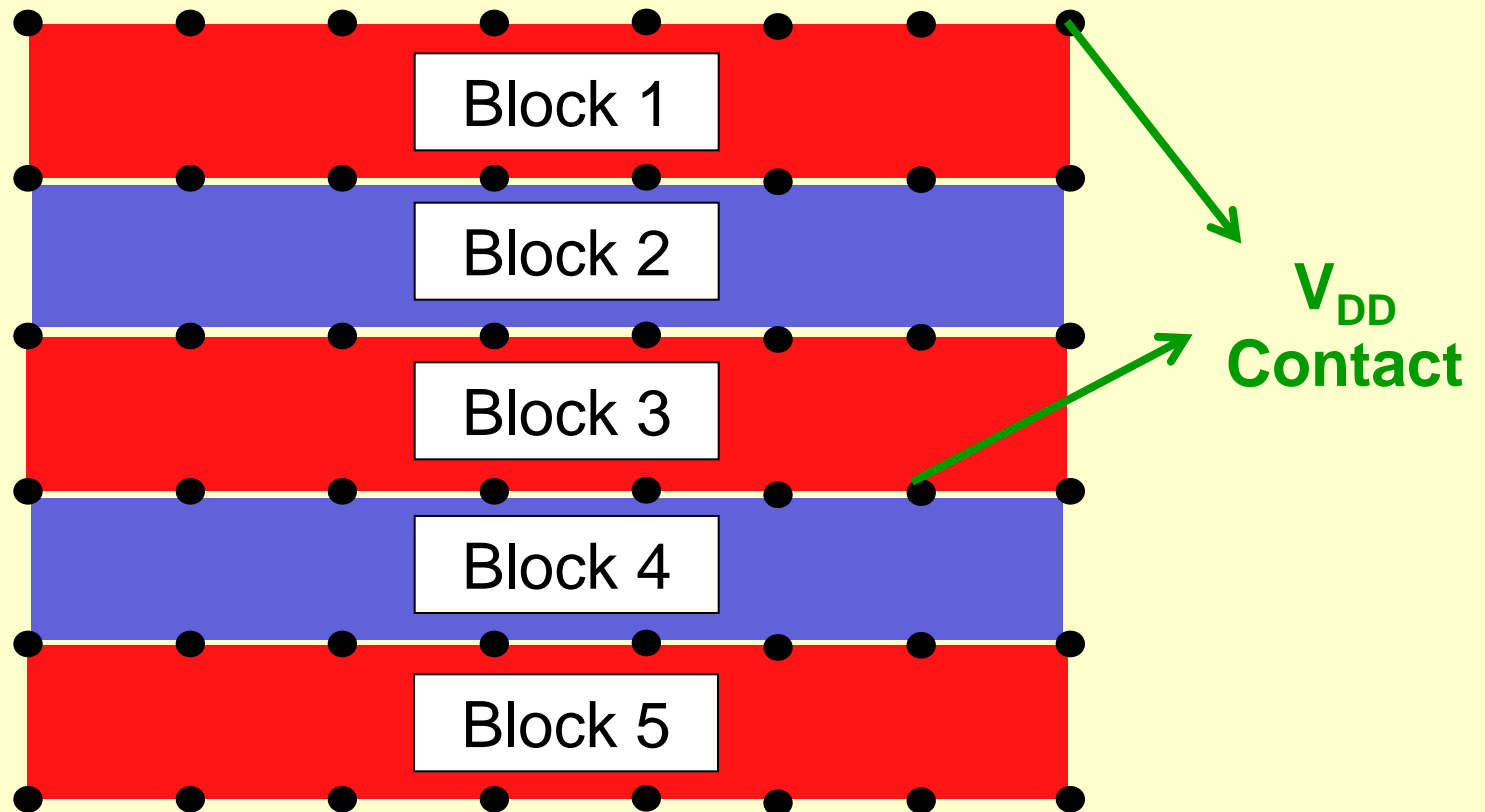
How to Partition the Power Grid????

Voltage Profiles - Sample 50X50 power grid

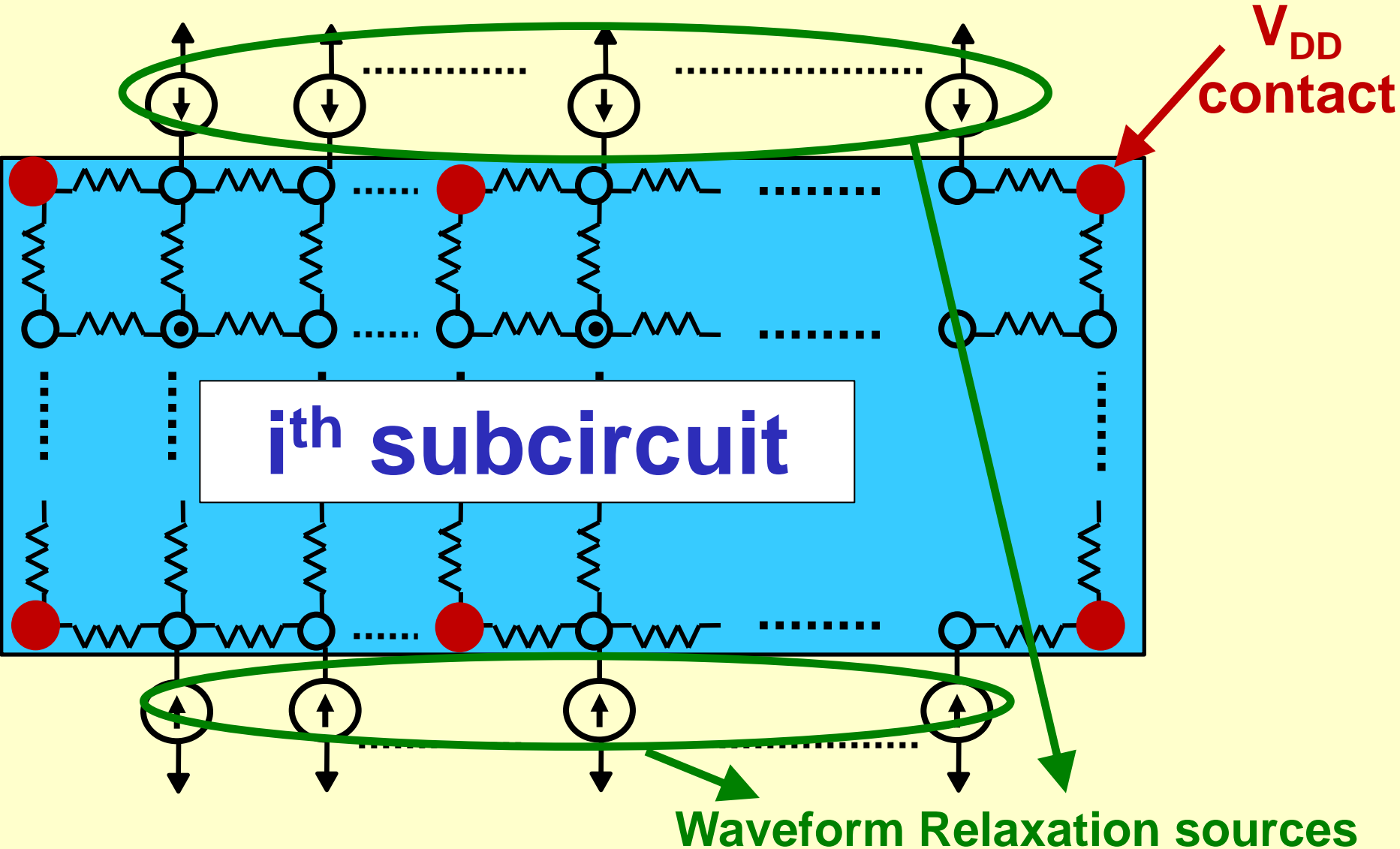


Partitioning

Block Row Partitioning



Block Row Partitioning



Initial-Guess Generation

MNA Equation for Power Grids

$$\mathbf{G}\mathbf{X}(t) + \mathbf{C}\dot{\mathbf{X}}(t) = \mathbf{B}\mathbf{u}(t)$$

For applying WR,

$\mathbf{X}(0)$

is required

very expensive!!!

“DC Solution” of the
power grid

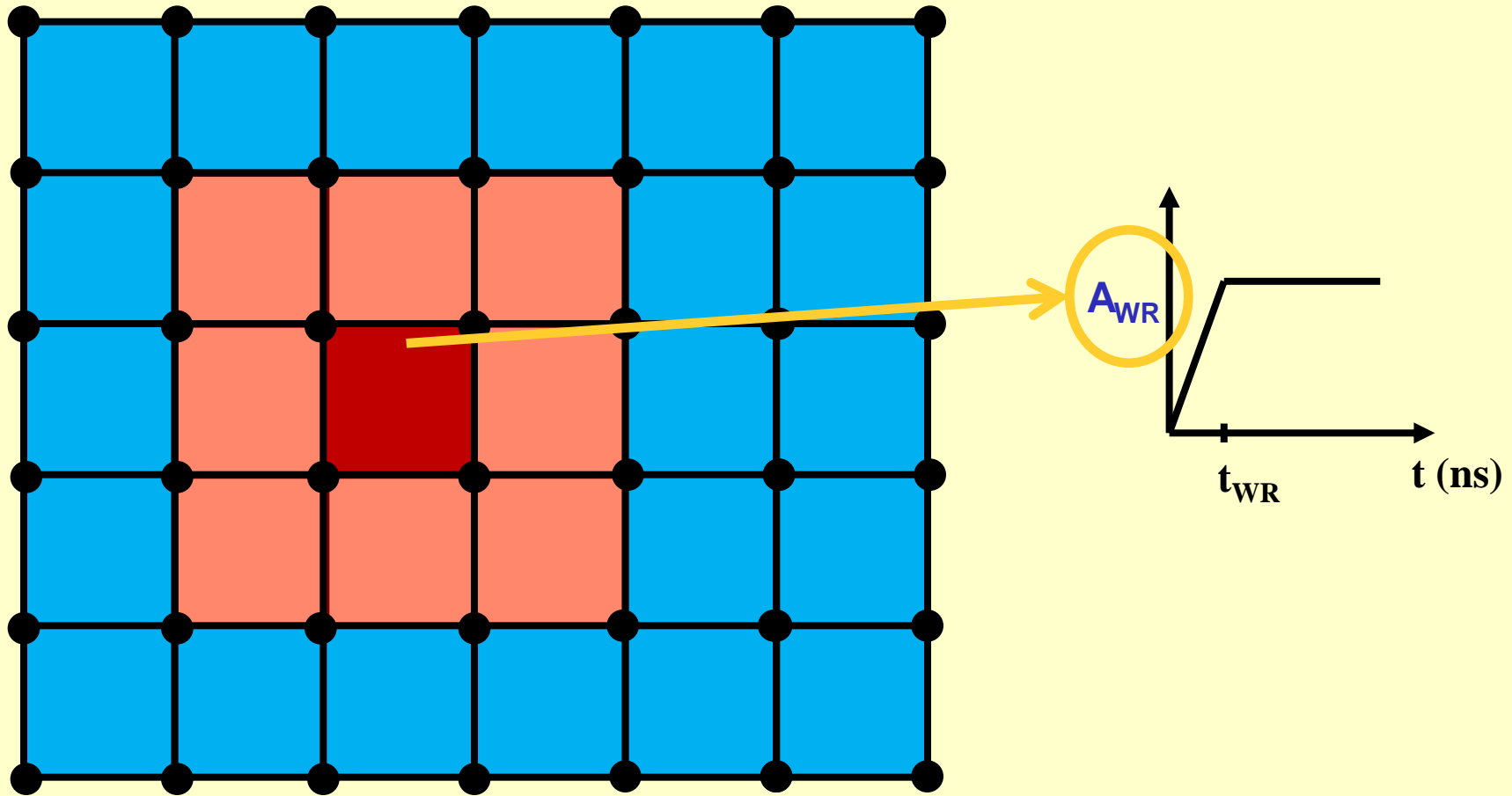
Must Solve:

$$\mathbf{G}\mathbf{X}(0) = \mathbf{B}_{DC}$$

Proposed → DC solution is made part of the WR iterations

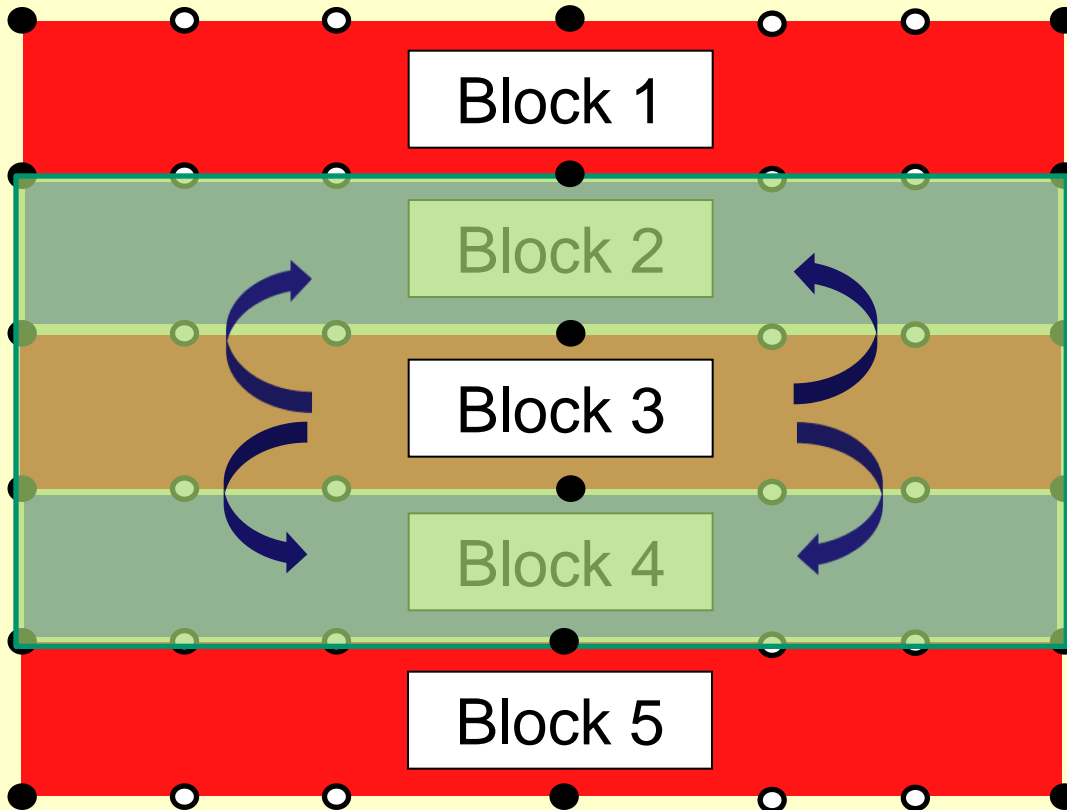
Estimation of A_{WR}

Estimation based on locality in DC solution



[Eli Chiprout, ICCAD 2004]

Parallelization Schemes

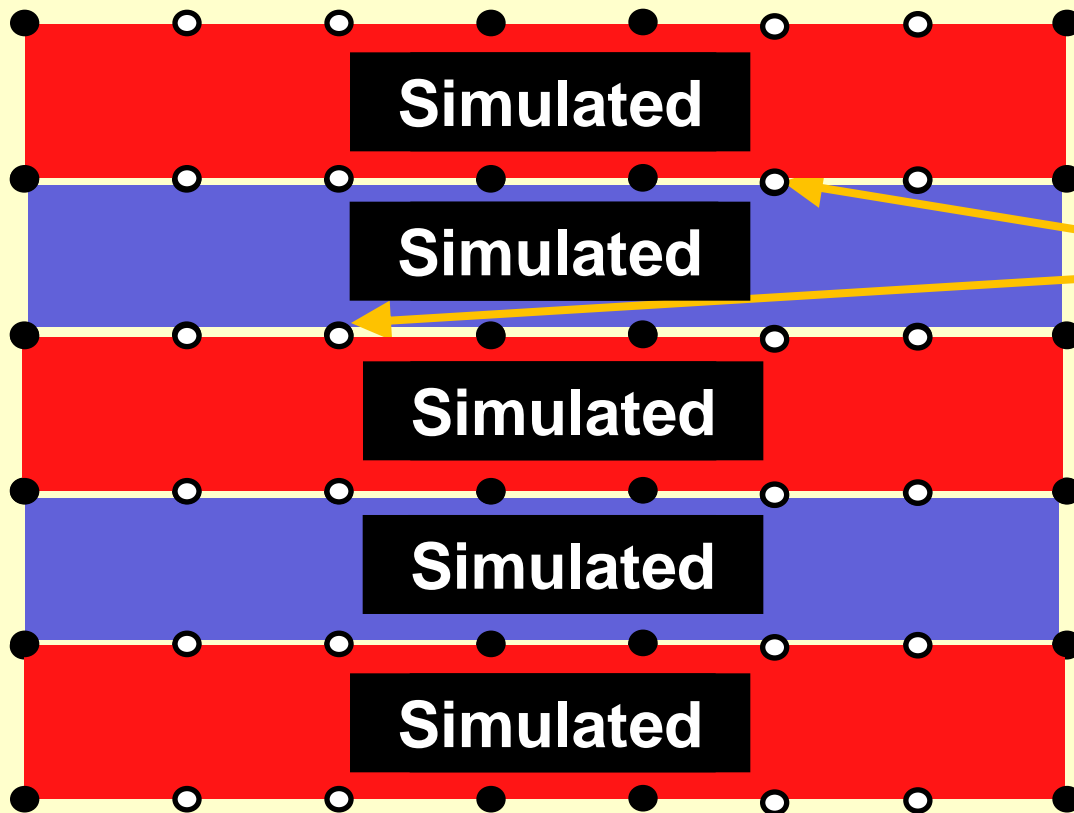


**coupling limited
to neighboring
block(s)**



Parallel GS-WR

Proposed Parallel GS-WR



- I. Simulate Odd blocks
- II. Update WR sources for Even blocks
- III. Simulate Even blocks
- IV. Update WR sources for Odd blocks
- V. Proceed to next iteration

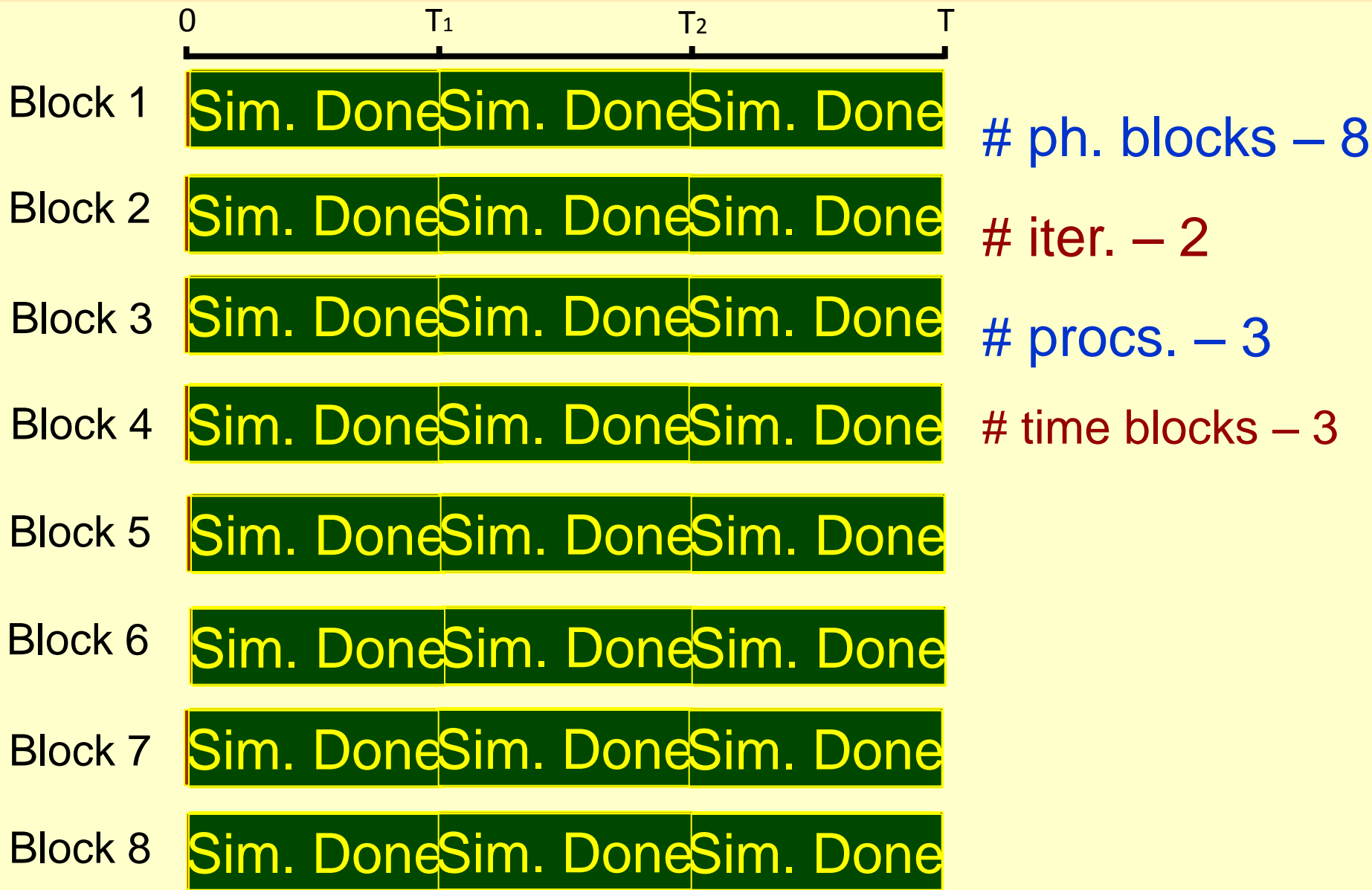
Enhanced pipelining

Pipelining via physical & time partitioning

- Scales well with the # of BRP partitions
- Scales well with the # of processors
- 100% CPU use ensured if

of time blocks = # of processors

Pipelining via physical & time partitioning

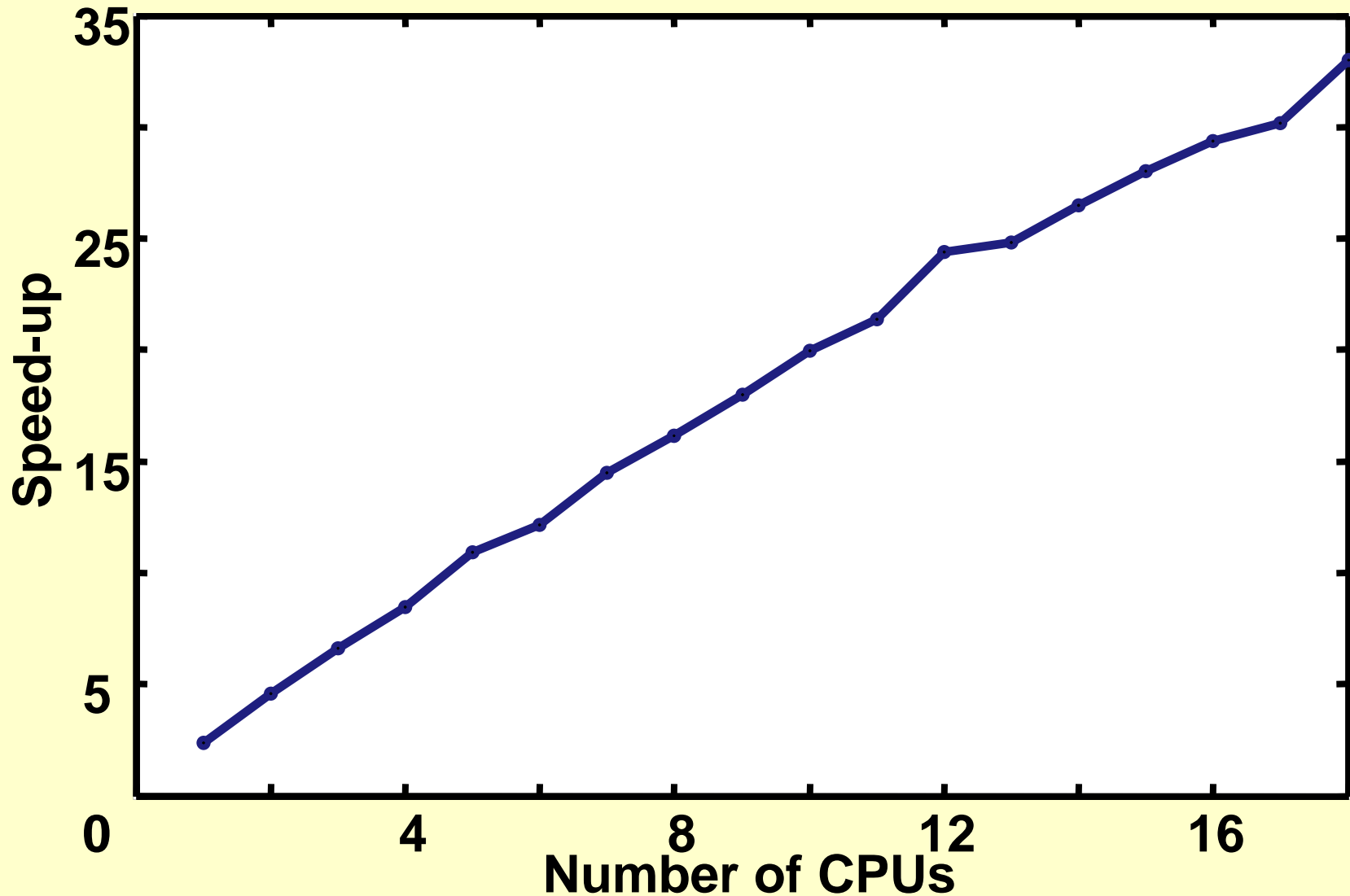


Power-Grid : 7.5 million nodes

Proposed GS-WR method		Direct- LU (CPU time) (min.)	Speed-Up
# CPUs	CPU time (min.)		
1	211	494	2.3
4	58		8
8	31		16
18	15		33

Example : 7.5 million nodes

Speed-Up Curve w.r.t. Direct-LU



Conclusions

- **Power-Grid Analysis :**

- **Large circuits**
- **CPU & Memory Intensive**

- **Emerging Parallel Platforms**

- **WR algorithms for transient analysis of power-grids**

- **Combines the merits of both direct & iterative methods**
- **Fast, Memory efficient**
- **Parallel & Scalable**

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