IEEE JOURNAL ON

EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS

CALL for PAPERS

Chip and Package-Scale Communication-Aware Architectures for General-Purpose, Domain-Specific and Quantum Computing Systems

Guest editors

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Scope, purpose and submission procedure

We are entering a new golden age of computer architecture, which is challenging but also exciting at the same time. The eminent end of Moore's law and Dennard scaling compelled everyone to conceive forthcoming computing systems once transistors reach their limits. Three leading approaches to circumvent this situation are using the chiplet paradigm, domain customisation and quantum computing. However, these architectural and technological innovations have shifted the fundamental bottleneck from computation to communication. Hence, on-chip and on-package communication play a pivotal role in determining the performance, efficiency and scalability of general-purpose, domain-specific and quantum computing systems. Due to this increasing significance, chip and package-scale communication has drawn a lot of attention from both academia and industry. This special issue promises a broad avenue to bring together academic and industrial explorations in chip and package-scale communications from multiple domains. Specifically, it will target the following:

- **General-Purpose Computing Systems: Data sharing and synchronisation between different cores (processors) demand efficient communication infrastructure within and between chips. Design practices like Network-on-Chip (NoC), Network-on-Package (NoP), and hierarchical interconnects are commonly used to optimise communication performance while reducing power consumption. Wireless, Optical, and 3D NoCs are some of the popular innovations proposed over the years. The first focus of this special issue is to present novel communication-aware architectures for adaptable general-purpose computing systems.**
- **Domain-Specific Computing Systems: They are tailored to particular application domains with specific communication requirements. Customised interconnects, accelerators and memory hierarchies are designed to minimise data movement and maximise computation efficiency. Chipletisation to integrate heterogenous Intellectual Properties (IPs) and In-Memory Computing (IMC) are recent innovations. The second focus of this special issue is to present novel communication-aware architectures for efficient domain-specific computing systems.**
- **Quantum Computing Systems: They promise to tackle problems beyond the ability of the fastest classical computing systems using the principle of superposition and entanglement. However, this will require millions of qubits, and we stand at around 500 qubits today. Hence, scaling a quantum computing system will require a communication infrastructure which is cryo-compatible and allows qubit synchronisation and entanglement. It should also reduce the effects of noise and quantum decoherence. The third and final focus of this special issue is to present breakthrough communication frameworks for scalable quantum computing systems.**

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Topics of interest

This special issue will explore academic and industrial research related to chip and package-scale communication for various computing paradigms. Topics include, but are not limited to:

- **NoC and NoP designs for general-purpose computing systems**
- **Cache coherent interconnects for I/O and compute devices (CXL, CCIX, etc.)**
- **Network interface designs for intra/inter-chip and rack-scale networks**
- **Emerging interconnect technologies, like wireless, optical, Carbon NanoTubes (CNT), 2.5D/3D**
- **Co-optimisations of communications with OS, compilers and programming models**
- **Security, reliability and scalability of on-chip and on-package communications**
- **Communications at large scales like data center, edge, and fog computing**
- **Modeling, characterisation, benchmarking, simulation and verification of communications**
- **Novel interconnection networks for domain-specific computing systems**
- **In-package die-to-die interconnects for chiplet integration (UCIe, BoW, etc.)**
- **New design methodologies (including ML-based) for chip and package-scale communications**
- **Communication/traffic-aware neural network architectures**
- **Data movement optimisation through task scheduling in domain-specific computing systems**
- **Near- and In-memory computing techniques for saving data movement**
- **Cryo-compatible communication infrastructures for scalable quantum computing systems**
- **Quantum intranet, internet and networking**
- **Quantum switches, routers, repeaters and other components for communication**
- **Communication-enabled architectures for multi-core quantum computing systems**
- **Interconnects for quantum neural network architectures**

Submission procedure

Prospective authors are invited to submit their papers following the instructions provided on the IEEE JETCAS website: https://ieee.atyponrex.com/journal/jetcas. The submitted manuscripts should not have been previously published, nor should they be currently under consideration for publication elsewhere.

Important dates

• Manuscript submissions due	March 04, 2024
• First round of reviews completed	April 22, 2024
• Revised manuscripts due	June 03, 2024
• Second round of reviews completed	July 01, 2024
• Final manuscripts due	July 22, 2024

Request for information

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