Editorial
Rolling Out the IEEE TVLSI EDICS

VLSI Systems research represents a dynamic and expansive domain. Over the years, it has evolved into a creative fusion of theoretical exploration, integrated chip design, performance evaluation, and practical applications related to the wide areas of circuits and systems, computer hardware and solid-state circuits. In acknowledgment of the extensive influence of very large-scale integration (VLSI) systems and the diverse research trends within this field, we have embarked on an Editor's Information Classification Scheme (EDICS) for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. The primary purpose of these EDICS is to provide a comprehensive description of the focal points within TVLSI. Furthermore, they aid in the judicious allocation of papers to associate editors and reviewers who possess expertise in the specific subject matter of each submission.

Interestingly, although most other IEEE TRANSACTIONS have had EDICS for many years, this is the first time EDICS categories are being rolled out for IEEE TVLSI. The landscape of VLSI systems is characterized by its dynamism, and thus, these EDICS are expected to undergo periodic adjustments to accurately encapsulate the interests of our authors and researchers, reviewers and editorial board.

In order to have the process converge in a timely manner the formulation of these new EDICS for TVLSI was steered by the Editor-in-Chief in collaboration with various Technical Committees of the IEEE CAS, CS, and SSC societies. The EDICS now encompass 19 overarching categories, each comprising multiple sub-EDICS. All sub-EDICS within a category share a coherent thematic framework. A novel numbering system has been introduced to enhance the clarity and organization of the sub-EDICS. Here are the new 19 TVLSI EDICS categories:

AMS—Analog and mixed-signal
RF—RF and microwave
DIGI—Digital circuits
HSIC—High-speed IC
MEM—Memory
PIM—Processing in and near memory
DNN—Deep neural network
SNN—Neuromorphic
SEC—Security
EDA—Electronic design automation
TEST—Testing and reliability
CPU—Processor design:
IoT—Internet of Things
REC—Reconfigurable computing
3DIC—Advanced technology nodes and 3-D integration
APPR—Approximate and stochastic computing
ET—Emerging technologies
OPTO—Photonics and optoelectronics
SENS—Sensors

And here is the complete list of EDICS and sub-EDICS:

AMS—Analog and mixed-signal:

1) Analog circuit design
2) Mixed-signal integrated circuits
3) ADCs and DACs
4) Voltage references and regulators
5) Analog filters and signal conditioning
6) Amplifiers/comparators/oscillators
7) Nonlinear circuits
8) PLLs
9) Power converters
10) Other

RF—RF and microwave:

1) RF circuit design
2) Microwave integrated circuits
3) Millimeter-wave ICs
4) Antenna-on-chip design
5) RF Filters and passive components
6) RF MEMS devices
7) RF energy harvesting
8) Other

DIGI—Digital circuits:

1) Deep submicron digital circuits
2) Digital circuit modeling and design
3) Flip-flops
4) Low-voltage and ultra-low-voltage digital circuits
5) Subthreshold circuit design
6) Digital signal processing
7) FFT and number theoretic transforms
8) Adder and multiplier design
9) Arithmetic circuits
10) Other

HSIC—High-speed IC:

1) High-speed digital circuits
2) High-speed analog and mixed-signal circuits
3) SerDes (serializer/deserializer) design
4) Clock distribution networks
5) Signal integrity in high-speed ICs

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6) High-speed memory interfaces
7) Other

MEM—Memory:

1) SRAM
2) DRAM
3) Flash
4) RRAM
5) STTRAM
6) Emerging memory
7) Memory interface circuits
8) Other

PIM—Processing in and near memory:

1) In-memory computing architectures
2) Near-memory processing units
3) Processing with-memory
4) Memristor and RRAM-based PIM
5) SRAM-based PIM
6) Memory-centric AI accelerators
7) Memory reliability in PIM
8) Other

DNN—Deep neural network:

1) Deep neural network architectures
2) Energy-efficient DNN inference
3) DNN training hardware
4) DNN hardware accelerator co-design
5) Sparsity techniques for DNNs
6) DNN quantization and compression
7) DNN-based edge devices
8) Other

SNN—Neuromorphic:

1) Event-driven computing
2) Neuromorphic chip architectures
3) Spike encoding and decoding
4) Brain-inspired computing
5) Spiking neural network hardware
6) Spike-based learning algorithms
7) SNN for robotics and control
8) Other

SEC—Security:

1) Crypto accelerators
2) Side-channel attacks and countermeasures
3) Trustworthy hardware design
4) Secure key storage and management
5) Physically unclonable function (PUF)
6) Hardware trojans detection and prevention
7) Post-quantum cryptography
8) Other

EDA—Electronic design automation:

1) Physical design automation
2) Logic and high-level synthesis
3) Formal verification
4) Low-power design automation
5) EDA for emerging technologies
6) EDA tools for 3-D IC design
7) Design for manufacturability
8) Other

TEST—Testing and reliability:

1) VLSI test structures
2) Built-In Self-Test (BIST)
3) Post-silicon validation
4) Reliability
5) Fault-tolerant circuit design
6) Testing of 3-D ICs
7) Analog/mixed-signal testing
8) Other

CPU—Processor design:

1) Microarchitecture design
2) Memory system architecture
3) Multicore and many-core processors
4) Parallel processing architectures
5) Network-on-Chip (NoC) architecture
6) Systems-on-Chip (SoC)
7) Graphics processors
8) Power management
9) Domain-specific architectures
10) Other

IoT—Internet of Things:

1) IoT sensor node design
2) Energy-efficient IoT hardware
3) Low-power communication protocols
4) IoT security and privacy
5) Wearable IoT devices
6) Other

REC—Reconfigurable computing:

1) Hardware acceleration on FPGAs
2) Partial reconfiguration strategies
3) Run-time reconfigurable systems
4) Field-programmable gate array (FPGA) architecture
5) Coarse grain reconfigurable architecture (CGRA)
6) Other

3DIC—Advanced technology nodes and 3-D integration:

1) FinFET and GAA circuit design
2) Monolithic 3-D integration
3) Heterogeneous integration techniques
4) 3-D memory stacking
5) Chiplet-based design
6) Thermal management in 3-D ICs
7) Power delivery networks in 3-D ICs
8) Other

APPR—Approximate and stochastic computing:

1) Approximate Computing Techniques
2) Stochastic computing architectures
3) Error-tolerant computing
4) Probabilistic hardware design
5) Precision-scalable computing

6) Approximate memory design
7) Other

ET—Emerging technologies:

1) Beyond CMOS technologies
2) Quantum computing hardware
3) Hardware for quantum communication
4) Quantum photonics
5) 2-D and 3-D nanoelectronics
6) Emerging memory technologies
7) Spintronics and magnetics
8) Bio-inspired hardware
9) Other

OPTO—Photonics and optoelectronics:

1) Photonic integrated circuits
2) Optical interconnects for VLSI
3) Silicon photonics
4) Photonic sensors and detectors
5) Optoelectronic memory devices
6) Optical computing architectures
7) Optical signal processing
8) Other

SENS—Sensors:

1) Photonic integrated circuits
2) CMOS imagers
3) Nonvisible
4) LIDAR
5) MEMS
6) Biomedical

I hope these new EDICS will help TVLSI systems moving forward by providing a framework for organizing activities and by helping authors, reviewers and the editorial staff. Every year we plan to gather feedback about the EDICS from all IEEE TVLSI constituencies in order to make adjustments when necessary.

This is the last issue of TVLSI for 2023, also the end of my first year as Editor-in-Chief, I am thankful to all the authors, reviewers, steering committee, administrative staff and editorial board for supporting TVLSI through another successful year. Happy New Year and Peace on Earth! Please join us on:

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Sincerely,

MIRCEA R. STAN, *Editor-in-Chief*
IEEE TRANSACTIONS ON VLSI SYSTEMS