# IEEE COMPUTER SOCIETY ANNUAL SYMPOSIUM ON VLSI

# CALL FOR PAPERS
## www.ieee-isvlsi.org

**ISVLSI 2024**

## July 1 - 3, 2024
## Knoxville, TN, USA

The 2024 Symposium explores emerging trends and novel ideas and concepts covering a broad range of topics in the area of VLSI: from VLSI circuits, systems and design methods, to system level design issues, to bringing VLSI design to new areas and technologies such as nano- and molecular devices, security, artificial intelligence, and Internet-of-Things, etc. Future design methodologies and new EDA tools are also a key topic at the Symposium. Over three decades the Symposium has been a unique forum promoting multidisciplinary research and new visionary approaches in the area of VLSI, bringing together leading scientists and researchers from academia and industry. The ISVLSI proceedings will be indexed in the IEEE Xplore Digital Library. Selected high quality papers will be further invited for submission to a journal special issue. The Symposium has established a reputation in bringing together well-known international scientists as invited speakers. The emphasis on high quality will continue at this and future editions of the Symposium.

## Contributions are sought in the following areas

- **Circuits, Reliability, and Fault-Tolerance (CRT):** analog/mixed-signal circuits design and testing, RF and communication circuits, adaptive circuits and interconnects, design for testability, online testing techniques, static and dynamic defect- and fault- recoverability, variation aware design, VLSI aspects of sensor and sensor network.
- **Computer-Aided Design and Verification (CAD):** hardware/software co-design, logic and behavioral synthesis, simulation and formal verification, physical design, signal integrity, power and thermal analysis, statistical approaches.
- **Digital Circuits and FPGA based Designs (DCF):** digital circuits, chaos/neural/fuzzy-logic circuits, high speed/low-power circuits, energy efficient circuits, near and sub-threshold circuits, memories, FPGA designs, FPGA based systems.
- **Emerging and Post-CMOS Technologies (EPT):** nanotechnology, molecular electronics, quantum devices, optical computing, spin-based computing, biologically-inspired computing, CNT, SET, RTD, QCA, reversible logic, and CAD tools for emerging technology devices and circuits.
- **System Design and Security (SDS):** structured and custom design methodologies, microprocessors/micro-architectures for performance and low power, embedded processors, analog/digital/mixed-signal systems, NoC, power and temperature aware designs, hardware security, cryptography, watermarking, and IP protection, TRNG and security-oriented circuits, PUF circuits.
- **VLSI for Applied and Future Computing (AFC):** Neuromorphic and brain-inspired computing, quantum computing, circuits and architectures for machine learning and artificial intelligence, methodologies for on-chip learning, deep learning acceleration techniques, applications for and use-cases of learning systems, sensor and sensor network, electronics for Internet of Things and smart medical devices.

The symposium program will include technical sessions by contributed papers and invited speakers by the Program Committee as well as a poster session. The keynotes, panels, special sessions, research demo sessions, and Student Research Forum are planned as well. Authors are invited to submit full-length, original, unpublished manuscripts in IEEE proceedings format (up to 6 pages). To enable blind review, the author information should be omitted from the submission. The manuscript as a single PDF is to be submitted online through Easychair.

## Paper submission deadlines

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| Paper Submission Deadline: | **March 4, 2024** |
| Acceptance Notification: | **April 15, 2024** |
| Submission of Final Version: | **May 6, 2024** |
| Special Session Proposal Deadline: | **March 4, 2024** |

Selected papers from ISVLSI 2024 will be invited for submission to a journal special issue. The selection process is based on reviewer feedback and quality of conference presentation

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**Industry Liaison Chairs**
Paul Montgomery, *Univ. of Tennessee, USA*
Hector Santos, *Univ. of Tennessee, USA*
Juan Lopez Jr., *DHS S&T, OSE, USA*

**Poster/Student Forum Chairs**
Tauhidur Rahman, *Florida Int. Univ, USA*
Ahmed Aziz, *Univ. of Tennessee, USA*
Laavanya Rachakonda, *Univ. N. Carolina, USA*

**Registration and Web Chairs**
Prasanth Yanambaka, *Texas W. Univ., USA*
Tyler Cultice, *Univ. of Tennessee, USA*

**Presentations/Video Chairs**
Amit Degada, *Marvell Technology, USA*
Joseph Clark, *Univ. of Tennessee, USA*

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