VENUE

The Bruges Meeting & Convention Centre (BMCC) is the ideal venue for special events, conferences, and trade fairs.
Its outstanding location, within walking distance of numerous Bruges hotels and world-famous attractions, meets all the needs of a modern event and conference location. The ground floor - with a total area of 4,500m^2 - is the ideal space for trade fairs, larger public events and even concerts. The upper floors are designed for meetings and conferences for 10 to 516 participants. The design of this unique building provides all that you need: a plenary room with a retractable seating platform for 516 people, a spacious foyer, poster areas, 12 breakout rooms and a catering area on the top floor with a beautiful view of Bruges city centre.

Beursplein 1, 8000 Bruges - Belgium

www.bmccbruges.com

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KU LEUVEN

The next circuits for a better life

ESSERC2024

9-12 September 2024
BRUGES (Belgium)

WWW.ESSERC2024.ORG

WHY BRUGES?

Bruges is a place that lives and breathes history. Visiting this historic city means travelling back in time to the Middle Ages. It is both magical and authentic. Brugge in medieval times was known as a commercial metropolis in the heart of Europe.

Bruges is one of Europe's best-preserved cities, evidenced by the fact that its historic city center has been designated an UNESCO world heritage site. The iconic spires of its cathedral and bell tower, its cobbled streets, winding canals and whitewashed façades are almost painfully picturesque.

In the 15th century, Brugge was the cradle of the Flemish Primitives and a center of patronage and painting development for artists such as Jan van Eyck and Hans Memling. Many of their works were exported and influenced painting styles all over Europe. Exceptionally important collections have remained in the city until today. Travelers from all over the world are coming to Belgium to visit Bruges.

GENERAL PURPOSE OF THE CONFERENCE

The aim of ESSERC (European Solid-State Electronics Conference) is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. It is a continuation of the past ESSDERC-ESSCIRC conferences. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary.
ESSERC is governed by a Steering Committee and consists of Plenary Keynote Presentations, invited papers and session on technology, circuits and joint papers bridging both device and circuit communities, respectively.

CONFERENCE TRACKS

Although not limited, papers are solicited for the following main topics:

Advanced Technology, Process and Materials
Process and material developments for logic, memory, and non-CMOS, including electrical and physico-chemical characterization, process integration and manufacturing: 2D TMDs and related insulators (e.g., hBN), graphene, TFTs, gate oxide, gate material, silicide, MOL and BEOL materials, 3D monolithic as well as conventional and novel memory cells including charge-based memories, ReRAM, MRAM, PCRAM, ferroelectrics, crosspoint and selectors, organic memory.

Analog, Power and RF Devices
From material growth to device, components, and systems (process, design, devices fabrication, applications). Device design and electrical/ physical/electro-thermal/reliability characterization of devices based on Si RF CMOS, RF SOI, SiGe HBTs, SiC, InP/InGaAs/ GaAs, AlGaN/InGaN/ GaN, CNT, diamond, and related material systems. Power systems integration issues including thermal management, packaging technologies, system-level electro thermal characterization, product quality and system reliability aspects. Device production processes and design for manufacturability.

Compact Modeling and Process/Device Simulation
TCAD and advanced simulation techniques and studies, compact/ SPICE modeling of electronic, optical, organic, emerging, and hybrid devices and their IC implementation and interconnection. Verilog-A models of semiconductor devices (including bio/ med sensors, MEMS, microwave, RF, high voltage and power, emerging technologies, and novel devices), parameter extraction, reliability and variability, performance evaluation and open-source benchmarking/ implementation methodologies. Modeling of interactions between process, device and circuit design, design/technology co-optimization, foundry/fabless interface strategies. Numerical, analytical, statistical modeling and simulation of electronic, optical and hybrid devices, interconnect, isolation, and 2D/3D integration. Simulations of material properties and fabrication processes. Advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport). Mechanical and/or electro-thermal modeling and simulation. Simulations of reliability aspects of materials and devices.

Analog Circuits
Building blocks, systems, and techniques operating in the analog or mixed-signal domain, such as amplifiers, drivers, comparators, filters, references, analog systems, analog interfaces, and analog techniques.

Data Converters
Nyquist-rate and oversampling A/D and D/A converters. Capacitance-to-digital, time-to-digital, frequency-to digital converters. Embedded and application-specific A/D and D/A converters. Analog to information conversion. A/D and D/A converter building blocks (sample-and-hold circuits, calibration circuits). Enabling new techniques, architectures, or technologies.

RF & mm-Wave Circuits
Building blocks and front-ends operating at RF, mm-Wave and THz frequencies for wireless communication, radar, sensing, and imaging.

Frequency Generation Circuits
Oscillators and controlled oscillators, PLL, DLL, injection locked oscillators, frequency dividers, any kind of frequency generation or time base circuits and systems.

Digital Circuits & Systems
Digital circuits and memory subsystems for microprocessors, micro-controllers, application processors, graphics processors; digital systems for communications, video, multimedia, security, and cryptography applications. Digital design techniques for power reduction, intra-chip communication, clock distribution, soft-error and variation-tolerant design, system-level integration. Devices and circuits for IoT and IoE security (e.g., PUFs, TRNGs).

Power Management
Power management and control circuits. Regulators. Switched-mode power converter ICs using inductive, capacitive, and hybrid techniques. Energy harvesting circuits and systems. Wide-bandgap topologies and gate-drivers. Power and signal isolators; robust power management circuits for automotive and other harsh environments. Circuits for lighting, wireless power and envelope modulators. Design for manufacturability

Wireless Systems
Wireless systems: radio transceivers, highly integrated front-ends, SoCs and SiPs, incl. heterogeneous packaging solutions, at RF, mmWave or THz frequencies, for established or future standards, as well as novel applications such as radar, sensing, and imaging

Wireline and Optical Circuits and Systems
2.5/3D interconnect, copper-cable links, and equalizing on-chip links, exploratory I/O circuits for advancing data rates, chip to chip system communications, high speed serial interfaces, optical interfaces, laser drivers, optical receivers, clock and data recovery.

Emerging Computing Devices and Circuits
Novel devices and circuits to improve existing and enable new computing paradigms. In-memory computing and logic-in-memory using emerging devices. Qubit devices and cryogenic circuits for quantum computing. Non-charge-based logic devices and circuits (magnetic logic, spintronics and plasmonics), beyond CMOS transistors (tunnel FETs, Dirac-source FETs). Devices and circuits based on low-dimensional systems (2D materials, nanowires etc.), topological insulators, and phase transitions.

Architectures and Circuits for AI and ML
Silicon implementations of AI, ML, neuromorphic accelerators and processors, together with their applications. Edge and cloud AI computing platforms. In- and near-memory computing at the array/processor-level using commercially available technologies.

Devices & Circuits for Sensors, Imagers and Displays
Devices and circuits based on MEMS and bioelectronics devices for biomedical and imaging applications. Image sensors and related circuits and systems, SoCs. Automotive, LIDAR, and ultrasonic sensors for ADAS, autonomous driving, smart mobility. MEMS sensor systems. Wearable, implantable, ingestible electronics, biomedical SoCs, neural interfaces and closed-loop systems. Biosensors, microarrays, and lab-on-a-chip. Display electronics, displays with sensing functionality. Devices, circuits, and systems for AR/VR and related sensing/actuation. Product quality and reliability aspects. Device and circuits production processes and design for manufacturability

CONFERENCE HIGHLIGHTS

- Keynote presentations
- Invited papers with overall coverage of all aspects of advanced devices and circuits
- Presentation of IEEE and ESSDERC-ESSCIRC 2023 Awards
- ESSERC Gala Dinner on Wednesday, September 11, 2024
- Tutorials and workshop

PAPER SUBMISSION

PAPERS SUBMISSION DEADLINE: APRIL 5, 2024

Papers submitted for review must clearly state:
- The purpose of the work
- How and to what extent it advances the state-of-the art
- Specific results and their impact

Only work that has not been previously published or submitted elsewhere will be considered. Submission of a paper for review and subsequent acceptance is considered as a commitment that the work will not be publicly available prior to the conference. Measurement results or calibration against measured data is required to support the claims of the submitted paper.

After selection of papers, the authors will be informed about the decision of the Technical Program Committee by e-mail by 24 May 2024.

At the same time, the complete program will be published on the conference website. An oral presentation will be given at the Conference for each accepted paper. No-shows will result in the exclusion of the papers from any conference related publication. The submitted final PDF files should be IEEE Xplore compliant.
For each paper independently, at least one (co-)author is required to register for the Conference (one registration one paper policy).
Registration fees and deadlines will be available on the conference website.

BEST PAPER AWARD

Papers presented at the conference will be considered for the "Best Paper Award" and "Best Young Scientist Paper Award". The selection will be based on the results of the paper selection process and the judgment of the conference participants. The award delivery will take place during ESSERC 2025.