CASS-Wide Webinar XXI: Low Power Cryo-CMOS Design for Quantum Computing Applications, Speaker: Sudipto Chakraborty

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Live Webinar Question & Answers

Q. What is stark shift?

A. An RF tone will change the qubit's resonant frequency. How much the frequency of the qubit changes is linearly dependent on the amplitude of the RF, and inversely dependent on the difference between the RF and the qubit's frequency.

Q. How the bending of the path is adjusted for frequency modulation in fabricated chip?

A. This refers to the resonator associated with the transmon. It is fixed and not adjusted for the frequency modulation. The circuits simply provide the signals at the desired frequency.

Q. How is QLA different from LNA ?

A. QLA (quantum limited amplifier) is the first stage of amplification. physicists think about it in terms of microwave photons, because that's how of it, but it basically just amplifies the readout RF pulse. It sits at the lowest stage in the cryo (~10mK), so there is very little loss between readout resonator and QLA.The LNA is the 2nd stage of amplification and sits at a higher stage (~4K), and has significantly more gain than the QLA, and it also provide enough gain to overcome the lossy coax between 4K and 300K.There is also a 3rd stage of amplification, which is at RT. Cryogenic LNAs in Silicon technology is an active area of research at the moment.

Q. How can one design CMOS qubit interfacing circuits if cryo-CMOS PDKs are not available?

A. Answered during the Q&A session, please refer to the recording but fundamentally using: (a) compensation and calibration, and (b) using low gain approaches (e.g. current mirror instead of gm) to reduce uncertainty

Q. Whether advanced tech can be used in design

A. Yes, Technology scaling should help the power consumption and area, so 7nm and 5nm nodes can be used

Q. How to cancel the phase and amplitude imbalance in LOI and LOQ going to the mixer?

A. The mixer itself is a switching type, so that takes care of amplitude imbalance (e.g., a limiter should ideally remove amplitude imbalance). For phase imbalance, fine and coarse adjustments are provided before and after the frequency divider respectively, with the sensor implemented using an XOR gate after the coarse adjustment buffer. In traditional wireless approaches, this adjustment is typically implemented in digital domain but since we have to implement a look up table based phase rotation, an analog implementation is used. The fine adjustment adjusts the duty cycle of the LO waveform before the div2, which leads to I-Q error adjustment.

Q. Where could we locate the ppt slide?

A. CASS website for the webinar repositories

Q. For being able to optimize the LO for power consumption, it is needed to know to minimim phase noise requirement needed. How do you decide this?

A. Typically for low x-talk between qubits, the frequencies are typically kept far away. If the frequencies are too close, then the signal from intended qubit will interfere with the unintended qubit, causing interference (also known as Stark-shifts in qubits); This is why a few MHz separation is good, and 5MHz and beyond are favorable numbers. Typically 10-50MHz separation is used and we care about phase noise at those far out offsets. The phase noise will follow the traditional shaped noise from PLLs. At far-out frequencies, it is limited by the buffers. So, the phase noise would actually transition from -20dB/dec slope to a zero slope as the frequency increases.

The calculation of the phase noise is much related to the way we use communication systems. As an example, assume that the qubits operate with -6dBm Pout with -150dBc/Hz noise floor and 100MHz bandwidth. This means, that the Interfering signal within the bandwidth is -6-150+10*log10(100e6)=-76dBm; hence, this interfering signal is 70dB below the "un-intended" qubit, so it might not provide perturbations to change the information state.

Q. **Are voting circuits used in QC**?

A. Not extensively, but error correction is essential and frequently used.

Q. **In the comparison table, the power is 12.8mW vs 23mW, but the output amplitude is also half 25mVp vs 50mVp, would that mean they are comparable?**

A. No, the output stage consumes only 15-20% of the overall power consumption, so the 12.8mW is indeed a superior solution

Q. If we want to design at the SoC level, what are the different challenges of designing under cryogenic temperature?

A. Typical challenges of SoC integration including SNR, SFDR, xtalk. Typically this is a system using multiple channels of very sensitive qubits, so x-talk becomes a major challenge. Then the packaging aspects are also non-trivial

Q. What is the circuit element “BBF”?

A. Base Band Filter, it’s the circuit between the DAC and the mixer using gm-C filtering function with low input impedance and high output impedance with independent gain and bandwidth adjustment.

Q. Are there any quick guidelines/tips which can be followed during the design/simulation phase using the available models (that can work till -40degC) that can ensure a good yield at cryo temperatures ?

A. We did not have cryo models, but simulated with the foundry models at 100K, which predicted the trends and they show similarity with the 4K measurements. Typically at low temperatures, the performance does not decrease linearly with temperature, but goes asymptotically down. Lot of compensation and calibration circuits were used to mitigate uncertainly and guarantee reasonable performance at low T even with modeling uncertainties.

Q. **When the chip generates self-heating and the temperature rises, is it possible to get the chip out of the deep cryogenic state? In this case, how to keep the chip temperature relatively stable?**

A. It is possible, but does not happen in practice. The ambient temperature is at 4K, while the circuits' junction temperature rises as they consume current. However, these increases are small because the circuits themselves are low power. An initial measurement indicates that the junction temperatures could be somewhere between 25-30K, which is reasonable for cryo operation.

Q. **My question has both technical & non-technical parts**

Q1) Technical question- Are there any PDKs specialized to cryo-CMOS design that is currently available ?

A1) Not at the moment, however the leading foundries (TSMC, Samsung) are working towards creating them.

Q2) Non-technical question- is based on countries secretly restricting the import/export of quantum computing components on the ground of security reasons. Do you think- trading QC components, sharing ideas or knowledge exchange on quantum computing should be restricted on the ground of misusing the quantum supremacy or winning who achieves supremacy first?

A2) This is beyond my capability to answer but like AI, something should be done to ensure that the usage does not fall into misuse or hurt humanity.

Q. Not sure if I understood correctly, but did you mention that higher frequency control for the qubit will give rise to better fidelity? (at the cost of higher power?)

A. The fidelity is given by the qubits. The energy spacing increases with frequency (E=hw); it's typically not controlled by the electronics but we do have to ensure that the pulse amplitudes etc. enables the qubit operation at the two lowest states. However, typically the broadband part of the electronic circuits consume higher power at 20GHz compare to 5GHz.