IEEE JOURNAL ON
EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS

CALL for PAPERS

2.5D/3D Chiplet Circuits and Systems, EDA, Advanced Packaging, and Test

Guest editors

Qinfen Hao, Chinese Academy of Sciences (haoqinfen@ict.ac.cn)
Kuan-Neng Chen, National Yang Ming Chiao Tung University (knchen@nycu.edu.tw)
Sandeep Kumar Goel, TSMC (skgoel@tsmc.com)
Hai Li, Duke University (hai.li@duke.edu)
Erik Jan Marinissen, imec (Erik.Jan.Marinissen@imec.be)

Scope and purpose

The task of integrating an increasing number of transistors onto a single chip is becoming increasingly arduous and costly. To counter this challenge, chiplet technology has captured the interest of both industry and academia. A chiplet is a small integrated circuit (IC) with a well-defined function, designed to be incorporated alongside other chiplets within a single package as a multi-die stack. Despite the current interest in a chiplet-based design approach, the associated technology faces numerous challenges that are influencing its development trajectory. This special issue is dedicated to showcasing the latest technological advancements in the field of chiplet technology and its applications.

In general, the chiplet interconnects faces design challenges such as achieving high bandwidth, low latency, high energy efficiency, high edge bandwidth density, low bit error rate, etc. There are existing standards for chiplet with no consideration on compatibility with each other at PHY layer specification, this raises the implementation cost of IP vendors and SoC designers.

Designing a chip based on the chiplet approach presents the challenge of how to effectively split a monolithic design into individual chiplets. An improper division will negatively impact the chip's performance and power efficiency. Furthermore, SoC designers must carefully consider the design of the system bus or I/O connected by chiplet interconnects, and keep the underlying structure remains transparent to the upper-layer software.

When developing a chip based on the chiplet approach, the SoC designer will meet the lack of comprehensive EDA tool coverage from front-end to back-end. For example, there are no EDA tools for multi-chiplets co-simulation in the front-end phase. They must leverage existing EDA tools that were initially designed for the development of monolithic SoC designs. Although multi-physics field co-simulation is utilized to identify potential risks before the tape-out phase, it is more beneficial and cost-effective to detect and mitigate issues during the front-end phase.

While chiplets are typically considered to be connected by interposers in advanced packaging, new methods such as silicon bridges have garnered public attention due to their lower cost. Hybrid bonding is also emerging as a promising technique for its extremely high density. 3D stacked ICs based on the chiplet approach draw more attention for their efficient way to integrate functional chiplets, but also result in more problems such as thermal.

2.5D- and 3D-stacked ICs based on the chiplet approach have many more potential test moments than conventional chips. Every test that is executed adds cost, and therefore, executing all these tests might lead to overkill and excessive test costs. However, not executing tests could lead to even higher costs. At the same time, pre-bond testing of the non-bottom dies is a challenging task, and we need to rely on a cooperative design-for-test infrastructure in the die-under-test and all dies below it.

The objective of this special issue is to give a systematic view of chiplet technology from many aspects, to find possible solutions for challenges, and to compile the latest research findings from researchers in the field.

Topics of interest

To give a comprehensive introduction to this field, we are soliciting paper submissions presenting the latest developments in SoC architecture for chiplet-based IC and chiplets, chiplet interconnects, dedicated EDA tools along the entire design trajectory, 2.5D/3D advanced packaging, 2.5D/3D test and DfT. This special issue's area of interest includes (but is not limited to) the following topics:

- Architecture exploration for chiplet-cased ICs
- System and technology co-optimization (STCO) for chiplet and advanced packaging
- System bus design in chiplet-based ICs
- General purpose computing chiplet
- Accelerator chiplet
- High-speed and low power I/O chiplet
- Multi-protocol combination design in I/O chiplet
- High-bandwidth memory chiplets
- High-speed design for chiplet interconnects
- Energy-efficient design for chiplet interconnects
- Multi-standard support in chiplet interconnects
- Adaptable I/O design for chiplet interconnects
- Floorplanning, partitioning, placement and routing optimization for chiplet-based IC by AI/ML
- Interconnect planning and synthesis
- Package/3D-IC placement and routing
- Extraction, TSV, and package modeling
- Deterministic/statistical timing analysis and optimization for chiplet-based IC
- Multi-chiplet functional co-simulation
- Multi-physics field co-simulation
- 2.5D/3D packaging and platforms
- Si/Glass/Organic-based interposer
- Si/Glass/Organic-based RDL
- Fanout wafer level and panel level packaging
- Hybrid bonding
- New chiplet and advanced packaging concepts and platforms
- Chiplet and stack description languages for advanced packaging
- SI and PI design for chiplet and advanced packaging
- Thermal design and materials in chiplet and advanced packaging
- Electromagnetic compatibility design in chiplet and advanced packaging
- Yield and cost estimation of stacked dies for chiplet and advanced packaging
- Stress, warpage, and reliability issue for chiplet and advanced packaging
- Built-In self-test (and repair) for chiplet interconnects
- Defects in chiplet Interconnects
- Design-for-test for and repair of chiplet interconnects
- DfT architectures for chiplet-based ICs
- EDA design-to-test flow for chiplet interconnects
- Failure analysis for chiplet interconnects
- Fault-tolerant design for chiplet interconnects
- Interposer testing
- Pre-, mid- and post-bond testing
- Reliability of chiplet interconnects
- Standards for chiplet interconnect test and repair, incl. IEEE Std P3405
- Standards for chiplet testing, incl. IEEE Std 1838
- Test flow optimization for chiplet interconnects
- Test pattern generation for chiplet interconnects
- Yield of stacked dies and their Interconnects

Submission procedure

Prospective authors are invited to submit their papers following the instructions provided on the IEEE JETCAS website: https://ieee-cas.org/publication/JETCAS/manuscript-submission-guide. The submitted manuscripts should not have been previously published, nor should they be currently under consideration for publication elsewhere. The IEEE JETCAS submission site: https://ieee.atyponrex.com/journal/jetcas

Important dates

- **Manuscript submissions due:** **March 03, 2025**
- **First round of reviews completed:** **April 21, 2025**
- **Revised manuscripts due:** **June 02, 2025**
- **Second round of reviews completed:** **June 30, 2025**
- **Final manuscripts due:** **July 21, 2025**

Request for information

Corresponding Guest Editor: Qinfen Hao (haoqinfen@ict.ac.cn)