UNIC-CASS Design-to-Tapeout(Sept. 11, 2024)

Analog flow for mock tapeout and precheck steps on Efabless platform

Presented by: D-to-T mentoring team

Gabriel Maranhão





UNIC-CASS educational material



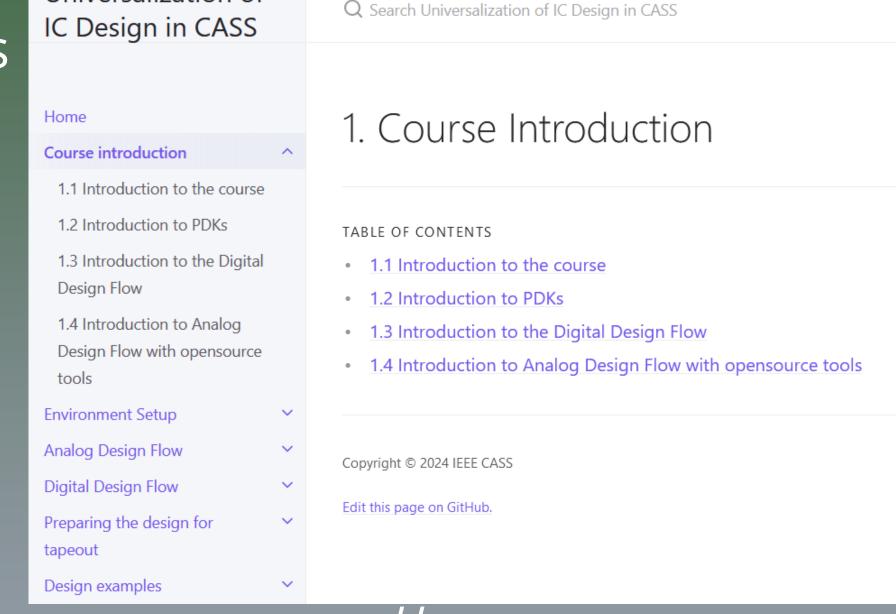
Universalization of IC Design from CASS (UNIC-CASS)

৪২ 9 followers & https://ieee-cas.org/universalization-i...

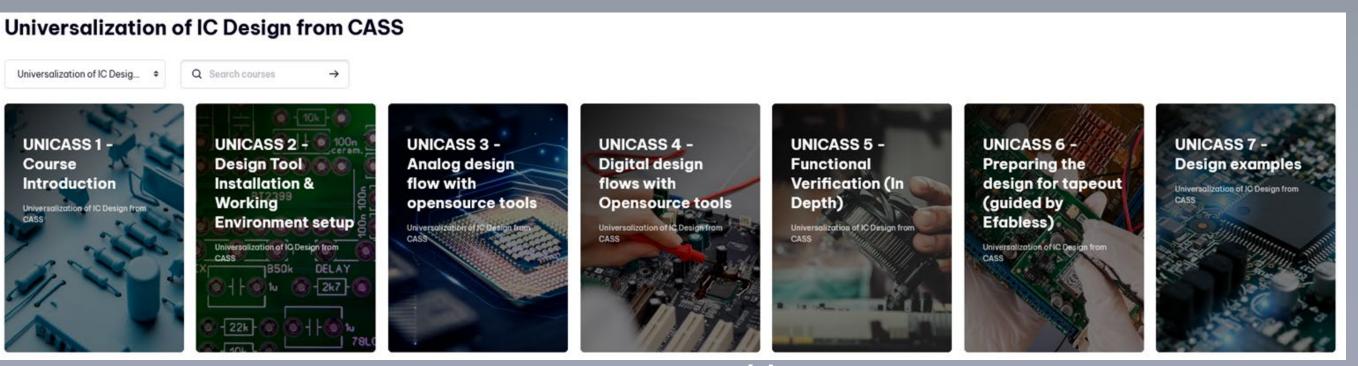
Source: https://github.com/unic-cass/unic-cass.github.io

Universalization of

- New videos made by volunteers following the lecture notes
- Lecture notes in Markdown format
 - ⇒ You can contribute by updating them
- New document theme using Just-the-docs Jekyll theme
- Latest materials in Github
- Materials in CASS-Mile will be updated into v2.0 soon
- Add instructions for Klayout in analog design flow
 - Layout
 - DRC
 - LVS



Website: https://unic-cass.github.io



[Duy-Hieu Bui, Vietnam National University Hanoi]

CASS-MiLE: <u>https://ml.ieee-cas.org</u>

Mock tapeout and Precheck

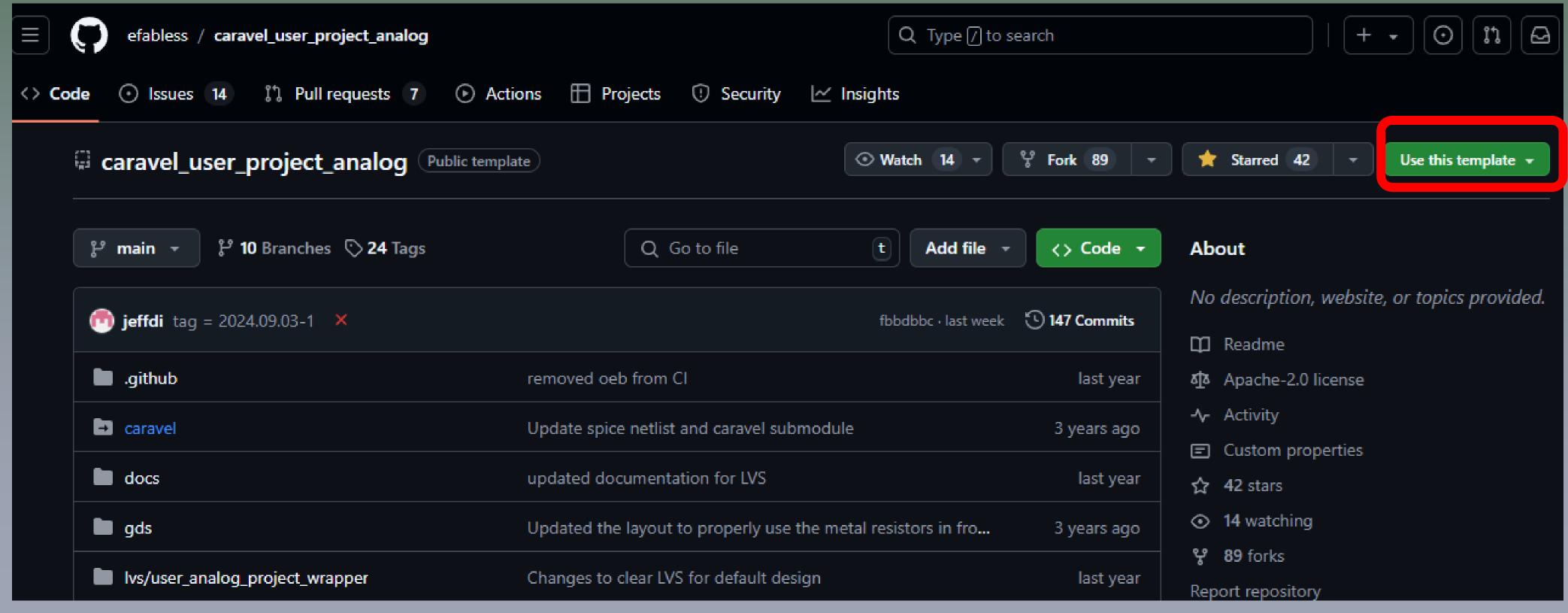
- First two stages that are correlated. Learn how to use the Efabless platform and to submit a project for tape-out;
- Mock tape-out: Is a empty or a really simple circuit/project;

Precheck: A verification processes to validate the files inside the project directory;

Efabless YouTube Playlist to help with these steps.

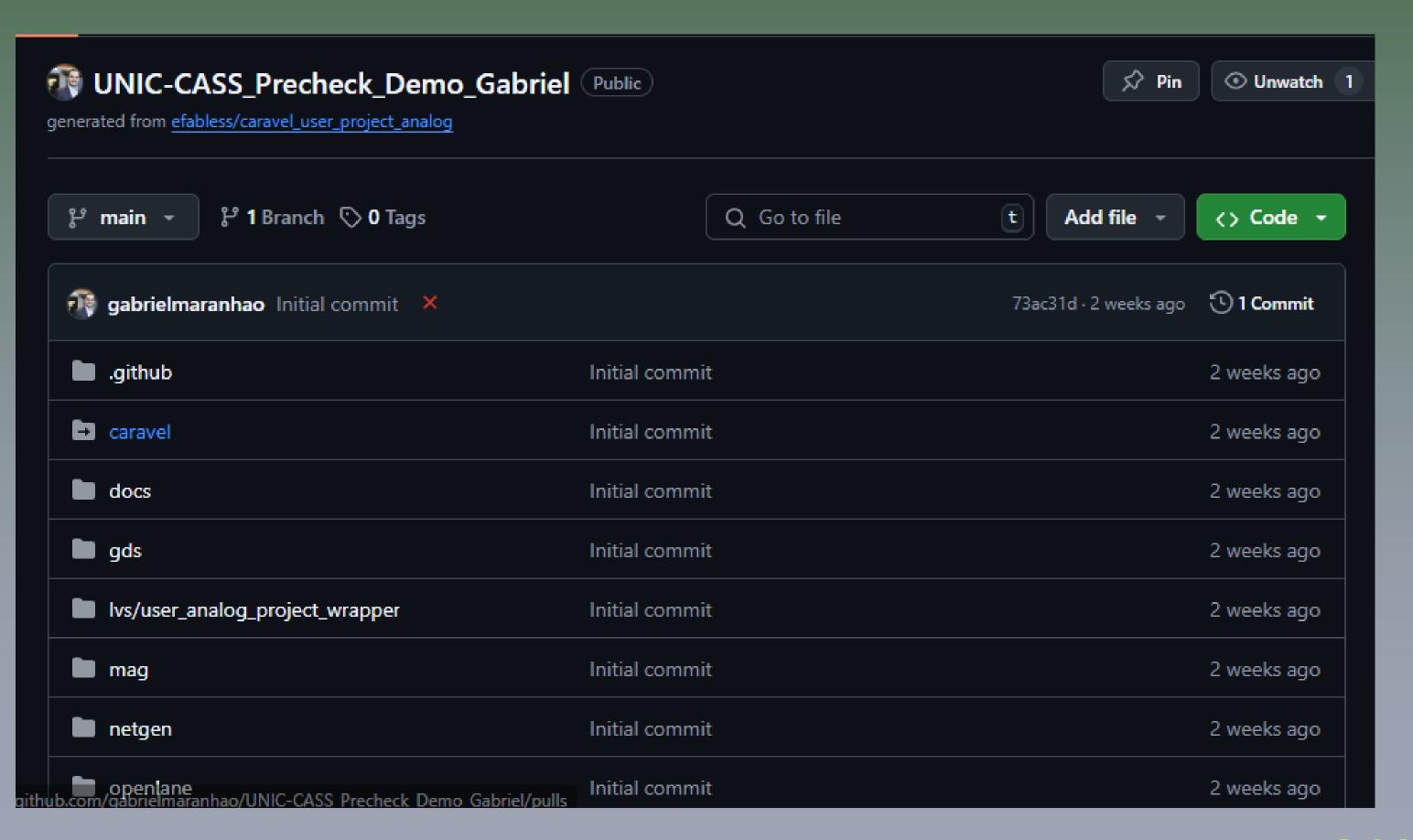
Creating the CARAVEL repository on github

- Click "Use this template", create a name, make it public.
 - https://github.com/efabless/caravel user project analog



Creating the repository on github

Example:



Clone the created github repository to your local PC or JKU (IIC-TOOLS) environment

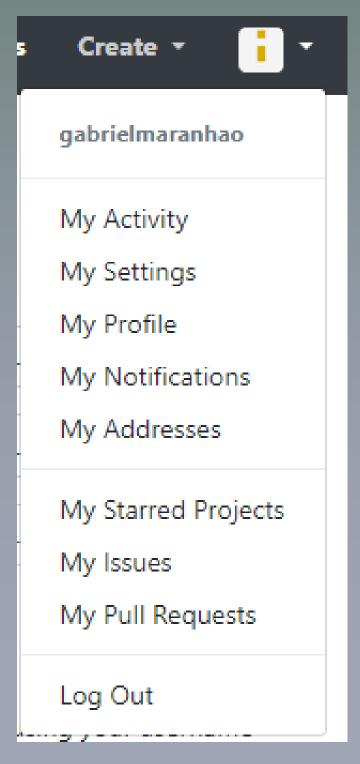
- Clone it using SSH. I recommend to have a SSH for github already created https://github.com/settings/keys
- \$ git clone https://github.com/....
- Make sure to have the environment variables (PDK_ROOT= /pdk/path/sky130)

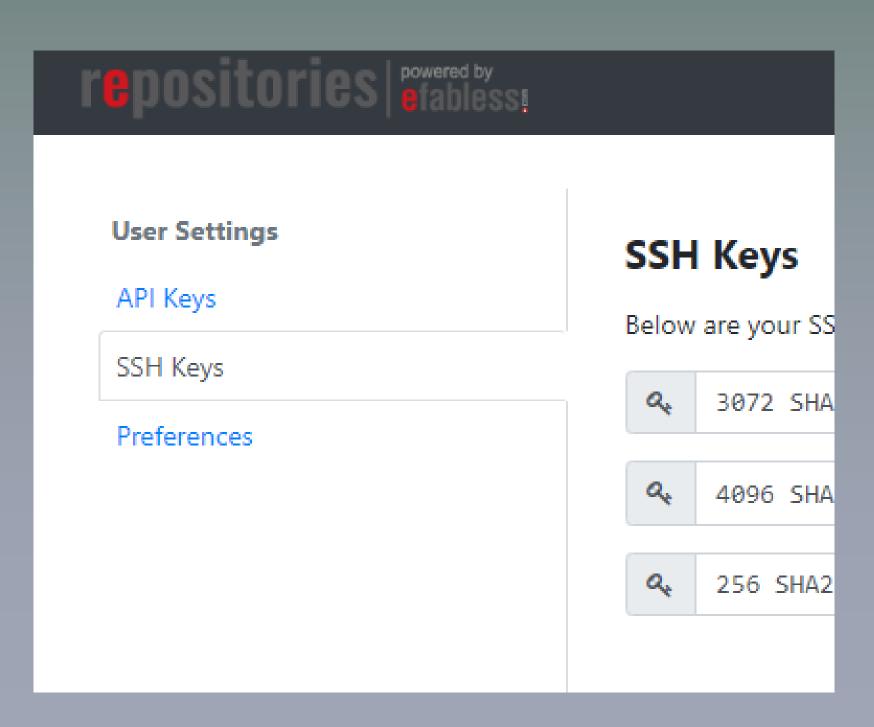
Creating the SSH on Efabless plataform

Make sure to have a efabless profile;

https://repositories.efabless.com/settings Go to Settings -> SSH Keys, follow

the steps.

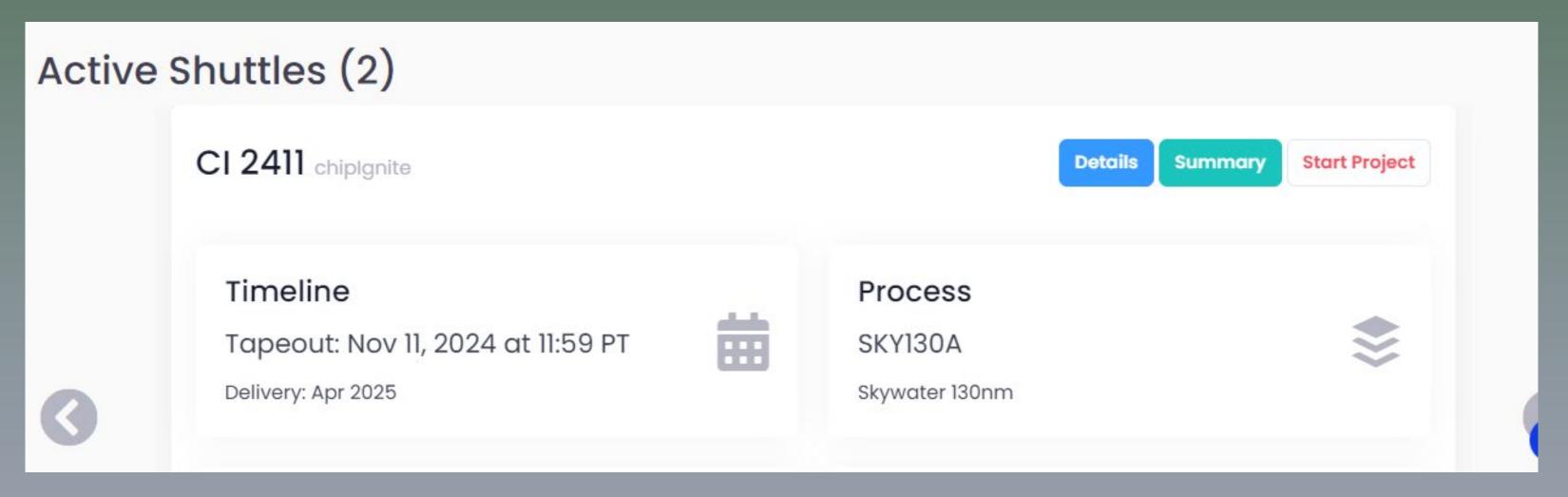




Efabless video tutorial

Create a project on Efabless platform

Go to https://platform.efabless.com/. The shuttle for UNIC-CASS is the CI2411 from the "Active Shuttles";



 Use the "Project Title" as the same name of the github repository (Not mandatory)

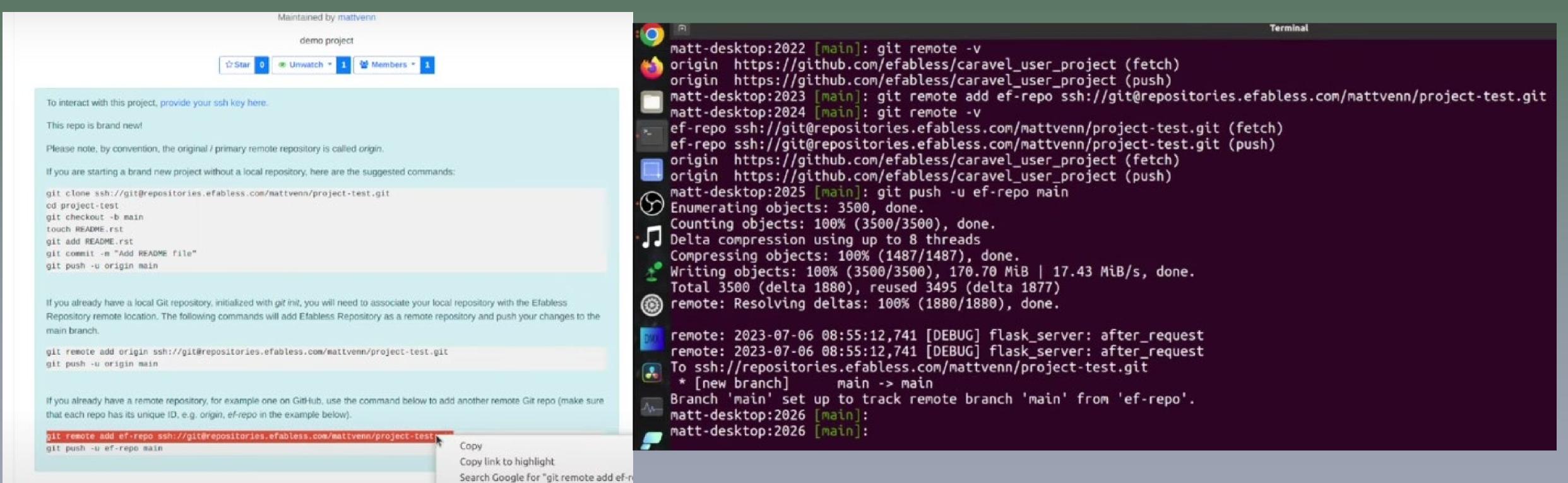
Create a project on Efabless platform

Translate selection to English

Bitwarden

Inspect

Push your github repo to Efabless repo



Check it - Efabless video tutorial

Efabless platform remote Precheck

- Push all the commits, make your repo up to date;
- Go to https://platform.efabless.com/shuttles/CI%202411 (Make sure to be logged)
- Click on "Submit" for "MPW Precheck"
- ▶ Use the commit hash of the last commit as a "Job name"
 - Command to print the last commit hash on your local repo
 - \$ git log -1 --pretty=format:"%H"
- Click "Submit", it takes 10min;
 - It is going to fail (Incomplete) if no changes were made in the repo files, is ok for now.

Local Precheck

- Go into your local repo file (make sure to have the right environment variable PDK_ROOT on this terminal);
- Push all the commits, make your repo up to date;
- Need docker and Klayout to run, see <u>Setup Desktop</u>;
- \$ make precheck (only one time)
- \$ make run-precheck

Mock Tape-out

- Now is time to get a "Complete" on the remote precheck run;
- Important files:
 - xschem/user_analog_project_wrapper.sch (SCHEMATIC)
 - verilog/rtl/user_defines.v (VERILOG)

```
// deliberately erroneous placeholder value; user required to config GPIO's to other
`define GPIO_MODE_INVALID 13'hXXXX

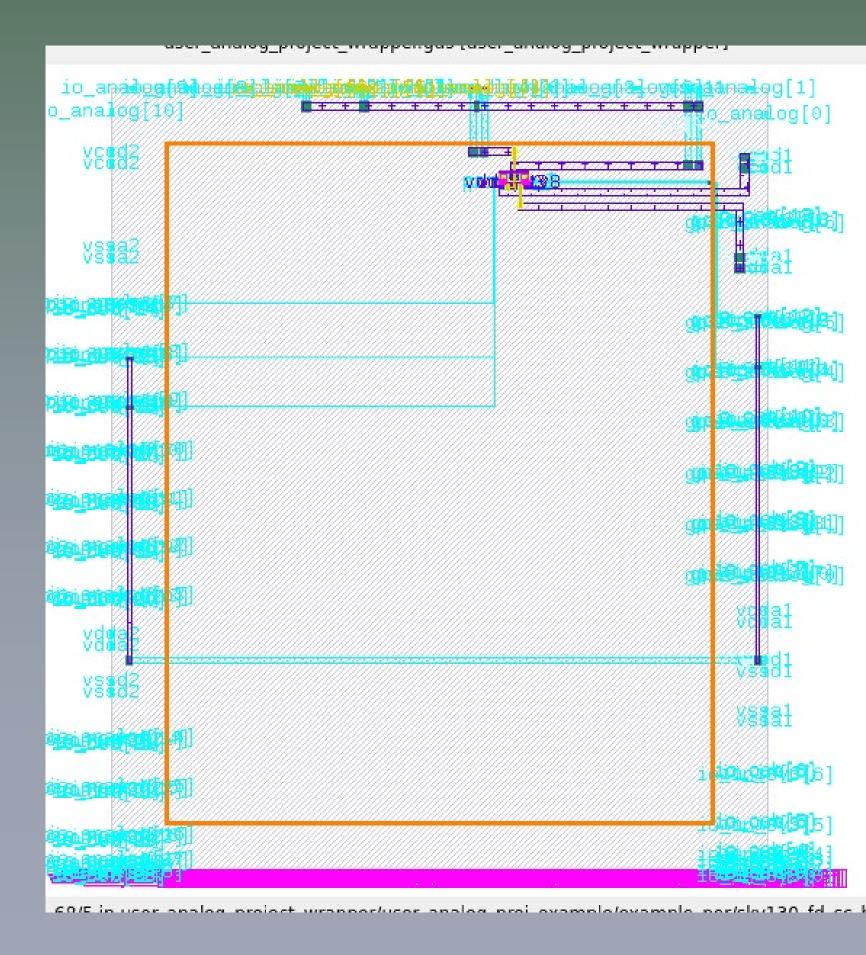
// Authoritive source of these MODE defs is: caravel/verilog/rtl/user_defines.v

// Useful GPIO mode values. These match the names used in defs.h.
//
```

gds/user_analog_project_wrapper.gds (LAYOUT)

Mock Tape-out

- Place your mock/simple layout inside the GDS wrapper (user_analog_project_wrapper.gds)
- This is your user project are
 - Don't rename the files;
 - Make sure to have a LVS clean.
- Edit the user_defines.v file (to fix the GPIO-Defines flag/error)
- Commit and push the updates, run precheck again
 - DRC clean
 - LVS not mandatory.



Observations

- If you created your own schematics files the LVS of the precheck will flag a LVS error.
 - If you want to have a precheck with LVS clear you need to edit the file "user_analog_project_wrapper.sch" and generate a new "user_analog_project_wrapper.spice"
- During the Local precheck, the flag "Default", appears only if either the .gds and the README.md was not modified from the default one.