IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS

CALL for PAPERS

In-Memory Computing (IMC): From Technology to Applications

Guest editors

- Alberto Bosio, Lyon Institute of Nanotechnology, France (Alberto.bosio@ec-lyon.fr)
- Deliang Fan, Arizona State University, USA (dfan@asu.edu)
- Xueqing Li, Tsinghua University, China (xueqingli@tsinghua.edu.cn)
- Leticia Maria Bolzani Poehls, IHP Microelectronics, Germany (poehls@ihp-microelectronics.com)

Scope and purpose

Computer architecture stands at an important crossroad facing several severe challenges. For more than four decades, the performance of computing systems has been improving by 20-50% per year. In the last decade, this number has dropped to less than 7% per year. At the moment, this rate is at the record low of 3% per year. The demand for performance improvement, however, keeps increasing and diversifies its profile. This higher performance often has to come at a lower power consumption cost too, adding to the complexity of the problem.

Both today's computer architectures and device technologies (used to manufacture them) are facing major challenges, making them incapable of delivering the performance required by complex applications, such as Artificial Intelligence (AI). The complexity stems from the extremely high number of operations to be computed and the involved amount of data. The direct consequence is that the computational workload involved in such applications is limited by the well-known walls of actual computing systems: (1) The Memory wall due to the increasing gap between processor and memory speeds, and the limited memory bandwidth making the memory access the performance killer and power drain for memory access dominated applications; (2) The Power wall, concerning the practical power limit for cooling, which means no further increase in CPU clock speed.

Nanoscale CMOS technology, which has been the enabler of the computing revolution, also faces three walls: (1) The Reliability wall as technology scaling leads to reduced device lifetime and higher failure rate, (2) The Leakage wall as the static power is becoming dominant at smaller technologies (due to the volatility technology and lower supply voltages); (3) The Cost wall as the cost per device via pure geometric scaling of process technology is plateauing. All of these have led to the slowdown of the traditional device scaling.

In order for computing systems to continue delivering sustainable benefits for the foreseeable future, alternative computing architectures and paradigms have to be explored in conjunction with emerging device technologies. This Special Issue aims at promoting In-Memory-Computing (IMC) and its applications as a promising solution. In doing so, we consider both well-established memory technologies (such as SRAM, DRAM, and FLASH) that can lead to more immediate solutions, and emerging memory technologies (such as RRAM, PCM, MRAM, and FeFET) that hold the promise for

longer term solutions.

Topics of interest

Topics of interest to this special issue include contributions concerning in-memory computing and applications. More specifically, these may include, but not limited to, the following:

- IMC based systems: architectures, design methodologies and framework, circuits, device modeling;
- Logic and circuit design concepts using memory devices: threshold logic, stateful logic, multi-level logic;
- Conventional and emerging nanoscale device-circuit co-design technologies for IMC: concept, modeling, and circuit demonstration;
- Architecture and system integration of IMC: interconnection, performance analysis, simulation/emulation;
- Test and Reliability for IMC circuits and systems: defect, fault modeling, test generation, DfT and Fault tolerance techniques applied to IMC circuits and systems;
- Security for IMC systems and IMC paradigm for security: threats, attacks and countermeasures for IMC, exploiting IMC paradigm to enhance the security of a computing system;
- Programming models, compilers and paradigms for IMC: code generation and optimization, programming models;
- Applications exploiting IMC from high-performance to edge computing: signal processing, chaos and complex networks, sensory applications, AI applications.

Submission procedure

Prospective authors are invited to submit their papers following the instructions provided on the IEEE JETCAS website: https://ieee-cas.org/publication/JETCAS/manuscript-submission-guide. The submitted manuscripts should not have been previously published, nor should they be currently under consideration for publication elsewhere. The IEEE JETCAS submission site: https://ieee.atyponrex.com/journal/jetcas

Important dates

- **Manuscript submissions due:** **August 31, 2025**
- **First round of reviews completed:** **October 12, 2025**
- **Revised manuscripts due:** **November 23, 2025**
- **Second round of reviews completed:** **December 21, 2025**
- **Final manuscripts due:** **January 11, 2026**

Request for information

Contact the Corresponding Guest Editor: Alberto Bosio (alberto.bosio@ec-lyon.fr)