## VLSI-SoC 2025

October 12-15, 2025 Puerto Varas, Chile





Paper Submission: Papers should present original research and industrial results not published or submitted for publication in other forums. Electronic submission in PDF format to the http://www.vlsi-soc.com website is required. The proceedings will be published by IEEE and available through IEEE Xplore.

A selection of the conference best papers will be invited to submit an extended version to be included as chapters of a book to be published by Springer.

Paper Format: Papers should not exceed 4 pages + a 5th page with only refeernces (single-spaced, 2 columns, 10pt font). Submissions should be in camera-ready, following the IEEE proceedings specifications located at:

http://www.ieee.org/web/publications/pubservices/ confpub/AuthorTools/conferenceTemplates.html

Paper Publication and Presenter Registration: Papers will be accepted for regular or poster presentation at the conference. Every accepted paper MUST have at least one author registered at the conference by the time the camera-ready paper is submitted; the author is also expected to attend the conference and present the paper. A limited number of travel grants are available to needy PhD students. Please see the web site for more information.

VLSI-SoC 2025 is the 33rd in a series of international conferences sponsored by IFIP TC 10 WG 10.5, IEEE CASS, IEEE CEDA and ACM SIGDA, which explores the state-ofthe-art in the areas that surround Very Large Scale Integration (VLSI) and System-on-Chip (SoC). Previous conferences have taken place in Edinburgh, Trondheim, Tokyo, Vancouver, Munich, Grenoble, Gramado, Lisbon, Montpellier, Darmstadt, Perth, Nice, Atlanta, Rhodes, Florianópolis, Madrid, Hong Kong, Santa Cruz, Istanbul, Playa del Carmen, Daejeon, Tallinn, Abu Dhabi, Verona, Cuzco, Salt Lake City, Singapore, Patras, Sharjah, and Tanger. The 2025 edition will take place at Puerto Varas, a tourist and top destination in South Chile, to who likes the beautiful of nature. It is a scenic location close to mountains, lakes, forests and national parks.



- Analog and Mixed-Signal IC Design
- 3-D Integration Physical Design
- Electronic Design Automation
- Variability, Reliability, Fault Tolerance and Test
- Digital Signal Processing and Image Processing SoC Design
   Prototyping, Validation, Verification, Modelling, and Simulation
- Embedded Systems and Processors, Hardware/Software Codesign
- Processor Architectures and Multicore SOCs
  Logic and High-Level Synthesis
- Low-Power and Thermal-aware Design
- Reconfigurable SoC Systems for Energy and Reliability

General Chairs:

- **Green Computing Systems**
- Circuits and Systems for Micro-sensing Applications







Program Chairs:

Special Sessions Chair: Local Arrangement Chair: Publication Chair: Publicity Chair: Finance Chair: PhD Forum Chair: Steering Committee:

Victor Grimblatt, Synopsys, Chile Pierre Emmanuel Gaillardon Ricardo Reis, UFRGS, Brazil Patrick Groeneveld, Stanford University, USA Jorge Marin, AC3E, Chile Carlos Muñoz, UFRO, Chile Carlos Silva-Cardenas, PUCPeru Christian Rojas, USM, Chile Graziano Pravadelli, Univ. Verona, Italy Gonzalo Carvajal, USM, Chile

Manfred Glesner, TU Darmstadt, Germany Matthew Guthaus, UC Santa Cruz, USA Salvador Mir, TIMA. France Ricardo Reis, UFRGS, Brazil Fatih Ugurdag, Ozyegin University, Turkey Graziano Pravadelli, (Chair), University of Verona, Italy Ian O'Connor, ECL, France Masahiro Fujita, University of Tokyo, Japan Ibrahim Elfadel, Khalifa University, UAE Luis Miguel Silveira, INESC ID, Portugal Chi-Ying Tsui, HKUST, Hong Kong, China

www.vlsi-soc.com

**Abstract Submission:** April 18, 2025 April 25, 2025 Paper Submission: April 18, 2025 Special Session Proposal: Notification of Acceptance: June 18, 2025 July 10, 2025 Camera-ready: