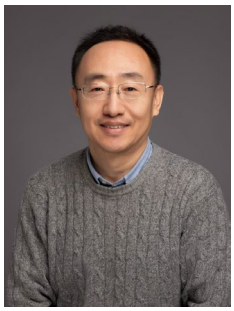
3rd IEEE Circuits and Systems Standard Activities Workshop
25 May 2025 at ISCAS 2025

Speakers and Panelists

Speakers:



Name: Prof Qinfen Hao
Affiliation: Chinese Academy of Science

Topic: The data center interconnect standard development and thinking in an AI era
Abstract: The exponential growth of artificial intelligence (AI) workloads, particularly in large-scale GPU clusters for distributed training and inference, is driving fundamental innovations in chiplet interconnect standards and optical integration strategies within system-on-chip (SoC) architectures. This presentation analyze the reason and necessity of standard effort in data center SoC such as CPU/GPU/Switch, summary the standard development of three critical advancements reshaping data center SoC design include (1) chiplet interconnect, (2) co-packaged optical (CPO) interconnects, and (3) scale-up interconnect between GPUs, finally conclude with some insights into the standardization challenges including technology and interoperability across multi-vendor ecosystems.
Bio: Qinfen Hao obtained his Ph.D. in System Architecture from the Institute of Computing Technology, Chinese Academy of Sciences in 2001. He is currently a Professor at the University of the Chinese Academy of Sciences (CAS) and the Director of the Interconnect Technology Laboratory of the Institute of Computing Technology, CAS. He has pioneered the first teraflops high-performance computers, the first 32-WAY high-end SMP servers, the first cache coherence interconnect chips in SMP server, the first ARM processor in China. He published more than 50 research papers with more 100 granted patents. He has won the second prize of the Chinese National Science and Technology Progress Award twice. He served as General Chair for China Interconnect Technology and Industry Conference, and China Chiplet Developers Conference. He is leading the Chiplet Interface Circuit Standard Development in China and also Chairing the IEEE P3468 Chiplet Interface Circuit Standard Working Group.

Name: Shafi Syed
Affiliation: GLOBALFOUNDRIES

Topic: Hardware Solutions at the heart of eDGE AI
Abstract: The talk presents a holistic approach to energy-efficient, high-performance edge computing and sensor fusion through advanced semiconductor technologies and memory architectures. We showcase the GF 22FDX (Fully Depleted SOI) platform for ultra-low-power logic design, enabling near

threshold operation ideal for always-on AI workloads, with High Performance AI Accelerators, area-scalable compute fabrics, balancing dynamic power savings with leakage mitigation. I introduce embedded non-volatile memory (eNVM) solutions like MRAM (for endurance and near-SRAM speeds) and RRAM (for high-density, low-power storage), paired with In-memory computing architectures by co-locating arithmetic operations within memory arrays. Tightly coupled memory architectures, optimized for FDX platform are analyzed for latency critical interfaces, alongside optimized AI libraries and eNVM's parallelism. The I/O, Connectivity and AutoRadar innovations in FDX address sensor fusion for edge AI under strict power budgets. The talk quantifies trade-offs between area, cost, and speed, emphasizing FDX's simplified BEOL for cost-sensitive edge deployments and RRAM/MRAM's role in minimizing off-chip data transfers. By unifying these advances, I present a framework for edge AI hardware that maximizes speed-per-watt, minimizes footprint, and sustains scalability and real-time responsiveness for applications across industrial IoT, autonomous cars, and wearables.

Bio: Shafi Syed is a seasoned Technical Leader with a strong background in Automotive, IoT and Smart Phone Integrated Circuit designs. With experience working at GLOBALFOUNDRIES, Motorola, and Qualcomm, he has successfully contributed to the launch of more than 3.5 billion ICs in various products over the last 25 years. Shafi holds an MBA in Management & Finance from the University of Florida, as well as an MS in Electrical Engineering from the same University. He holds over 15 design and technology patents and has published 20+ peer-reviewed Tier 1 conference papers. Shafi has also been working with eco-system partners and government research institutions on AI Driven Design Methodologies for RF ICs. Throughout his career, Shafi has demonstrated expertise in design, architecture and system analysis for applications including IoT protocols like Cat-M1, NB-IoT, BLE and WiFi, UWB, 5G mmWave and Automotive Radar applications. Currently, as a Senior Director, Design Engineering at Global Foundries, Shafi manages the global reference circuit design team working on Digital SoC, Analog and RF/mmWave applications for Automotive SoC, IoT edge AI, ADAS, SatCom and cellular subsystems.=
In addition to his design accomplishments, Shafi has significant experience in engineering management, factory and manufacturing operations interface, RF test and certification processes, and risk assessment and communication. He brings an in-depth understanding of the wireless and RF semiconductor markets, blending deep technical expertise with strategic business insight.

Panelists:

Name: Ayan Datta
Affiliation: Western Digital

Bio: Ayan has an overall 16+ years of industry experience in the VLSI domain. He is currently working as a technologist in Sandisk, where he is spearheading the next-gen methodology development team, which works on developing advanced digital design methodology on Ultra Deep Submicron nodes. Before joining Sandisk, he lead the timing convergence of digital design in High-Performance Intel Cores. He also led the development of several PPA design optimization tools, which were deployed across multiple projects at Intel. Before joining Intel he worked in IBM Labs for 8 years on high-performance processors designs after completing his master's degree from Jadavpur University, Kolkata. He is a Senior IEEE member and has close to 13 Publications in Leading IEEE conferences/journals and 6 US Patents. He is currently the Vice Chair of Industry Engagement of the IEEE CAS Bangalore Section. He has been part of several organizing conference committees, including VLSID, and also chaired many sessions at conferences.

Name: Alan Wong
Affiliation: Ensilica

Bio: Alan is currently Senior Vice President of Engineering at EnSilica plc. based in Oxford UK, where he leads the design and volume supply of high-reliability ASICs for RF, communications, sensing and control applications.
He has more than 25 years of experience in semiconductor development, initially in technical positions at Tokyo Electron and Sony Semiconductor, and then as IC Design Director at Frontier Microsystems & Toumaz Ltd, where he led the design and delivery of wireless SoC products for medical and consumer markets.
Alan is a Chartered Engineer, MIET, Senior member IEEE, and served as TPC member for ISSCC (EU & Wireless) and on IEEE802 standards committee.
Alan graduated in Engineering from the University of Oxford, and has published work in IEEE JSSC, ISSCC, MTTS-RFIC Symposium focussed on RF and mmWave silicon circuit design.

Name: Tian Dong
Affiliation: InterDigital

Bio: Dong Tian (Fellow, IEEE) is currently a Senior Director with InterDigital, Inc., New York, NY, USA. He serves as the Chair of IEEE CASS MSA TC, MPEG-AI, MPEG AI-Based PCC. He was an Associate Editor for IEEE Transactions on Image Processing from 2018 to 2021, a General Co-Chair of MMSP'20 and MMSP'21, and the TPC Chair of MMSP'19. Prior to InterDigital, Inc., he was a Senior Principal Research Scientist at MERL, Cambridge, MA, USA, from 2010 to 2018, a Senior Researcher with Thomson Corporate Research, Princeton, NJ, USA, from 2006 to 2010, and a Visiting Researcher at Tampere University of Technology (TUT) from 2002 to 2005. He holds numerous U.S.-granted patents and publications in top-tier journals/transactions and conferences. His research interests include image processing, 3D video, point cloud processing, and deep learning. He is an Advisor Member of IEEE MMSP TC. He received the B.S. and M.Sc. degrees from the University of Science and Technology of China (USTC), Hefei, China, in 1995 and 1998, respectively, and the Ph.D. degree from Beijing University of Technology, Beijing, in 2001.

Name: Zhou Peng
Affiliation: LuxiTech

Bio: Dr. Peng Zhou received her bachelor's degree from the School of Artificial Intelligence and Automation at Huazhong University of Science and Technology and earned her Ph.D. from the Department of Electrical and Computer Engineering at the University of California, Santa Cruz. She co-founded and served as CTO of LuxiTech, a company focused on brain-inspired and efficient large language models, and has since held a postdoctoral position at City University of Hong Kong. Her research interests include neuromorphic computing, memristors, spiking neural networks, and large language models, in which she has published many papers and patents. She is a member of the IEEE CAS Technical Committees on Neural Systems and Applications (NSA) and Cellular Nanoscale Networks and Memristor Array Computing (CNN-MAC). Dr. Zhou serves as a program committee member, review committee member, and session chair for conferences including NeurIPS, IEEE ISCAS, ICONS, and ICNC, etc, and is a reviewer for IEEE TCAS-I, TBioCAS, NeurIPS, ICLR, etc. She has received awards including Best New Neuromorph at the Telluride Workshop and the IEEE CAS Darlington Best Paper Award. Dr. Zhou is also a member of the United Nations STEM4ALL STEMinist network, actively participating in discussions on women in technology and policy-making, and she has contributed to the development of national AI standards including those related to generative AI and neuromorphic chip.

Panelist Moderator

Name: Ahmed Madian
Affiliation: Nile University, Egypt
Bio: Ahmed Madian (SM'12) is currently a Professor and director for Electronics and Computer Engineering Program, Faculty of Engineering and Applied Science, NILE University, Giza, Egypt on leave from the Egyptian Atomic Energy Authority. He is the former director of Microelectronics System Design Master Program from 2015 -2020. Also, He has been the director of Nanoelectronics Integrated System Design Research Center (NISC) since 2016 -2023. He has published more than 200 papers in international conferences and journals with h-index 30. Also, he served on the many technical and organizing committees of many international conferences. He received many research grants as Principal Investigator (PI), CO-PI, or Consultant from different national/international organizations. Also, he is a member of the National Radio of Science Committee (NRSC), ASRT since 2018-now. He is a member of the Information Technology and Communication Council, ASRT from 2021 to now. Dr. Madian is senior member IEEE. He is currently the IEEE Egypt Section chair and served as the IEEE Egypt section secretary/conference coordinator and member of the ExCom from 2020 – 2023. He served as technical program co-chair of many IEEE international conferences and as organizing committee of many IEEE events and student's competition. He is a member of the steering committee of many IEEE conferences. He served in the higher council of Communication and Information Technology, Egyptian Academy for Science, research, and Technology (ASRT). He has been elected as a voting member of IEEE CASS Standards Activities subdivision. He organized many awareness sessions for proposal writing and fundraising for different IEEE units.
* Dr. Madian won the Best Researcher award (Dr Hazem Ezzat Award 2017) for his outstanding research profile and El-Shorouk Academy Award for Scientific and Technological Creativity 2020 winner.
* He is a co-founder of the IEEE Robotics and Automation Egypt chapter which won the Chapter of the Year Award region 8 for 2012.
* He is also the founder of IEEE CASS technical chapter Egypt section won the Chapter of the Year Award Region 8 for 2023 and won IEEE-CASS outreach for many years.
* He is the IEEE African Council Treasure 2024-2025.
* Finally, he has been selected as Distinguished Lecturer for the Circuits and Systems Society (CASS) 2024-2025.