



UNIVERSIDAD TECNICA
FEDERICO SANTA MARIA



AC3E

Advanced Center for Electrical
and Electronic Engineering

Introduction to the Opensource Analog Design Flow

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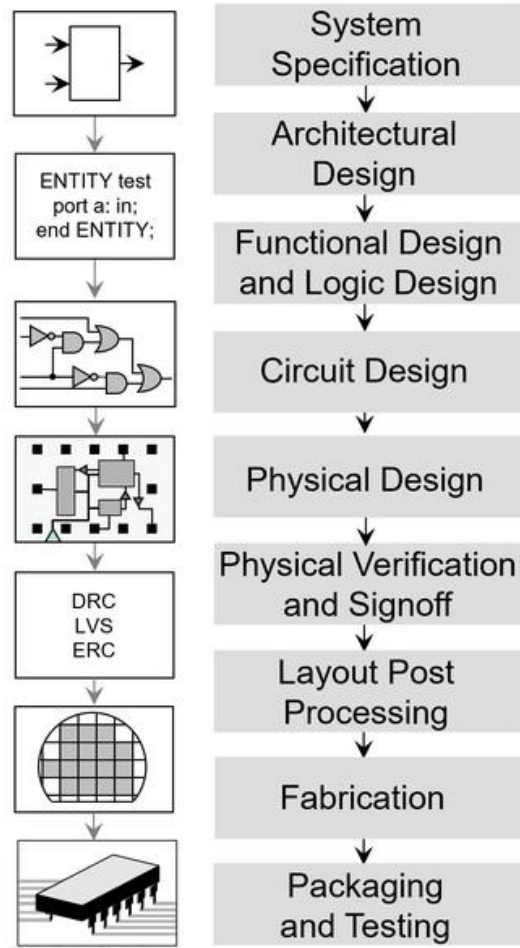


INTRODUCTION

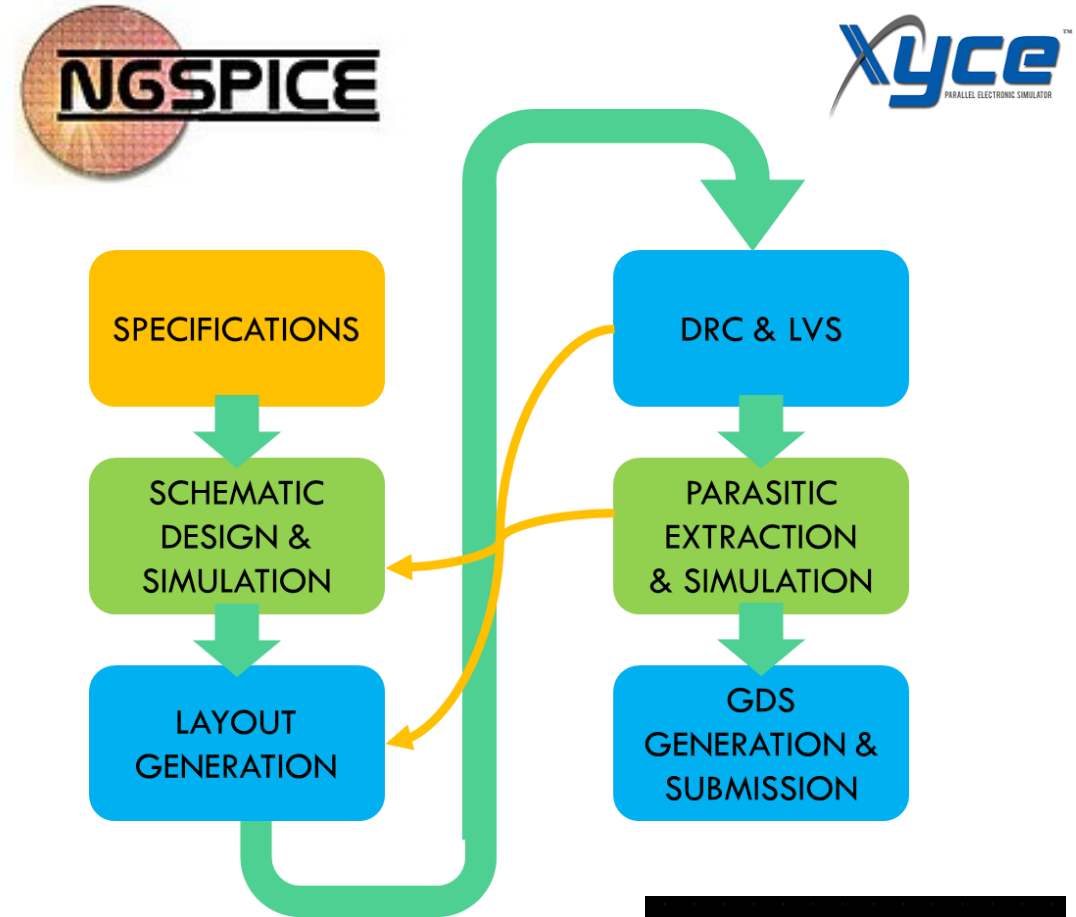
Analog vs digital design flows

OPENSOURCE EDA TOOLS

DIGITAL FLOW



ANALOG FLOW

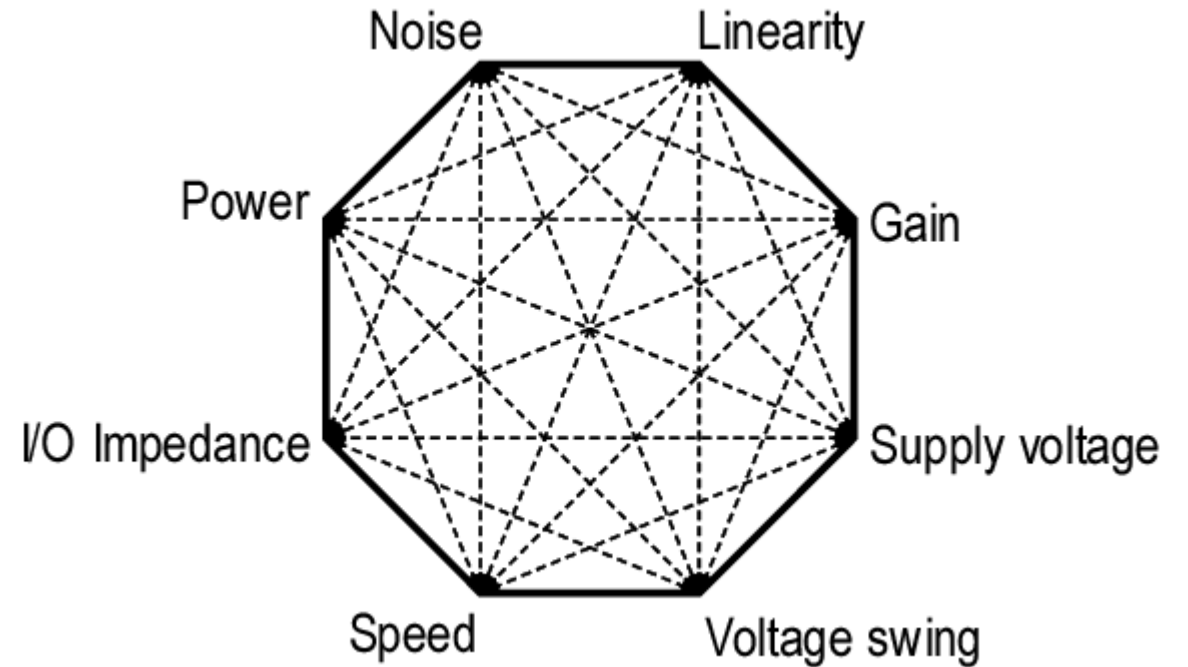
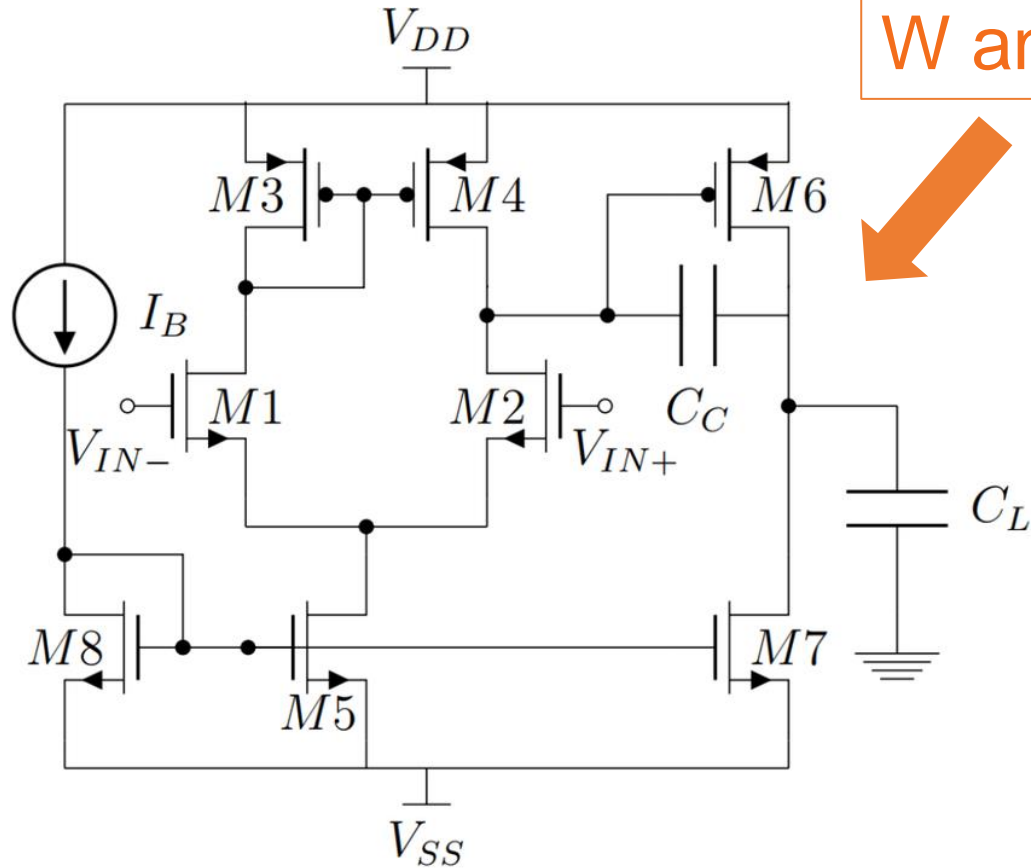


Magic VLSI Layout Tool
Current distribution version 8.2

XSCHEM

Tradeoffs in analog design

W and L for each transistor M1 to M8?



[B. Razavi]

Analog block example: Miller OTA

Performance is limited by the tradeoff in target specifications



**BASIC USE OF
ANALOG TOOLS**

How to get started with design and simulation?

- Environment setup

- Option 1: Analog Mixed Signal Design using docker image & remote desktop

- e.g. IIC-OSIC-TOOLS docker

- Clone at: <https://github.com/iic-jku/iic-osic-tools>

- Follow detailed instructions

- Option 2: Analog Mixed Signal Design tools on Linux or WSL using Conda

See the environment setup material in the UNIC-CASS page: <https://unic-cass.github.io/02-env-setup.html>

- Relevant tools
 - Xschem → schematic entry and netlist generation
 - Ngspice → simulation based on netlist generated by Xschem
- Visualization
 - Ngspice window → quick checks
 - GAW → integrated in Xschem
 - External viewer through raw data (e.g. Python script)

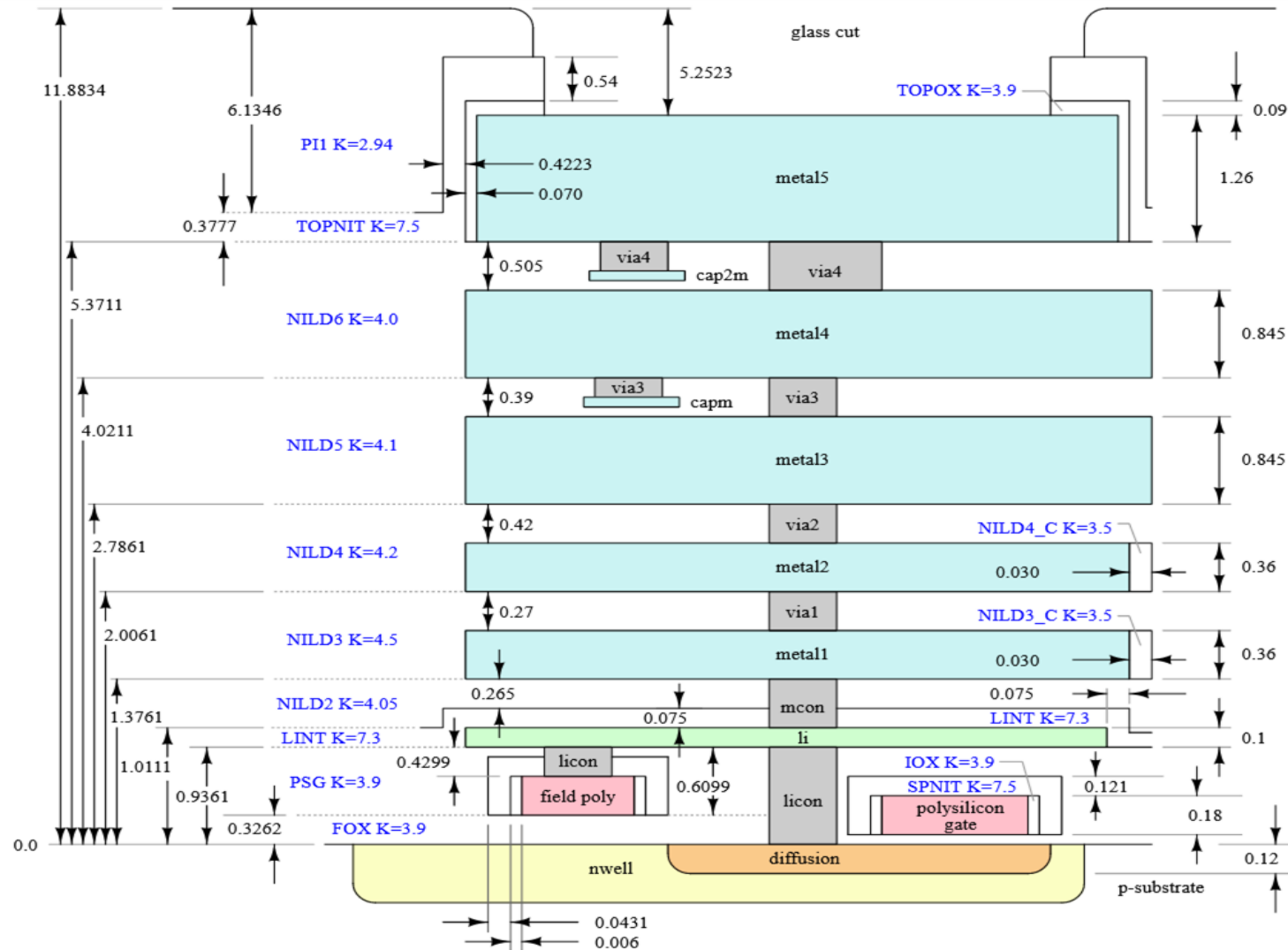


- Simulation types
 - DC → operating point
 - AC → frequency sweep
 - Transient → time-domain behavior
 - Noise → simulation of device intrinsic noise
 - And others...

Ngspice manual will become your best friend!
<https://ngspice.sourceforge.io/docs/ngspice-manual.pdf>



Available devices in SKY130



Device Details

1.8V NMOS FET

Spice Model Information

- Cell Name: sky130_fd_pr_nfet_01v8
- Model Name: sky130_fd_pr_nfet_01v8

Operating Voltages where SPICE models are valid

- $V_{DS} = 0$ to 1.95V
- $V_{GS} = 0$ to 1.95V
- $V_{BS} = +0.3$ to -1.95V

Explore

www.skywater-pdk.readthedocs.io

for device info

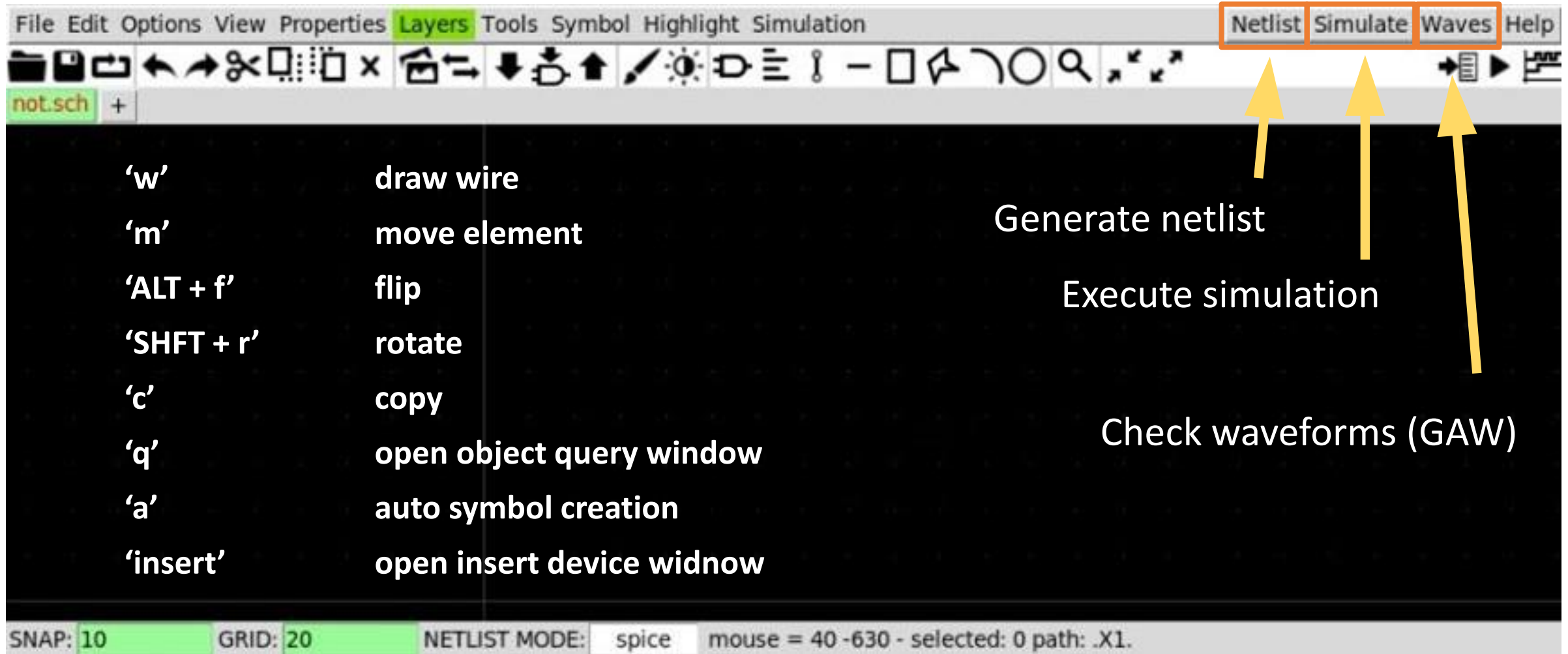
SPICE models inside IIC-OSIC-TOOLS docker:

```
.lib /foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice tt
```

Single-transistor DC simulation

For more detailed explanations, explore:
<https://unic-cass.github.io/03-analog-design-flow.html#3-analog-design-flow-with-opensource-tools>





The screenshot shows the Xschem GUI interface. The menu bar at the top includes 'File', 'Edit', 'Options', 'View', 'Properties', 'Layers', 'Tools', 'Symbol', 'Highlight', 'Simulation', 'Netlist', 'Simulate', 'Waves', and 'Help'. The 'Netlist', 'Simulate', and 'Waves' menus are highlighted with orange boxes, and yellow arrows point from text labels to these menus. Below the menu bar is a toolbar with various icons. The main workspace is dark and contains a table of keyboard shortcuts. At the bottom, a status bar shows 'SNAP: 10', 'GRID: 20', 'NETLIST MODE: spice', and 'mouse = 40 -630 - selected: 0 path: .X1.'.

'w'	draw wire
'm'	move element
'ALT + f'	flip
'SHFT + r'	rotate
'c'	copy
'q'	open object query window
'a'	auto symbol creation
'insert'	open insert device widnow

Generate netlist

Execute simulation

Check waveforms (GAW)

- Nominal

Ideal simulation without considering many fabrication effects

- P(VT) corners

Considers global process variation (P) and environment (V, T)

```
.lib /foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice tt
```

- Mismatch

Considers local statistical variation among devices

→ See: section 7.7 in <https://unic-cass.github.io/07-design-examples.html>

- Parasitic extraction/ post layout simulations

Components associated to extrinsic structures (metallization)

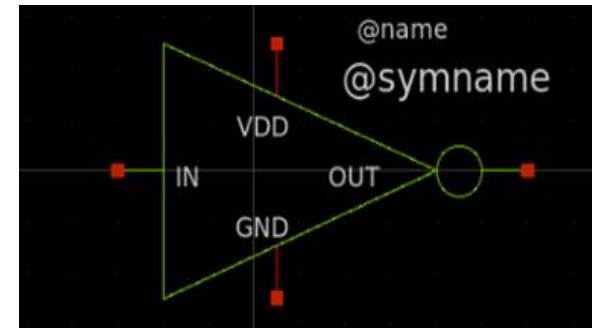
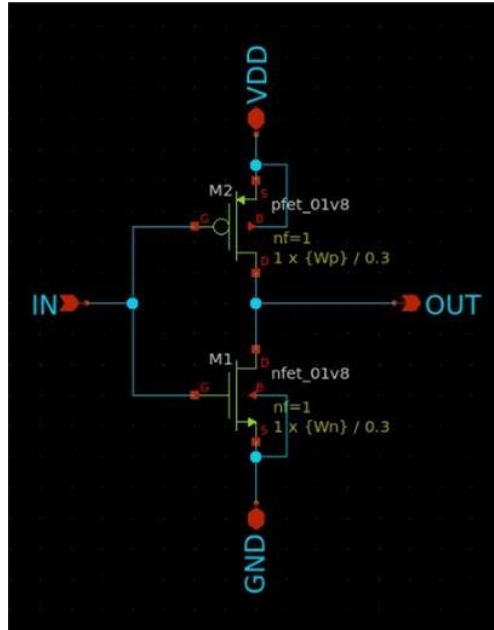
A photograph of an AC3E inverter board with a semi-transparent orange overlay. The board features a large electrolytic capacitor, a transformer, and various electronic components. A white box highlights the central area. The board is labeled with 'AC3E', 'FORMERLY', and 'PHILIPPINES R-25222'. A test point table is visible on the board.

INVERTER EXAMPLE

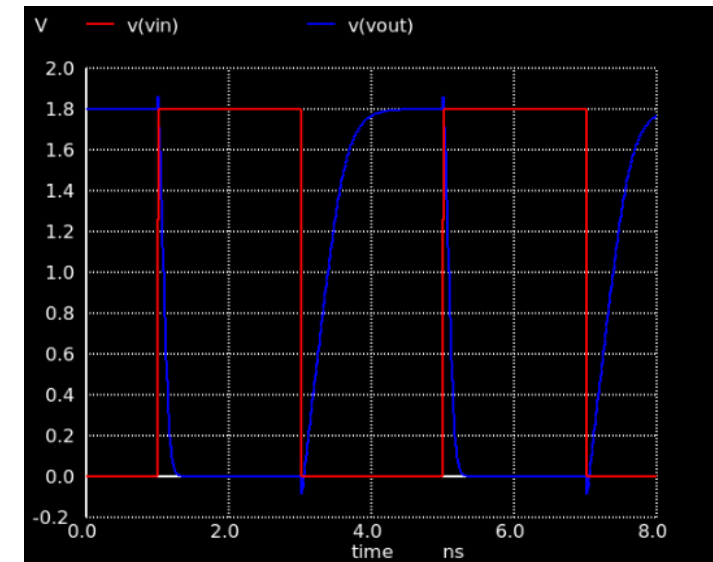
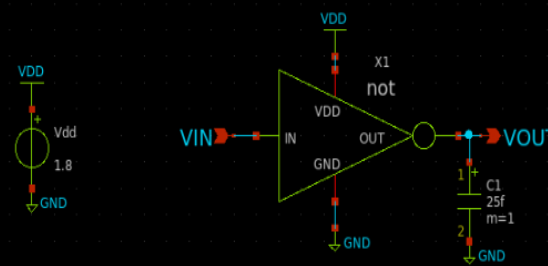
Test points:

TP1-TP2:	1in-tr afo
TP1-TP3:	1out-tr afo
TP2-TP4:	1out-tr afo
TP3-TP5:	1out-tr afo
TP4-TP6:	1out-tr afo
TP5-TP7:	1out-tr afo
TP6-TP8:	1out-tr afo
TP7-TP9:	1out-tr afo
TP8-TP10:	1out-tr afo
TP9-TP11:	1out-tr afo
TP10-TP12:	1out-tr afo
TP11-TP13:	1out-tr afo
TP12-TP14:	1out-tr afo
TP13-TP15:	1out-tr afo
TP14-TP16:	1out-tr afo
TP15-TP17:	1out-tr afo
TP16-TP18:	1out-tr afo
TP17-TP19:	1out-tr afo
TP18-TP20:	1out-tr afo
TP19-TP21:	1out-tr afo
TP20-TP22:	1out-tr afo
TP21-TP23:	1out-tr afo
TP22-TP24:	1out-tr afo
TP23-TP25:	1out-tr afo
TP24-TP26:	1out-tr afo
TP25-TP27:	1out-tr afo
TP26-TP28:	1out-tr afo
TP27-TP29:	1out-tr afo
TP28-TP30:	1out-tr afo
TP29-TP31:	1out-tr afo
TP30-TP32:	1out-tr afo
TP31-TP33:	1out-tr afo
TP32-TP34:	1out-tr afo
TP33-TP35:	1out-tr afo
TP34-TP36:	1out-tr afo
TP35-TP37:	1out-tr afo
TP36-TP38:	1out-tr afo
TP37-TP39:	1out-tr afo
TP38-TP40:	1out-tr afo
TP39-TP41:	1out-tr afo
TP40-TP42:	1out-tr afo
TP41-TP43:	1out-tr afo
TP42-TP44:	1out-tr afo
TP43-TP45:	1out-tr afo
TP44-TP46:	1out-tr afo
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TP400-TP402:	1out-tr afo
TP401-TP403:	1out-tr afo
TP402-TP404:	1out-tr afo
TP403-TP405:	1out-tr afo
TP404-TP406:	1out-tr afo
TP405-TP407:	1out-tr afo
TP406-TP408:	1out-tr afo
TP407-TP409:	1out-tr afo
TP408-TP410:	1out-tr afo
TP409-TP411:	1out-tr afo
TP410-TP412:	1out-tr afo
TP411-TP413:	1out-tr afo
TP412-TP414:	1out-tr afo
TP413-TP415:	1out-tr afo
TP414-TP416:	1out-tr afo
TP415-TP417:	1out-tr afo
TP416-TP418:	1out-tr afo
TP417-TP419:	1out-tr afo
TP418-TP420:	1out-tr afo
TP419-TP421:	1out-tr afo
TP420-TP422:	1out-tr afo
TP421-TP423:	1out-tr afo
TP422-TP424:	1out-tr afo
TP423-TP425:	1out-tr afo
TP424-TP426:	1out-tr afo
TP425-TP427:	1out-tr afo
TP426-TP428:	1out-tr afo
TP427-TP429:	1out-tr afo
TP428-TP430:	1out-tr afo
TP429-TP431:	1out-tr afo
TP430-TP432:	1out-tr afo
TP431-TP433:	1out-tr afo
TP432-TP434:	1out-tr afo
TP433-TP435:	1out-tr afo
TP434-TP436:	1out-tr afo
TP435-TP437:	1out-tr afo
TP436-TP438:	1out-tr afo
TP437-TP439:	1out-tr afo
TP438-TP440:	1out-tr afo
TP439-TP441:	1out-tr afo
TP440-TP442:	1out-tr afo
TP441-TP443:	1out-tr afo
TP442-TP444:	1out-tr afo

Simple inverter example (to be used in Layout later)



```
NGSPICE
""
.lib /foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice tt
vin VIN 0 PULSE(0 1.8 1ns 0ns 0ns 2ns 4ns)
.control
save all
tran 0.01n 8n
plot V(VIN) v(VOUT)
meas tran tpHL_in FIND time WHEN v(VIN)=0.9 TD=0 FALL=1
meas tran tpHL_fin FIND time WHEN v(VOUT)=0.9 TD=0 RISE=1
print tpHL_fin - tpHL_in
.endc
""
```





Other resources

Analog flow tutorial for
main flow (in Spanish
with subtitles)



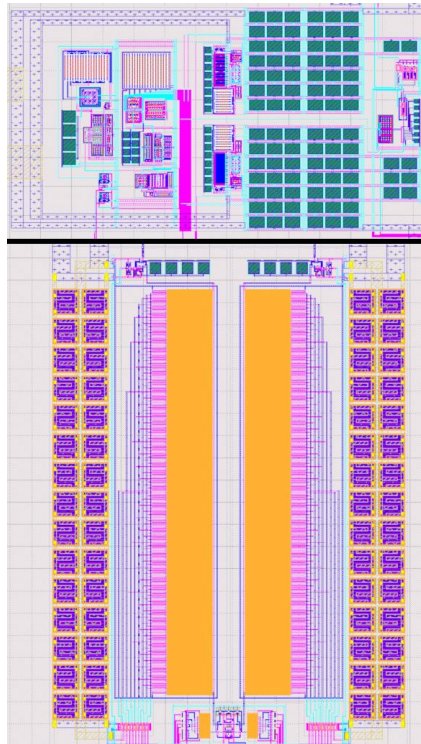
Link: <https://www.youtube.com/watch?v=6NEOxb7CF6A>



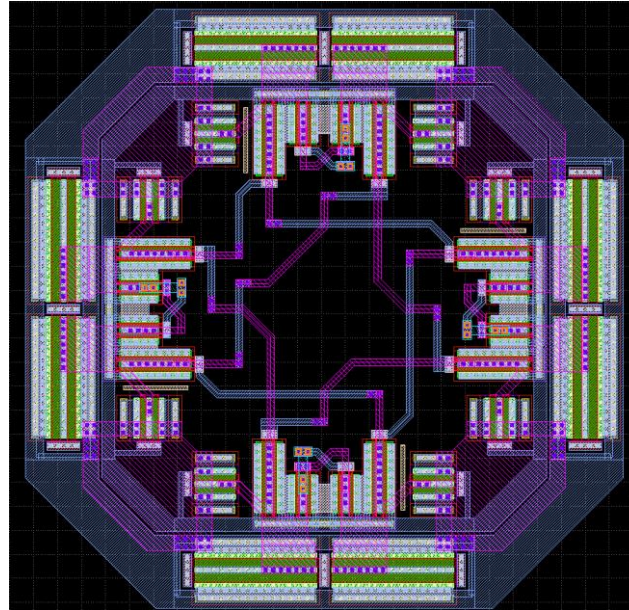
Opensource designs → re-use and get inspired

Visit: <https://platform.efabless.com/projects/public>

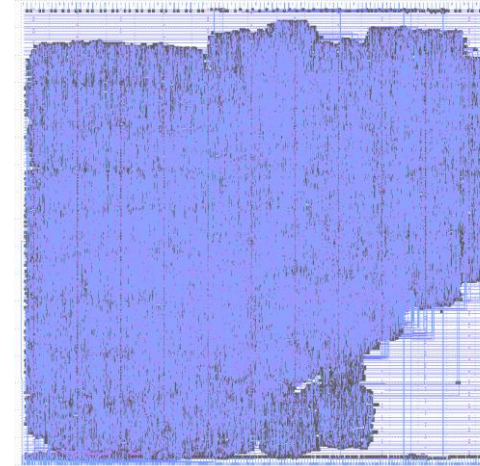
SAR ADC



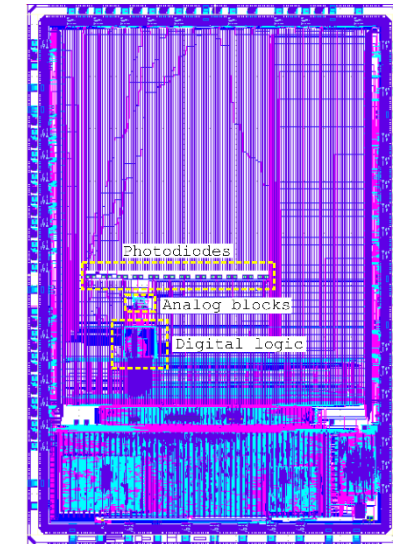
Satellite transceiver



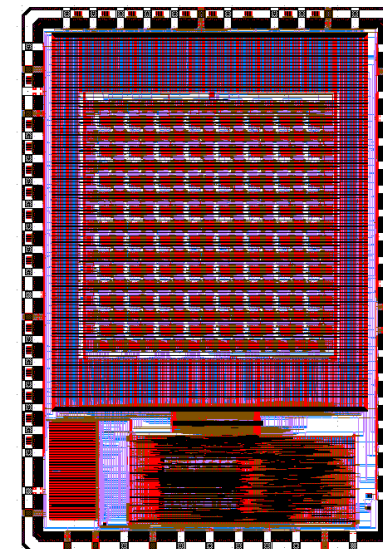
Sudoku Accelerator



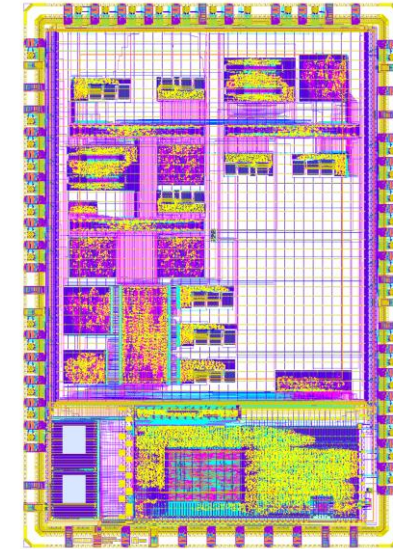
MixPix



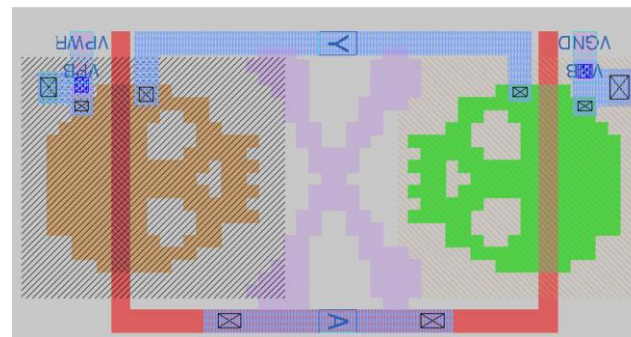
OpenFPGA



Time to Data Converter

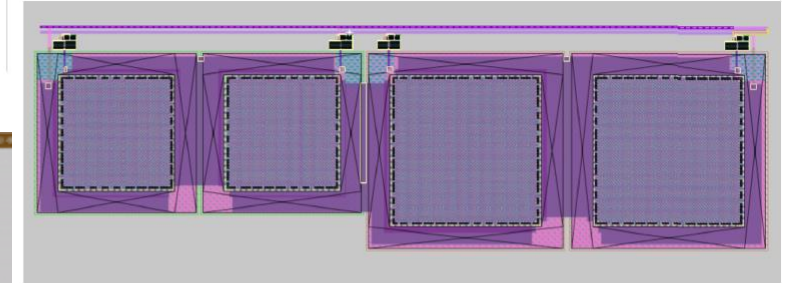
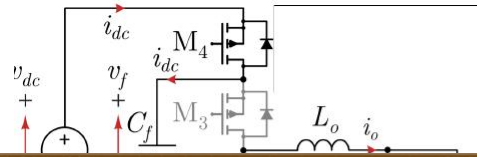
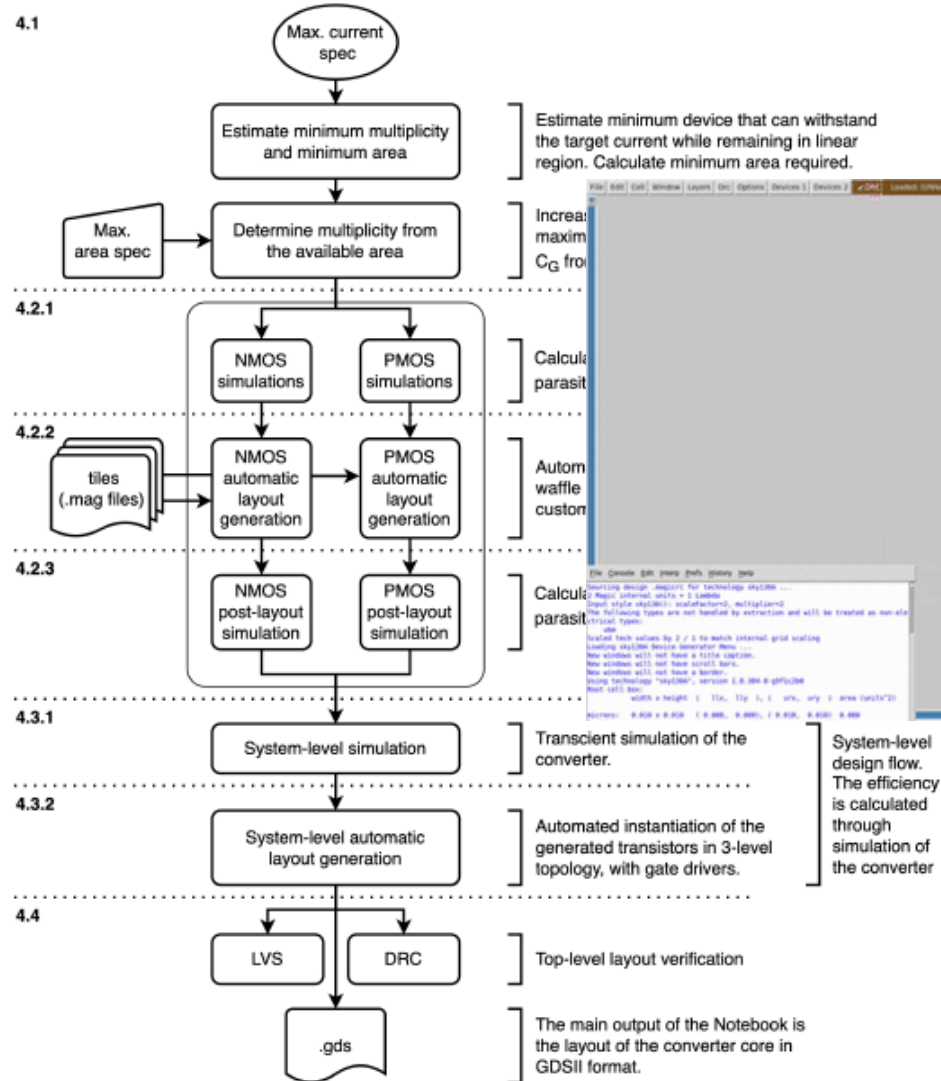


Logic inverter

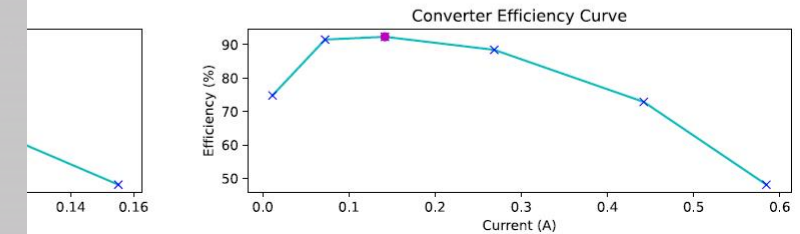


Code-a-chip automated power IC specs-to-GDS flow

https://github.com/sscs-ose/sscs-ose-code-a-chip.github.io/tree/main/VLSI23/accepted_notebooks/3LFCC



Converter schematic (left) and layout (right)



- Full Python-based automated flow using open-source toolkit
- From current, voltage, area and frequency specs to manufacturable layout (GDS file)



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Thank you



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