Design of DTC-Assisted High Performance Fractional-N PLLs

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2024/11/10

Outline

- Fractional-N PLL Design Challenges
- PLL Architecture Review
- DTC-Assisted Phase Detector Design
- Digital Calibrations to Enhance PLL Performance
- LO Chain Design Example for 5G NR

Demand for Low Jitter Fractional-N PLLs

Latest wireless standards strive for very high throughput

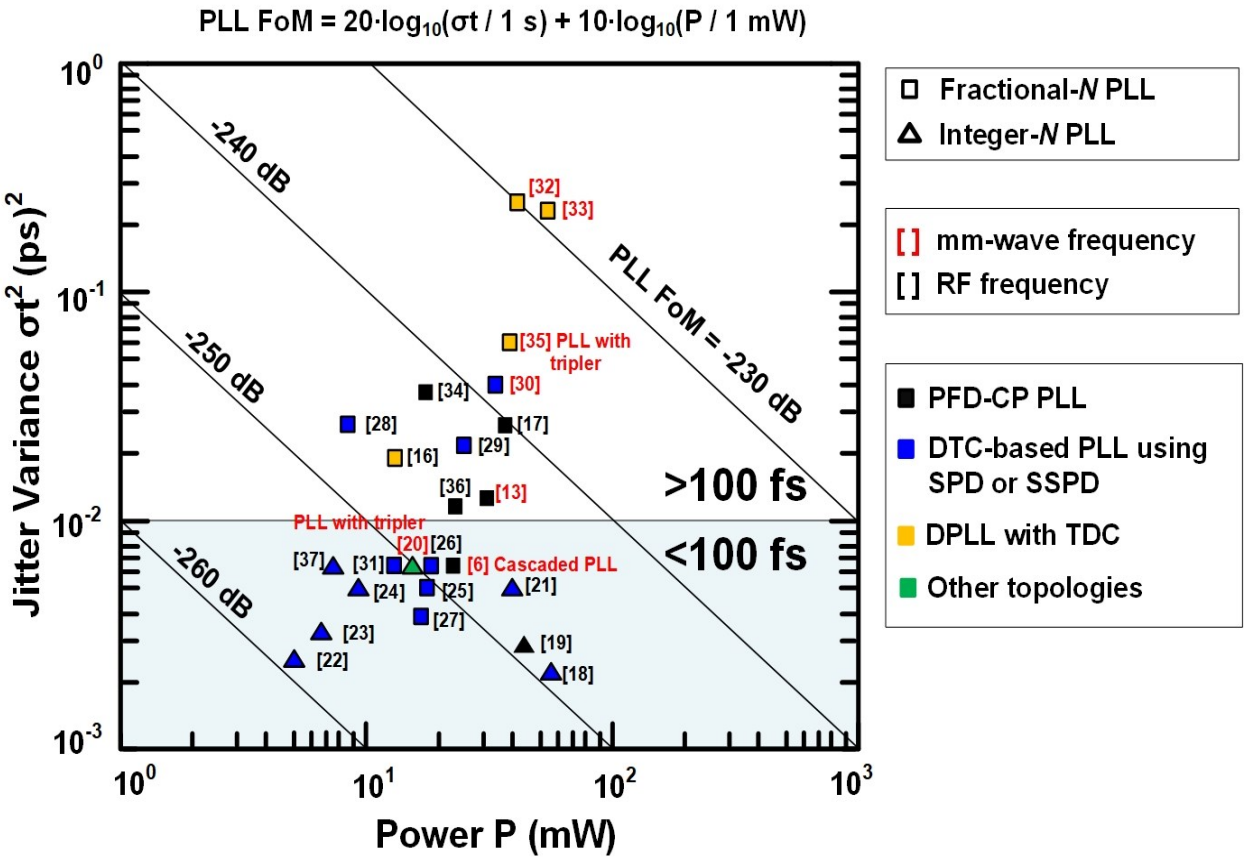
- **WiFi 7 enables 4k-QAM at 7GHz**
- **Cellular FR2 (MMW) transceivers to support 256-QAM at 40+ GHz**

→ RMS jitter <100fs is required for LO

DSB IPN Requirement (dBc)		Integrated RMS jitter (fs) (Int. 1kHz to 100MHz)				
		29.5GHz	40GHz	43GHz	47GHz	7.125GHz
64-QAM	-30	171	126	117	107	707
256-QAM	-33	121	89	83	76	500
1K-QAM	-44	NA	NA	NA	NA	141
4K-QAM	-47	NA	NA	NA	NA	99.8

State-of-the-Art Low Jitter Fractional-N PLLs

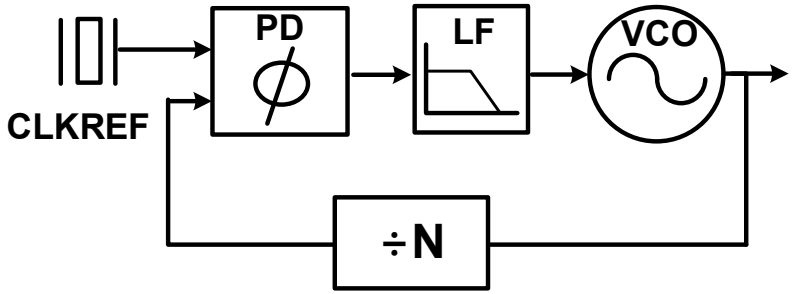
- A few frac. N PLLs achieved <100fs$_{rms}$ jitter; FoM is still worse than integer-N PLLs
- Even harder for mmW PLLs due to mmW VCO
- Analog/digital PLLs using DTC-assisted PD achieves lower jitter and better FoM

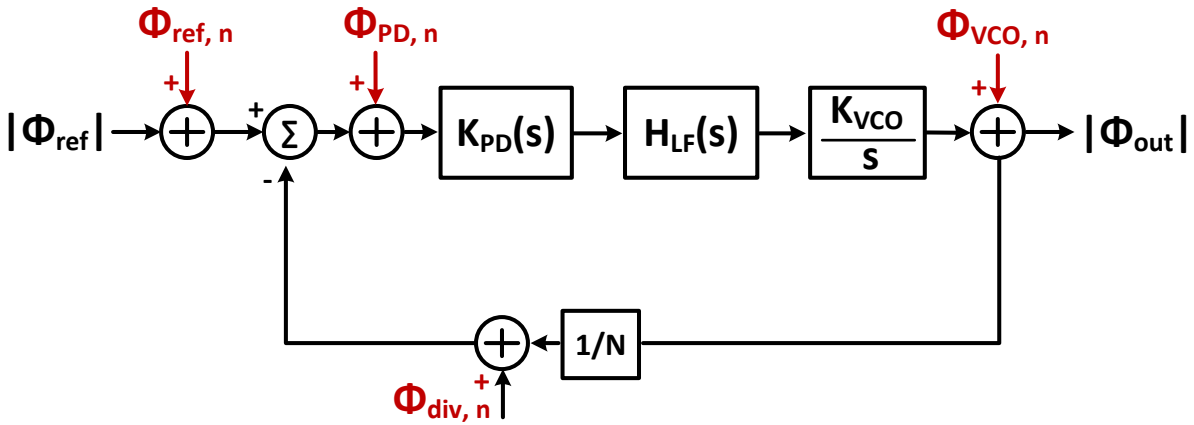


Major Noise Source in Any PLLs

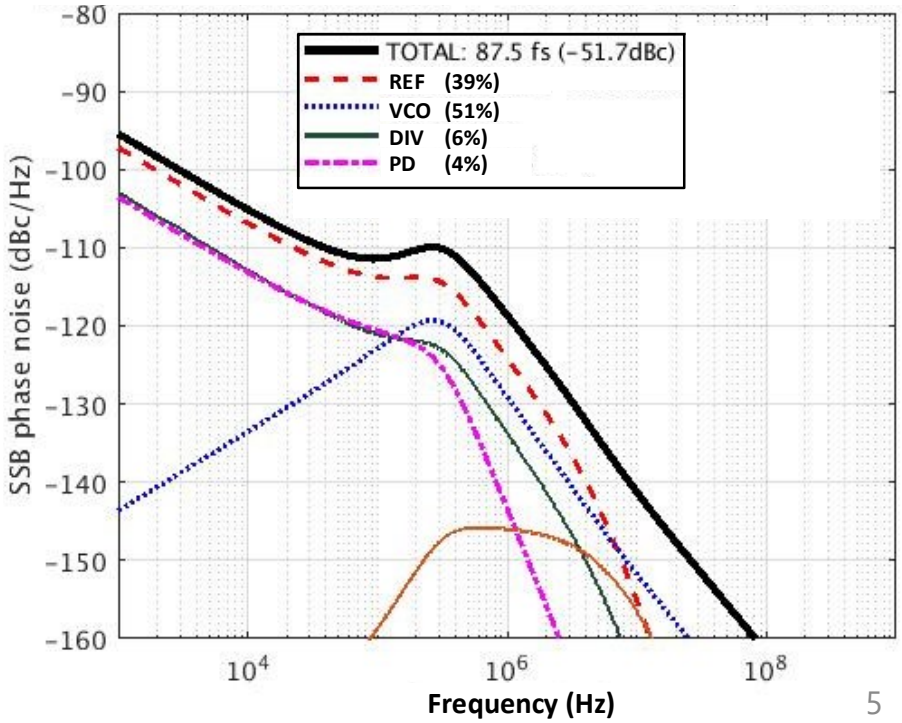
- **Major noise source in a PLL**
  - **VCO/DCO**
  - **CLKREF**
  - **Phase detector (PD) → try to minimize**
  - **Feedback divider → negligible**

→ **Dominate**

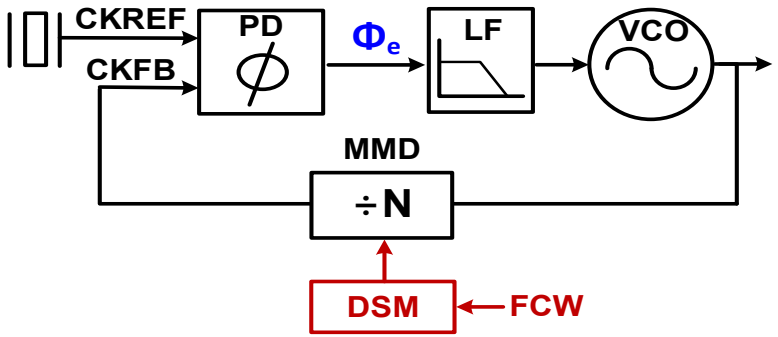


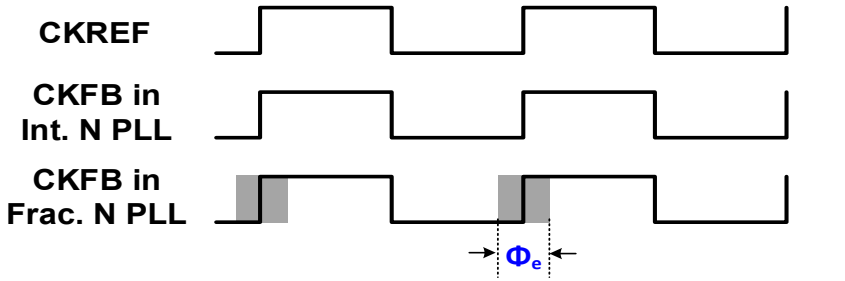


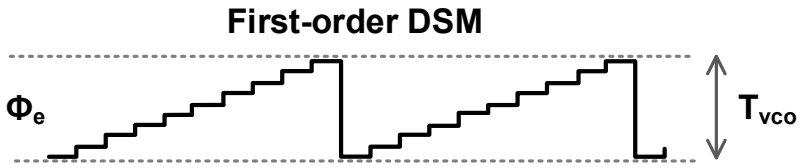
SSB PN contributors at a low jitter 6-GHz PLL output



Extra Challenges in Fractional-N PLLs

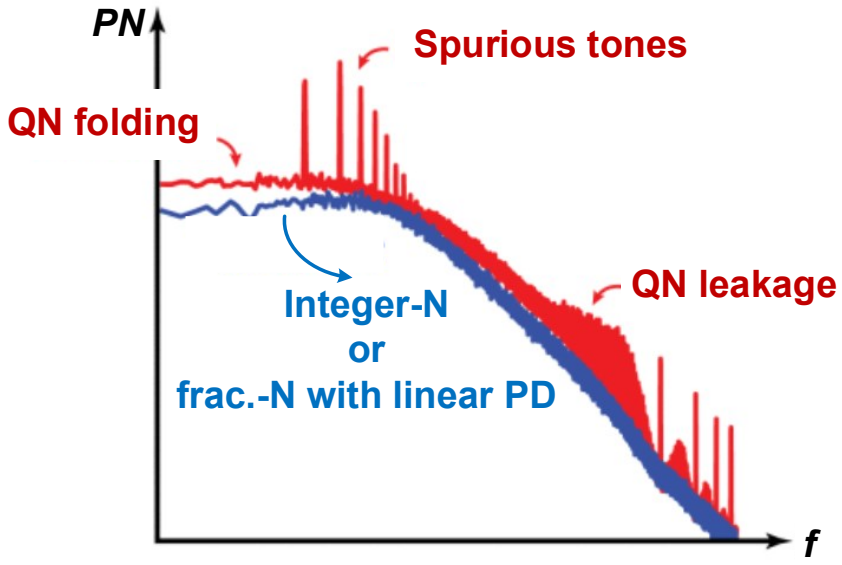






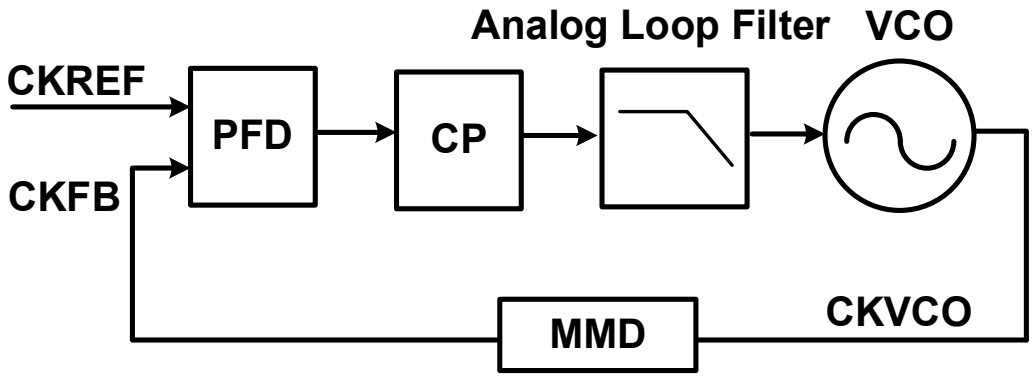
Mash1:	$-T_{VCO}/2 \leqslant \Phi_e \leqslant +T_{VCO}/2$
Mash1-1:	$-T_{VCO} \leqslant \Phi_e \leqslant +T_{VCO}$
Mash1-1-1:	$-2T_{VCO} \leqslant \Phi_e \leqslant +2T_{VCO}$

- **DSM QN**
- **Much wider dynamic range (DR) needed in PD**
- **Fractional spurs:**
  - **MMD, PD nonlinearity → result in noise folding, higher inband noise**
  - **Coupling between VCO/DCO and PD/CLKREF**

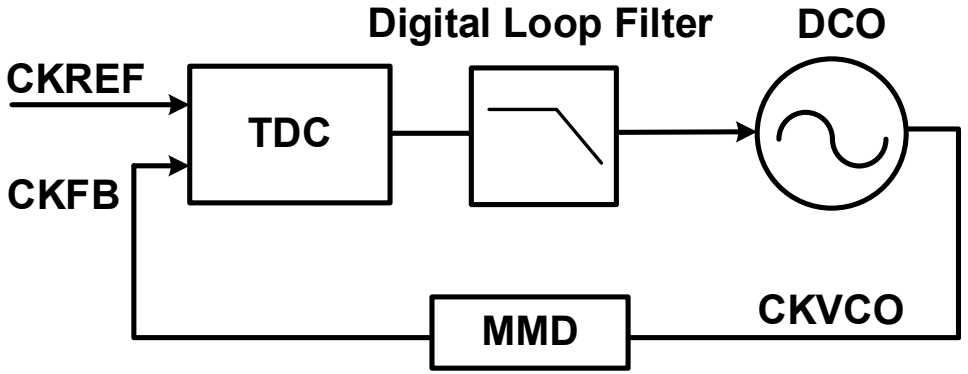


Major PLL Topologies – PD is Key Difference

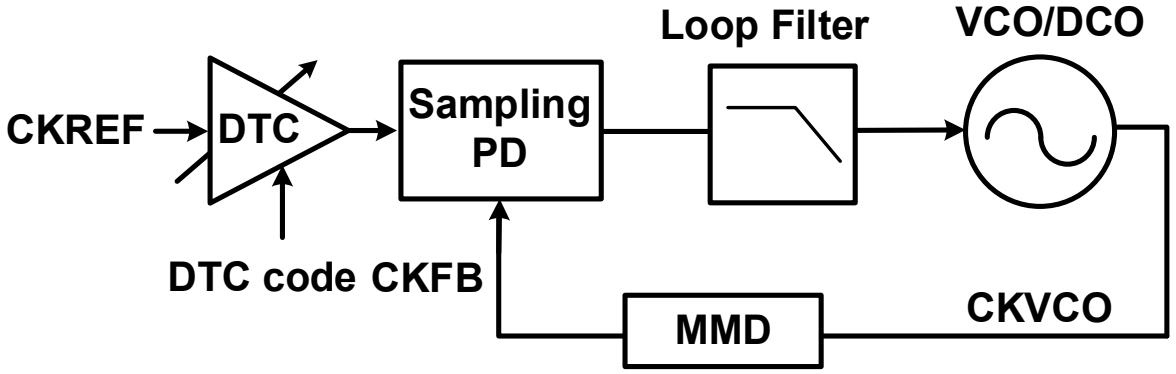
- Analog PLL using PFD-CP



- DPLL using TDC: small LF size, flexible calibration and configurability



- PLL using DTC-assisted PD



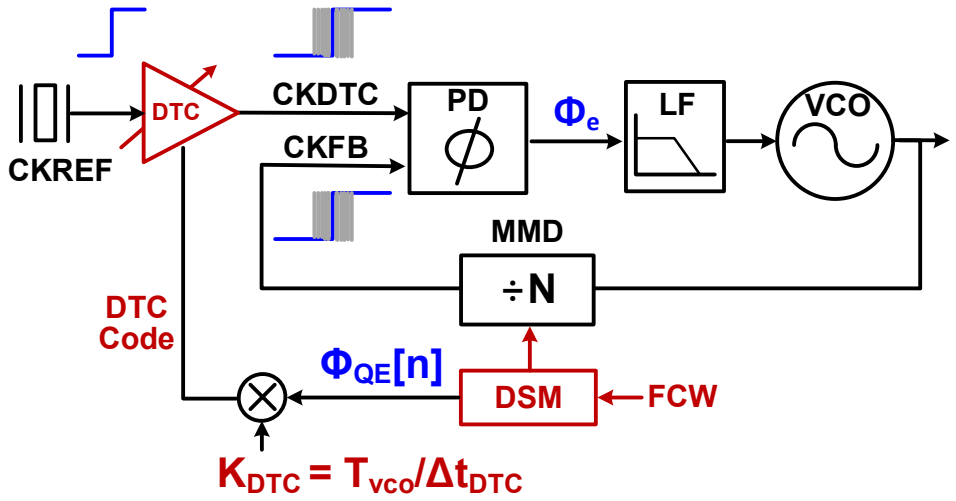
Show more advantages, gain popularity in both academia and industry

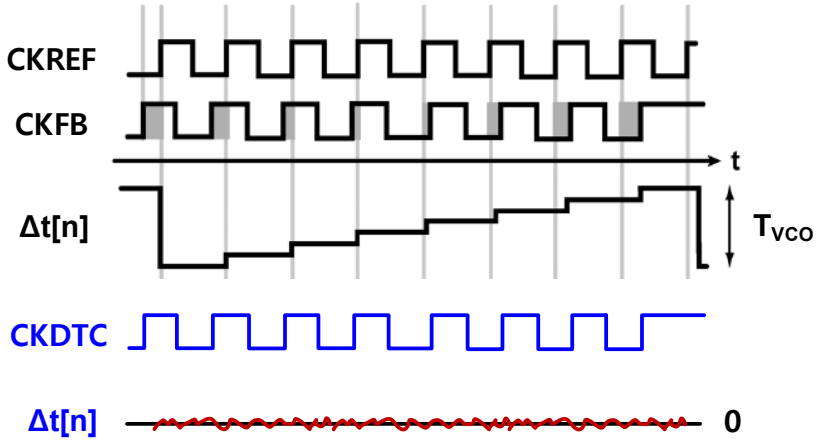
PD design metrics	▪ Thermal/flicker noise, maybe QN ▪ Linearity over required DR ▪ P_{dc} ▪ Complexity, area

Outline

- Fractional-N PLL Design Challenges
- **PLL Architecture Review**
- DTC-Assisted Phase Detector Design
- Digital Calibrations to Enhance PLL Performance
- LO Chain Design Example for 5G NR

Advantages of DTC-assisted PD





- DTC is a Digital-to-Time Converter
- DTC cancels accumulated QE on CKFB due to DSM

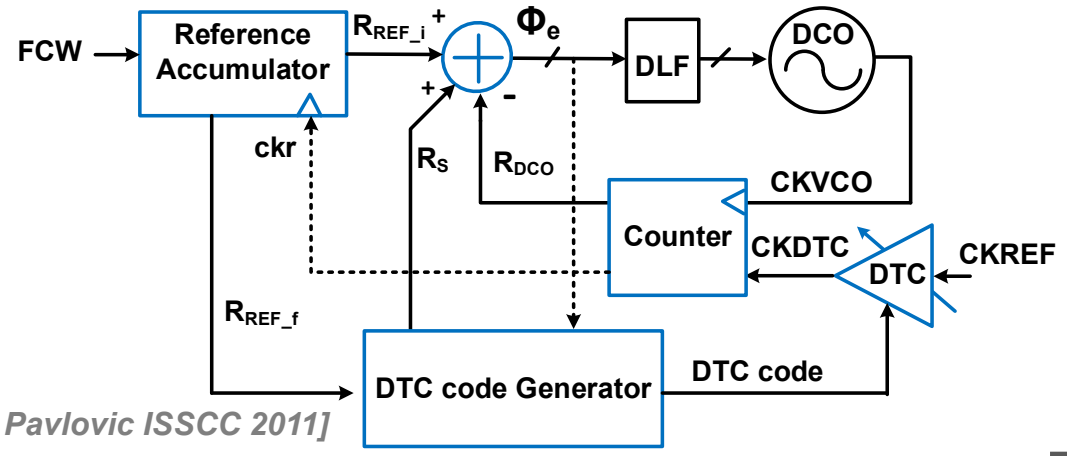
→ Near zero phase error at PD after locking

Just like integer-N case!

→ Can use high gain PD of small dynamic range for lower inband noise, high linearity, lower P_{dc} …

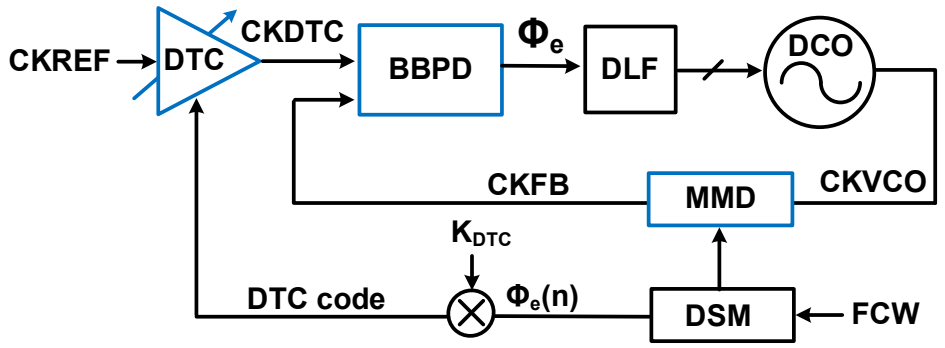
DTC-based PLL Variations – Digital PLLs

- **DTC-based ADPLL (1st order DSM)**



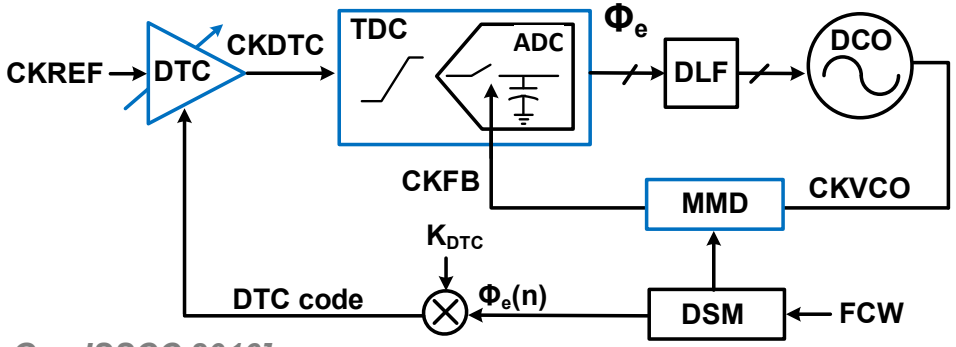
[N. Pavlovic ISSCC 2011]

- **DTC-based Bang-bang PLL**



[D. Tasca JSSC Dec. 2011]

- **Digital sampling PLL**



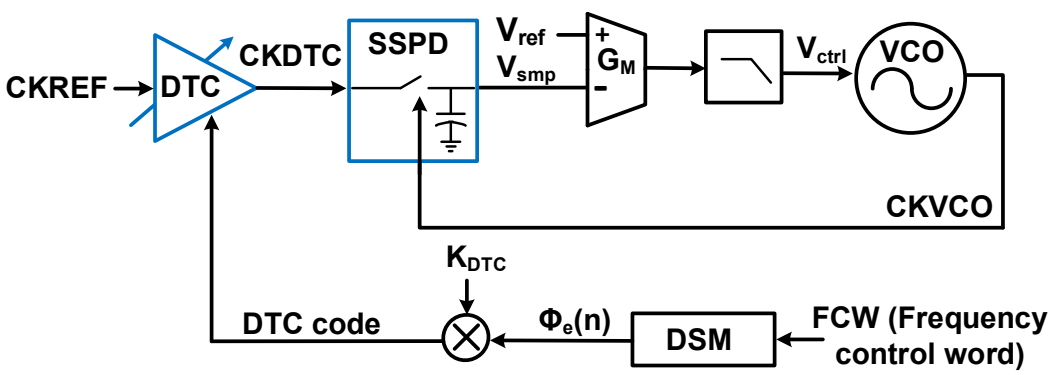
[X. Gao ISSCC 2016]

Pros:
- Φ_e is 1- or n-bit digital word
  → Used for LMS based K_{DTC} calibration
- DLF small chip area

Cons:
- BBPD simpler than TDC (sampler+ADC), but need aux circuits to linearize its gain, and achieve fast locking
- Need DCO

DTC-based PLL Variations – Analog PLLs

- **Analog PLL using sub-sampling PD**

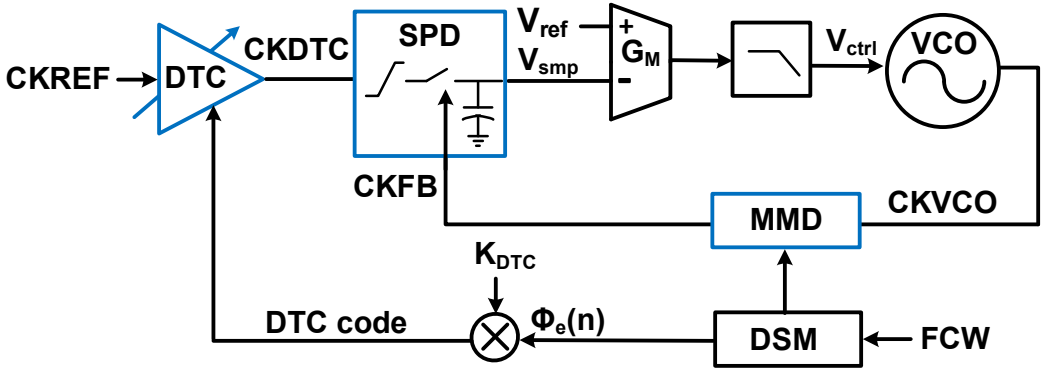


[K. Raczkowski JSSC May 2015]

Pros:
- PD is a simple sample-hold circuit
- K_{PD} is linear and well-defined vs. BBPD
- No high-resolution TDC, no DCO

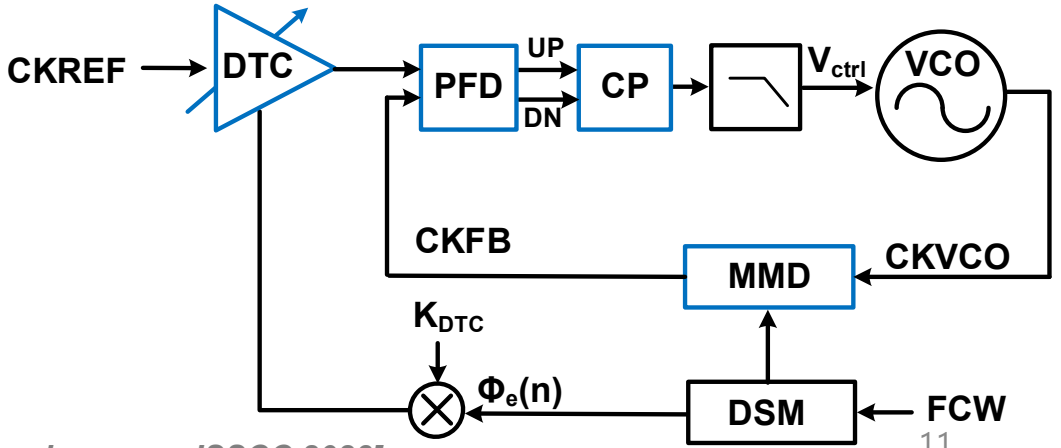
Cons:
- LF C_I for optimal IPN ≤ 50pF typically (small overhead); type-I removes C_I
- Need to digitize Φ_e for calibrations

- **Analog PLL using sampling PD (SPD)**



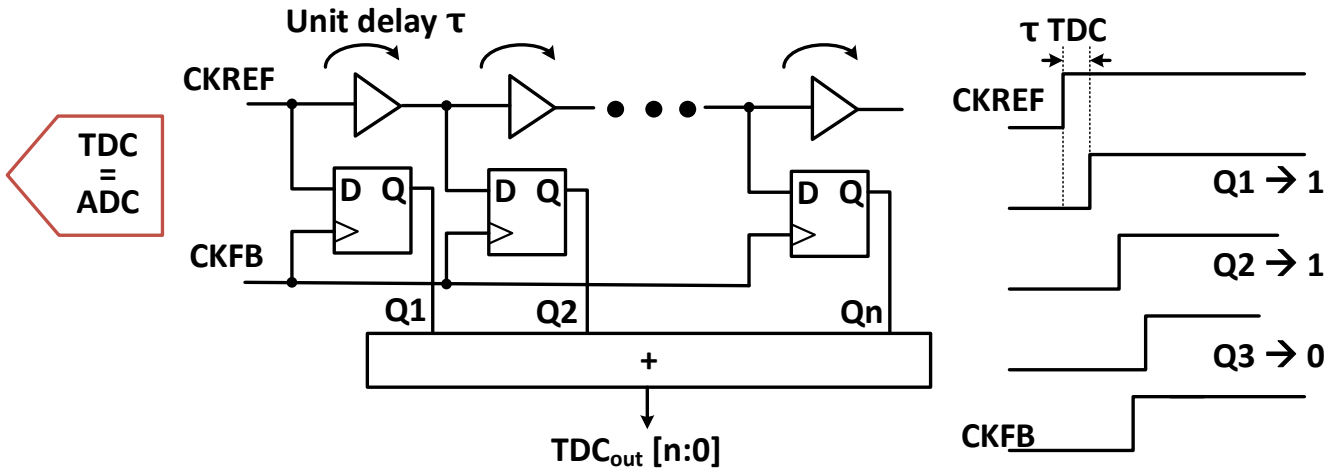
[W. Wu JSSC May 2019]

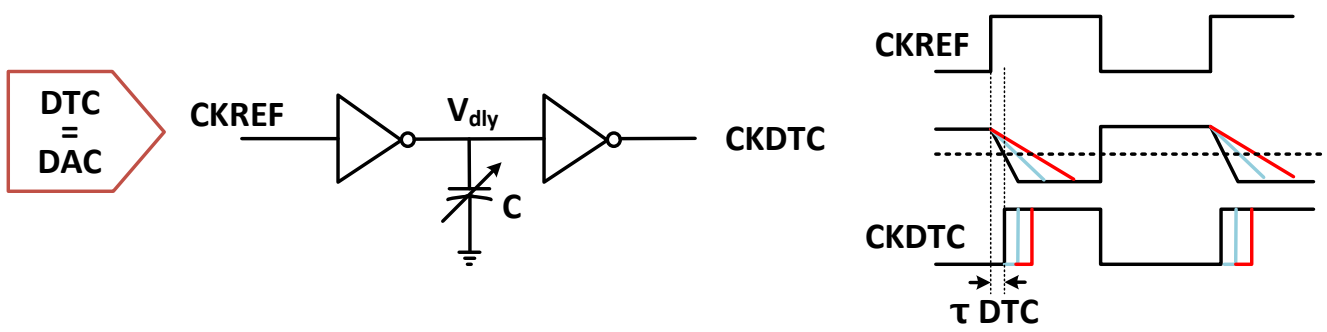
- **DTC-assisted CP PLL**



[P. Renukaswamy ISSCC 2023]

DTC vs. TDC as Phase Detector





- **TDC-based digital PLL**
  - **In-band noise limited by TDC QN**

    Δt ~ 8ps in 14nm CMOS
  - **Finer τ → Complexity ↑**

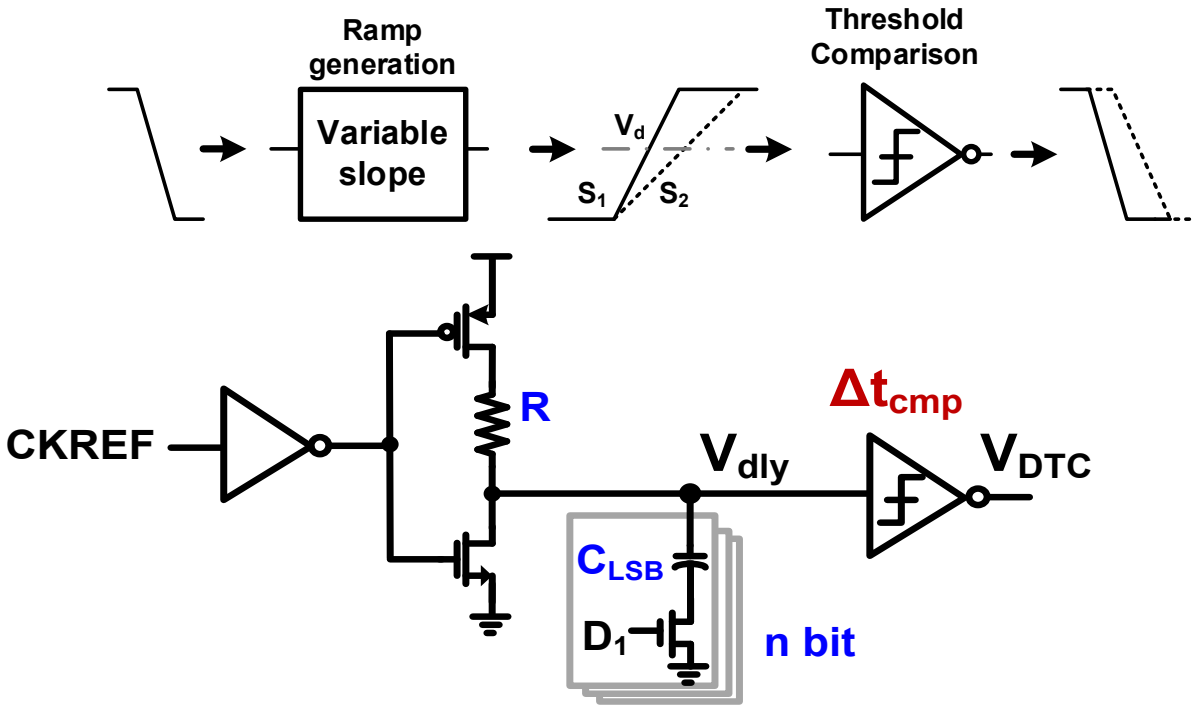
    coarse-fine, Vernier delay line, timing amplifier, noise shaping, stochastic flash TDC, …
- **DTC-based analog/digital PLL**
  - **QN < other noise**

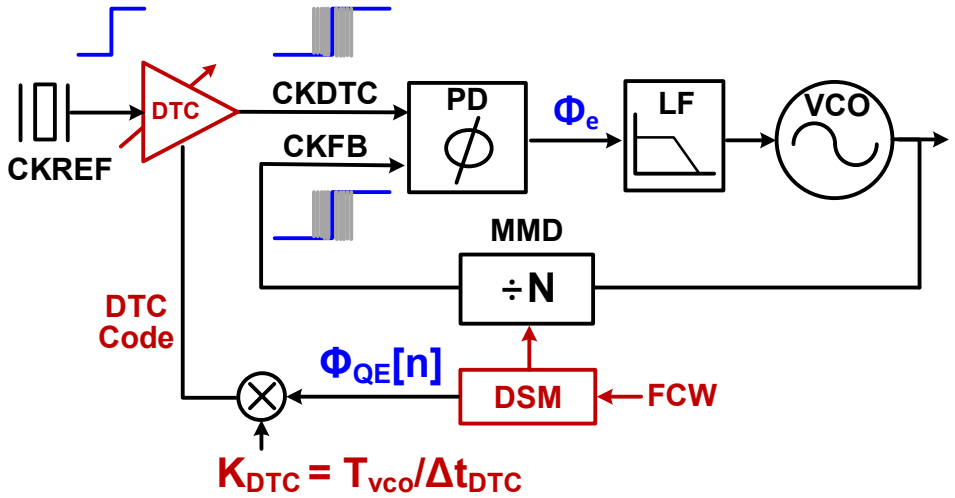
    Δt ~ 100fs in 14nm CMOS
  - **Broadly applicable**
    - **Bang-bang**
    - **Type-I/II (sub)sampling**
    - **Digital (sub)sampling**

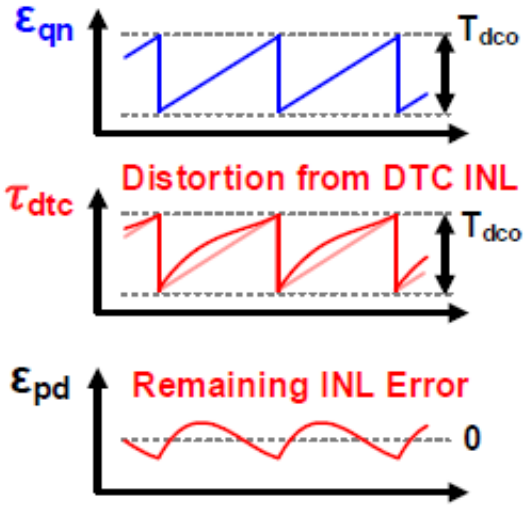
Outline

- Fractional-N PLL Design Challenges
- PLL Architecture Review
- **DTC-Assisted Phase Detector Design**
  - **RC Delay Based DTC**
  - **Other DTC Topologies for high linearity**
- Digital Calibrations to Enhance PLL Performance
- LO Chain Design Example for 5G NR

RC Delay Based DTC- Variable Slope DTC







DTC contributes to PLL integrated PN (IPN)

- DTC RMS jitter → inband PN
- DTC quantization noise → inband PN
- DTC nonlinearity → frac. N spurs and noise folding

DTC Noise: Quantization Noise

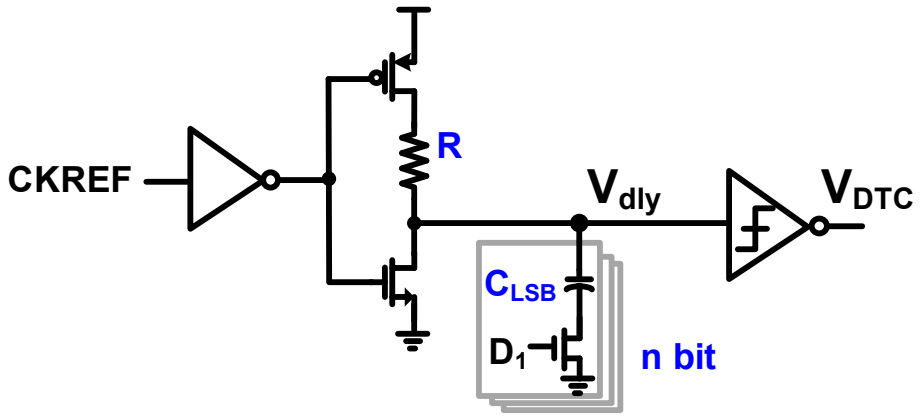
■ DTC QN

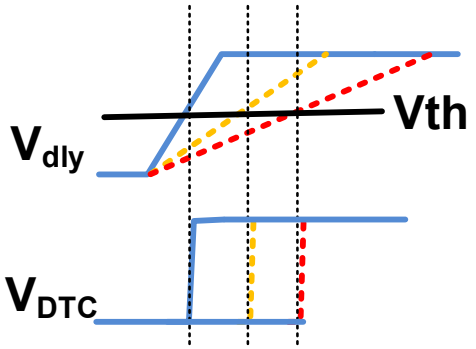
Unit delay $T_{res} = \ln 2 \cdot R \cdot C_{LSB}$

Input referred (at CKREF) $\Phi_{DTC,\ QN} = \frac{(2\pi \cdot T_{res})^2}{12} \cdot f_{ref}$

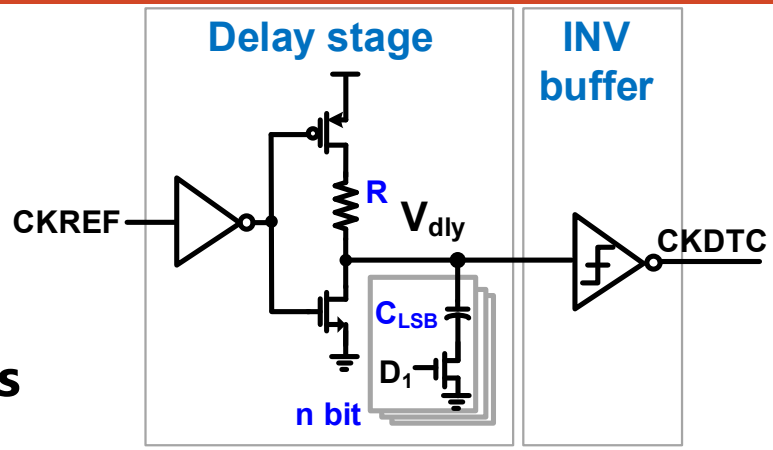
e.g., T_{res} **= 400fs,** f_{ref} **= 104MHz, → $\Phi_{DTC,\ QN,\ in\ dBc/Hz}$ = -163dBc/Hz**

10bit → total delay range, DR = 400ps, can support 2nd-order DSM with f_{VCO}> 5GHz





DTC Noise: Thermal Noise



■ DTC thermal noise: delay stage and INV buffer

1) PN from delay stage:

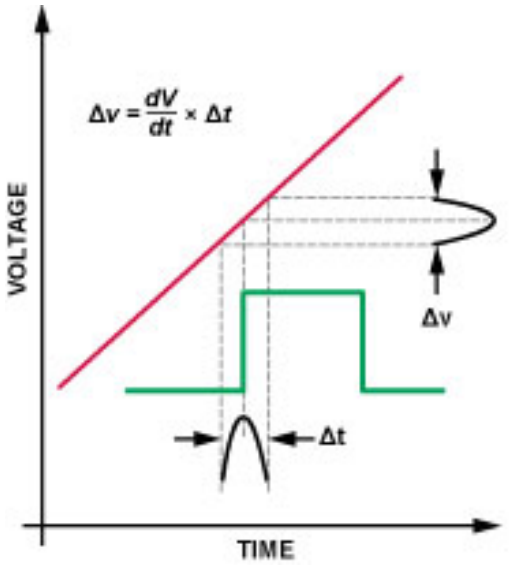
Depends on slew of V_{dly}, thus, DTC code

SSB PN sampled at half VDD transition considering noise folding is

$$\mathcal{L} \cong 10 \cdot log_{10}\left[\frac{1}{2}\left(\frac{2\pi \cdot f_{ref}}{k_{slew}}\right)^2 \cdot S_v^{folded}(f_m)\right], k_{slew} = \frac{1}{2RC} \text{ at } \frac{VDD}{2}, S_v^{folded}(f_m) \cong \frac{KT/C}{f_{out}/2}$$

$$\rightarrow \mathcal{L} \cong 10 \cdot log_{10}\left[2kT \cdot f_{ref}\left(\frac{2\pi}{\ln 2}\right)^2 \cdot \frac{2^n \cdot {T_{res}}^2}{C_{LSB}}\right] \text{ at mid code,}$$

e.g., C_{LSB} needs ≥ 2fF for PN floor < - 171dBc/Hz



2) PN from INV buffer dominates:

INV BUF size up to hundreds of μm Width

[W. Wu JSSC 2019]

DTC Nonlinearity – Static Distortion

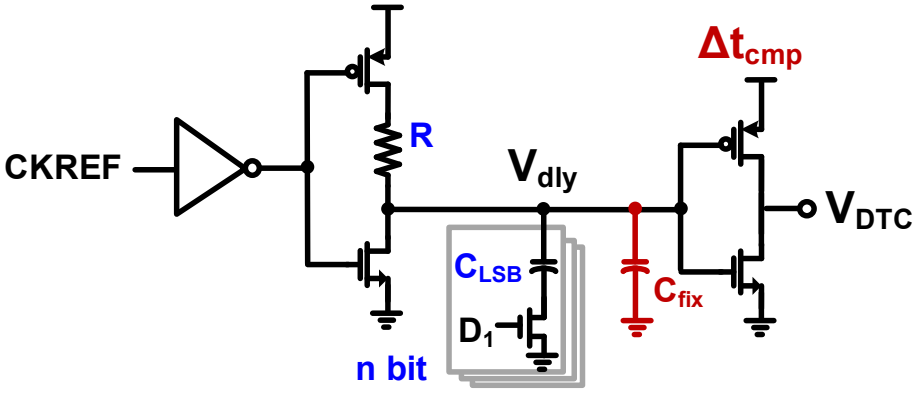
- **Matching of capacitor array → not dominate as $C_{LSB} \geq 2fF$**

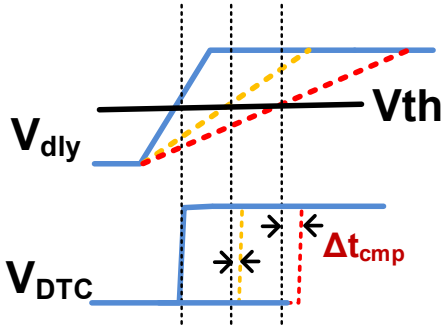
- Common centroid layout, DEM to achieve DNL= ±0.2 LSB for 10bit DTC

- **Code/slope dependent Δt_{cmp} → INL, dominate!**

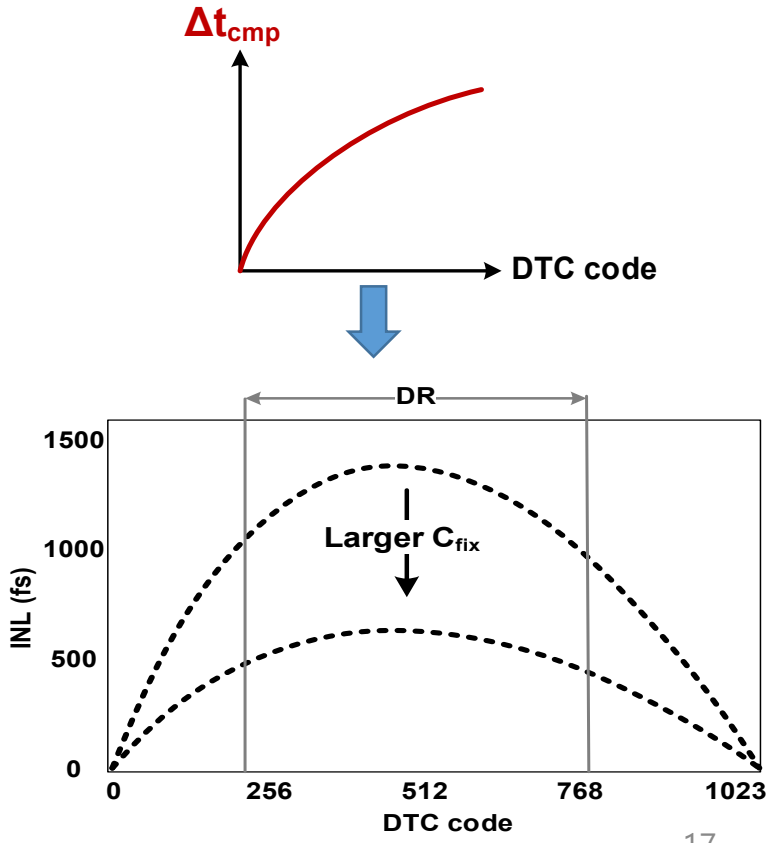
- Fixed cap. (e.g., 1~2 pF) reduces INL < ~2 LSB

- Parasitic cap of INV BUF serves as fixed cap





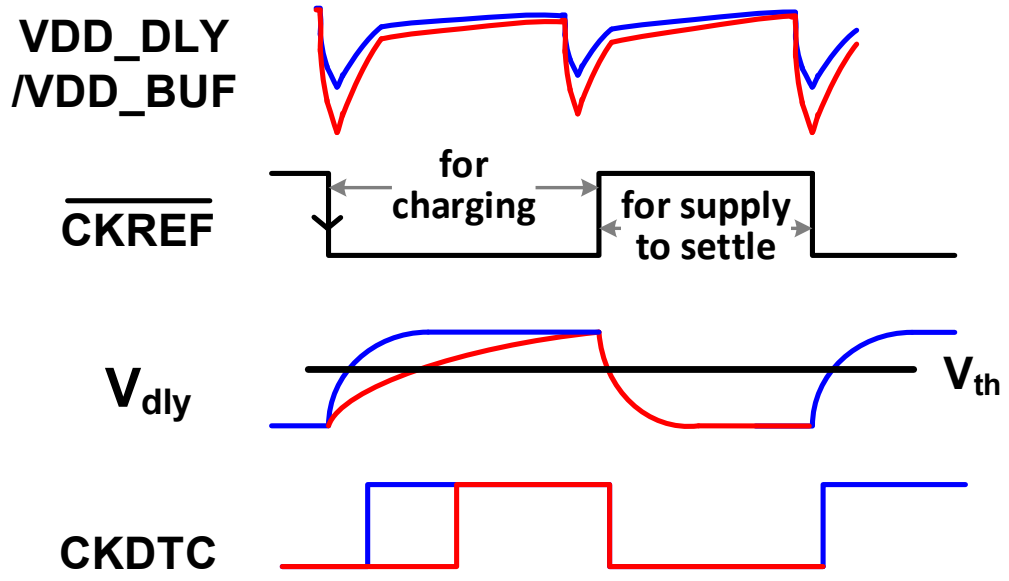
Δt_{cmp} varies with V_{dly} slope → INL

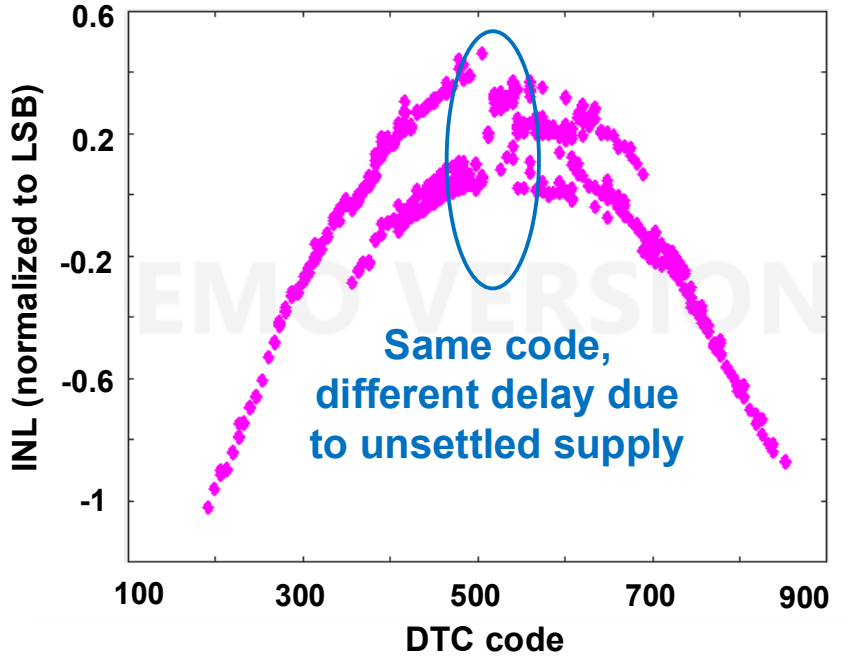


DTC Nonlinearity – Dynamic Distortion

- **Code-dependent supply settling error → INL, memory effect, dominate!**

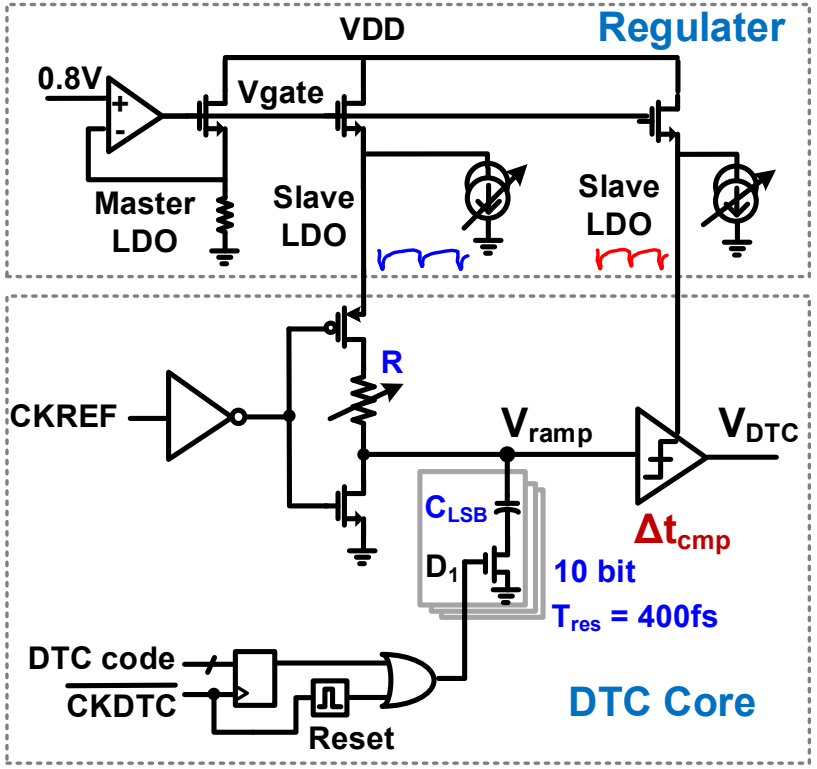
  Large transient current at CKREF edges, supply dips and resettle each cycle



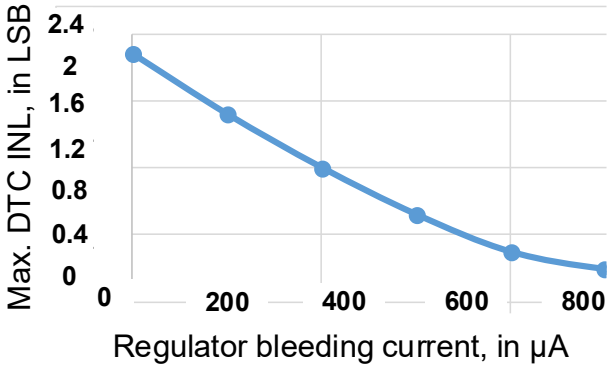


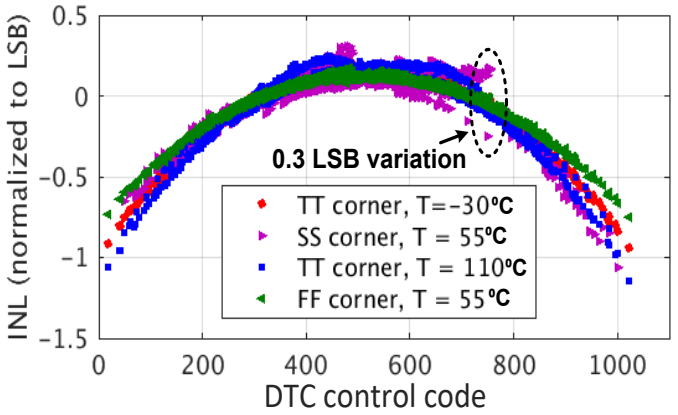
- **Code-dependent charge on bottom plate of unit cap. array**
  → INL, memory effect

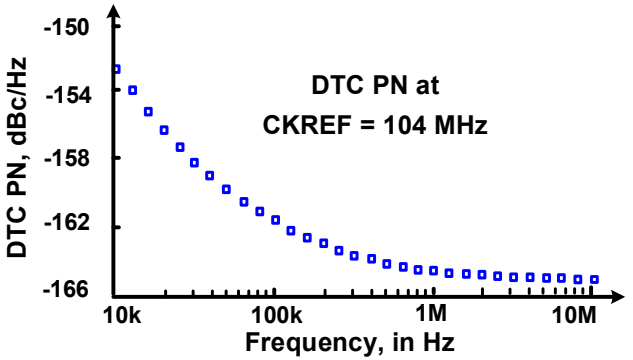
High Performance DTC Design Example



- Master-slave regulator for fast settling
- Bleeding current
  ↑ gm/C to speed up settling
  at cost of higher I_{dc}
- Programmable R cover process variation



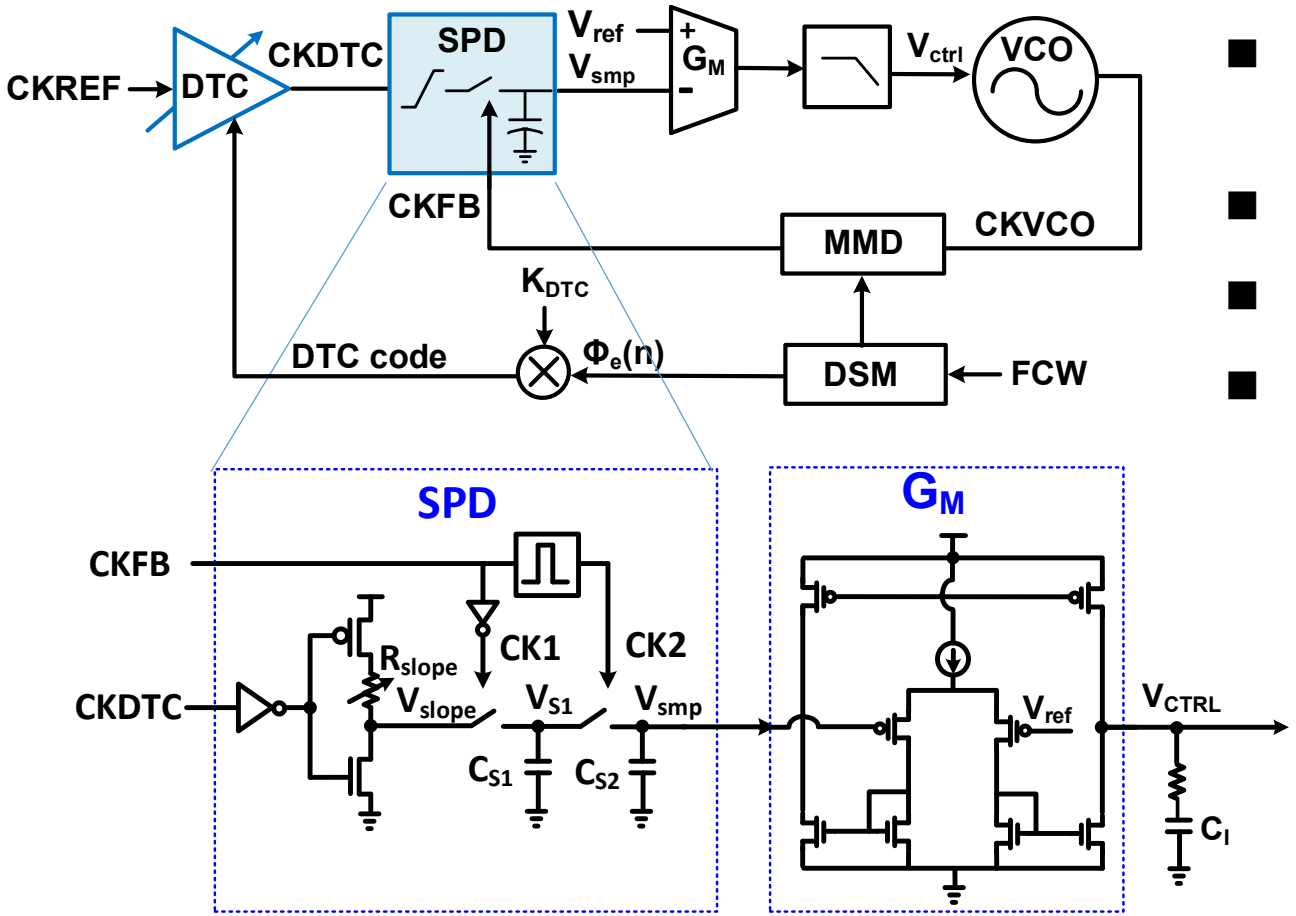




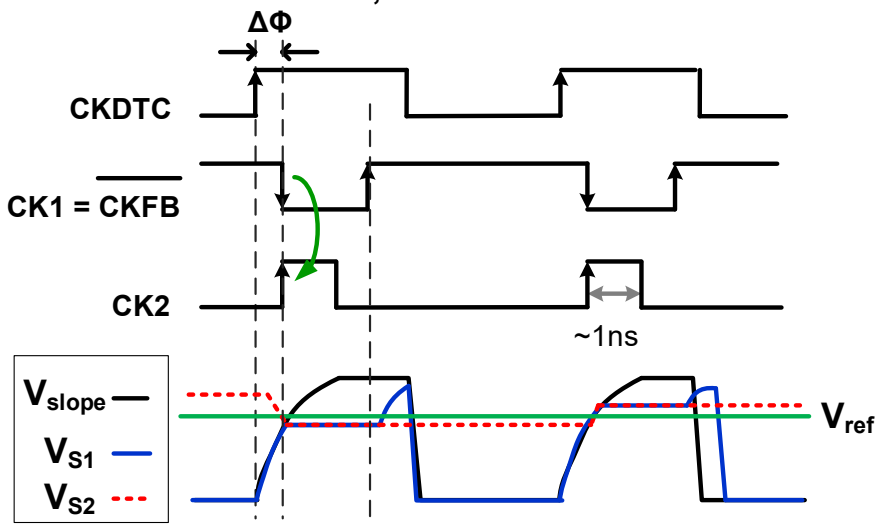
[W. Wu JSSC Dec 2021]

- DTC code reset to "1" each cycle to fully discharge tuning cap.

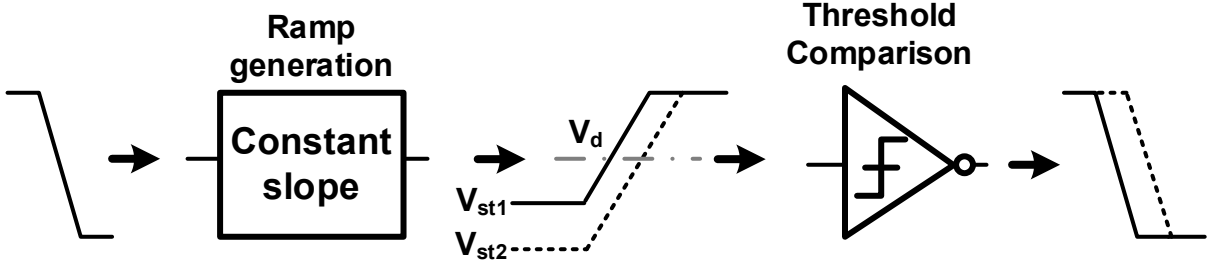
Continue with DTC-Assisted PD in Analog PLL



- Vsmp is ZOH: 1st-order IIR filtering
- $K_{SPD}=K_{slope}/(2\pi f_{ref})$, for K_{slope}= 6GV/s, f_{ref}= 104 MHz, → K_{SPD} =57/2π >> K_{PD} in PFD-CP PLL
- G_M can be μA, its noise suppressed by high K_{SPD}
- Linearity of SPD not critical as DTC cancels QE
- Noise: ~200fF $C_{s1,2}$ results in <-170dBc/Hz

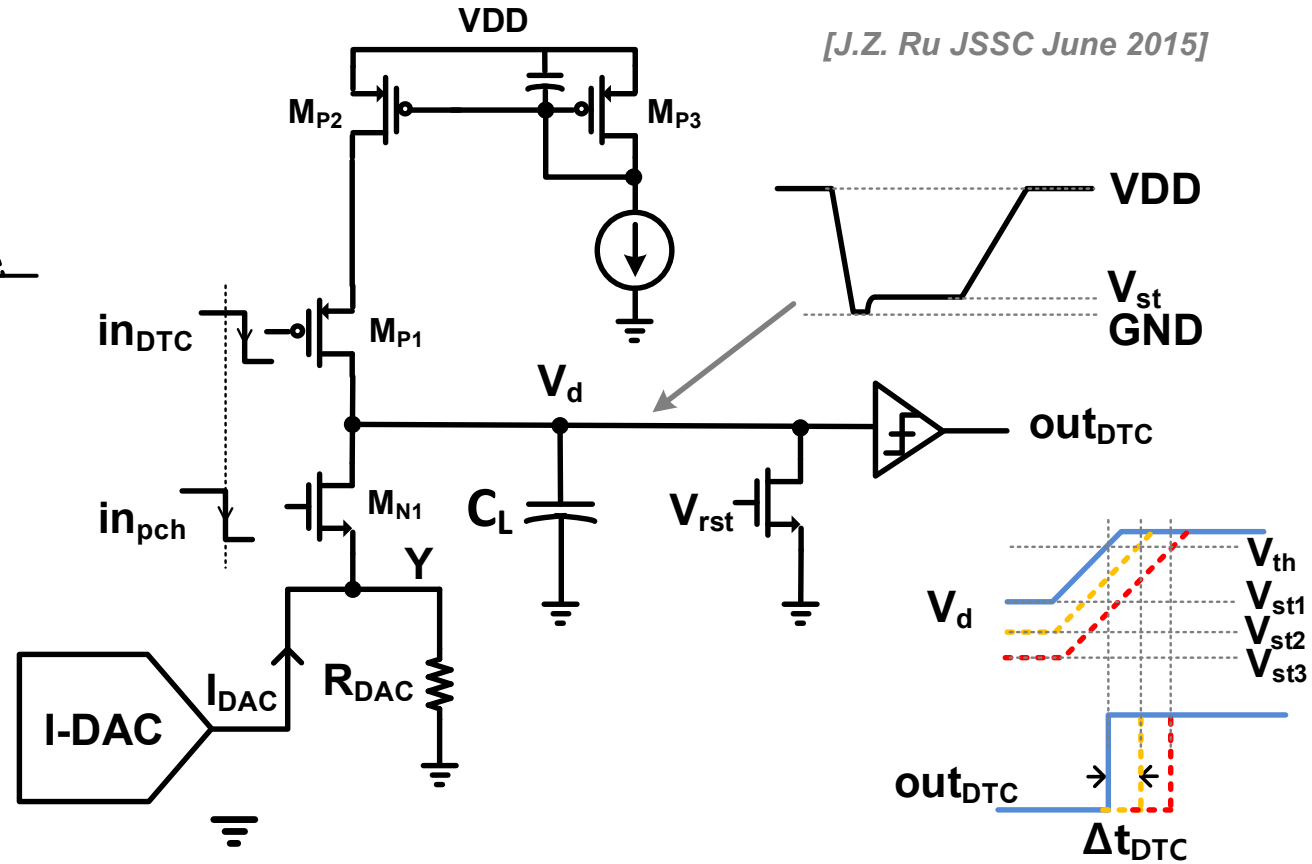


Constant Slope DTC (I/C)

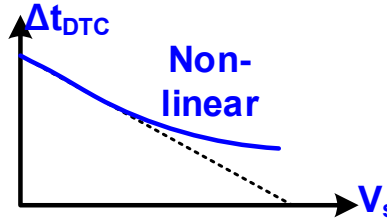


- **Pros:** no slope dependent delay
- **Cons:**
  - **Nonlinearity sources**: I varies with code due to channel length mod., V_{st} settling error, etc.
  - **Flicker noise** from I
  - **Need high VDD** for high performance (e.g., 1.5V)

[J.Z. Ru JSSC June 2015]

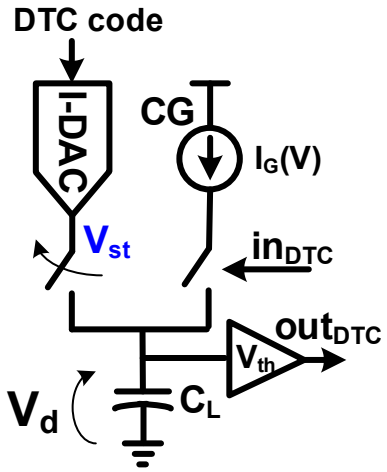


$$\Delta t_{DTC} = \int_{V_{st}}^{V_{th}} \frac{C_L(V)}{I_G(V)} dV$$



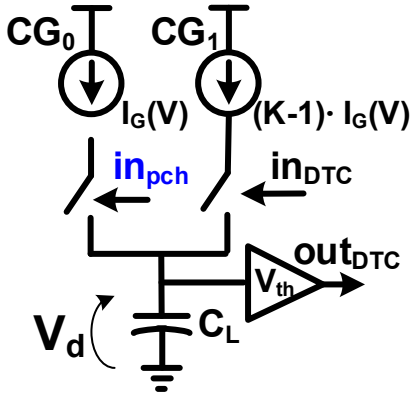
Inverse-Constant-Slope DTC for Coarse-Fine DTC

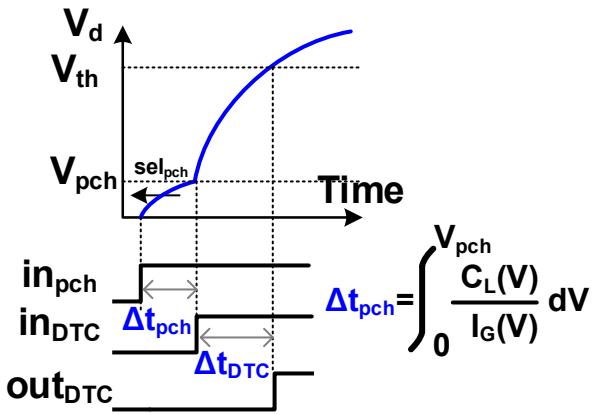
Constant slope DTC



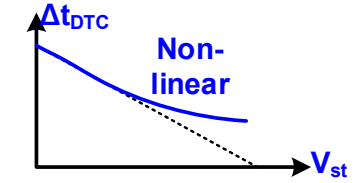
ICS-DTC

[S. M. Dartizio ISSCC 2023]

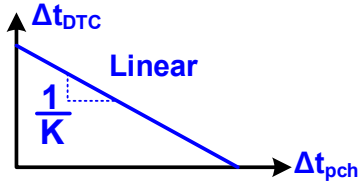




$$\Delta t_{DTC} = \int_{V_{st}}^{V_{th}} \frac{C_L(V)}{I_G(V)} dV$$



$$\Delta t_{DTC} = \int_{0}^{V_{th}} \frac{C_L(V)}{K\cdot I_G(V)} dV - \frac{\Delta t_{pch}}{K}$$

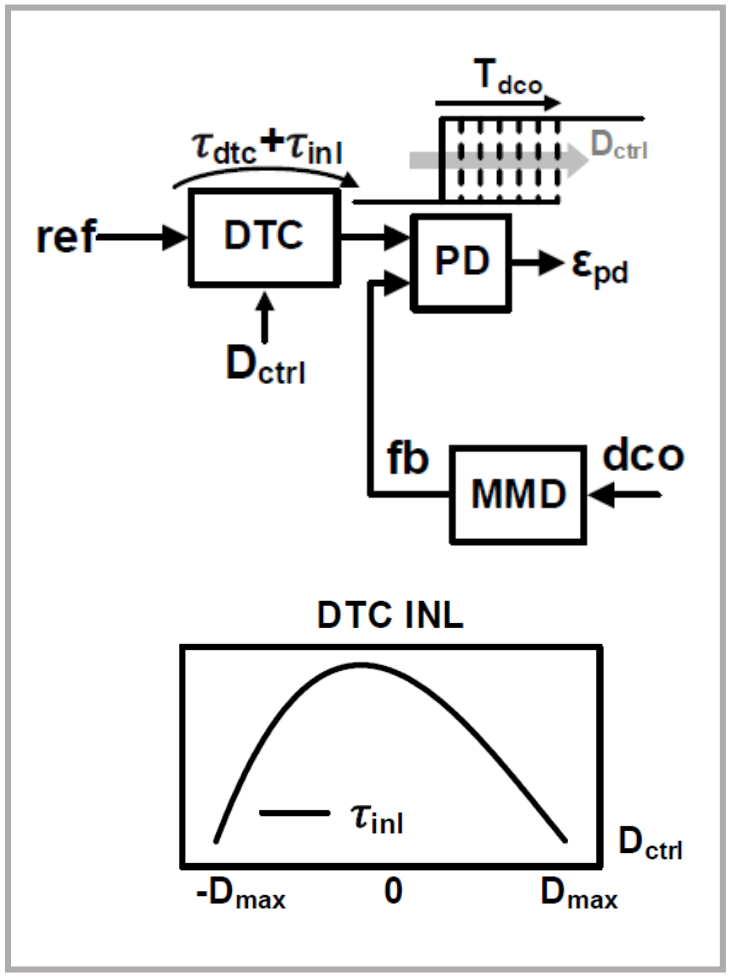


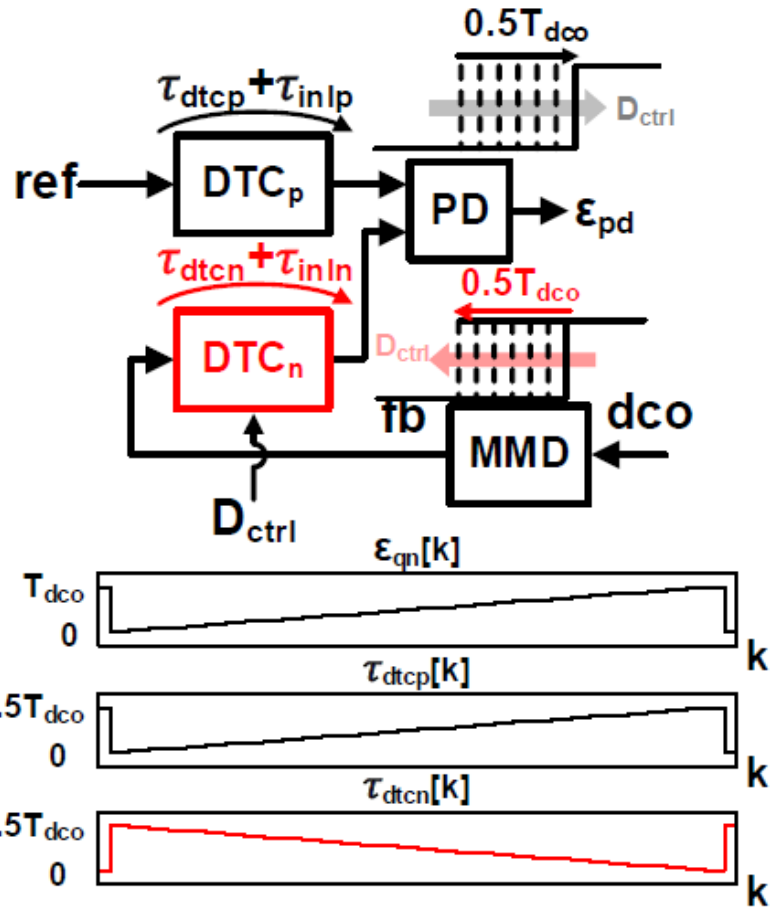
- DTC delay controlled by voltage Vpch → controlled by time Tpch
- Linearity affected to $I_G(V)$ and C(V) → immunity to $I_G(V)$ and C(V)
- Linearity affected by DAC → no need DAC

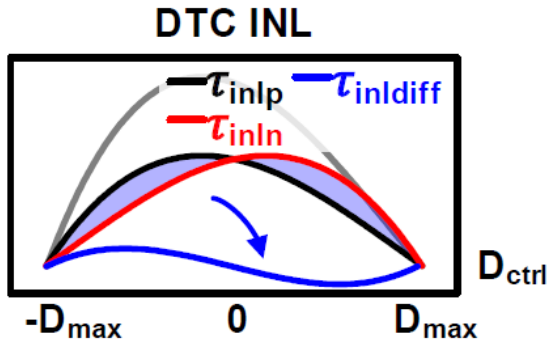
Too coarse, need another fine DTC

T_{pch}, T_{dtc} gen. uses DFFs and mux at fvco

Pseudo-Differential DTC for Better Linearity







$$\tau_{inldiff}(D_{ctrl}) = \tau_{inlp}(D_{ctrl})-\tau_{inln}(D_{ctrl})$$

$$= 2b_1 \frac{D_{ctrl}}{2D_{max}} \left(1-4\left(\frac{D_{ctrl}}{2D_{max}}\right)^2\right)$$

only odd-symmetric components

[D. Xu ISSCC 2024]

- Two half-range DTCs → each DTC has better linearity
- Even-symmetric INL cancels

Digital Assisted Techniques for Linear DTC

- DTC nonlinearity calibration (NLC)
- Reverse-Concavity Variable-Slope DTC
- DTC range reduction with multiple VCO/DCO phases

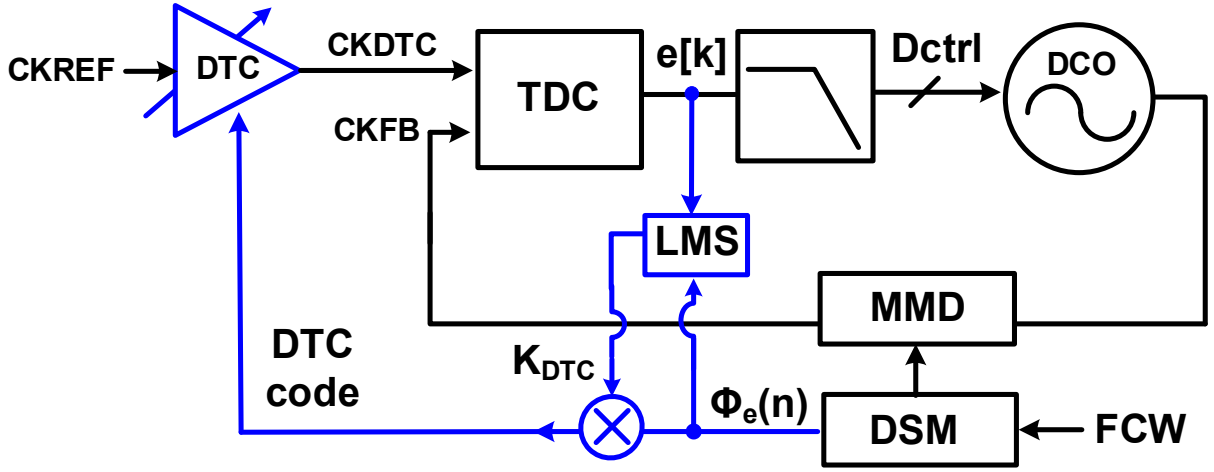
Will be discussed next in digital calibration section

Outline

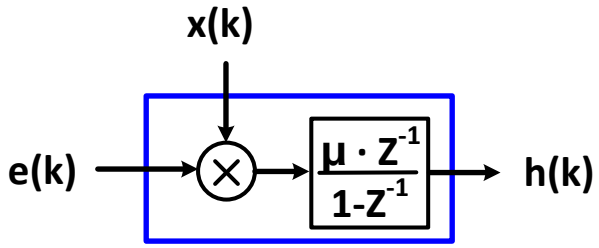
- Fractional-N PLL Design Challenges
- PLL Architecture Review
- DTC-Assisted Phase Detector Design
- **Digital Calibrations to Enhance PLL Performance**
  - **DTC Gain CAL, NLC, Range Reduction**
- LO Chain Design Example for 5G NR

Adaptive Filter Used in DPLL for Calibration

DTC gain need to be accurate to ensure QN cancellation

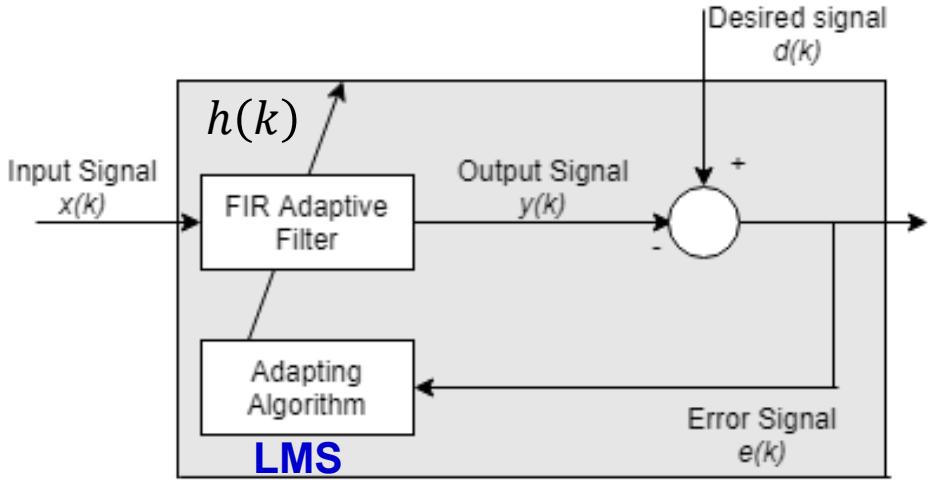


LMS adaptation

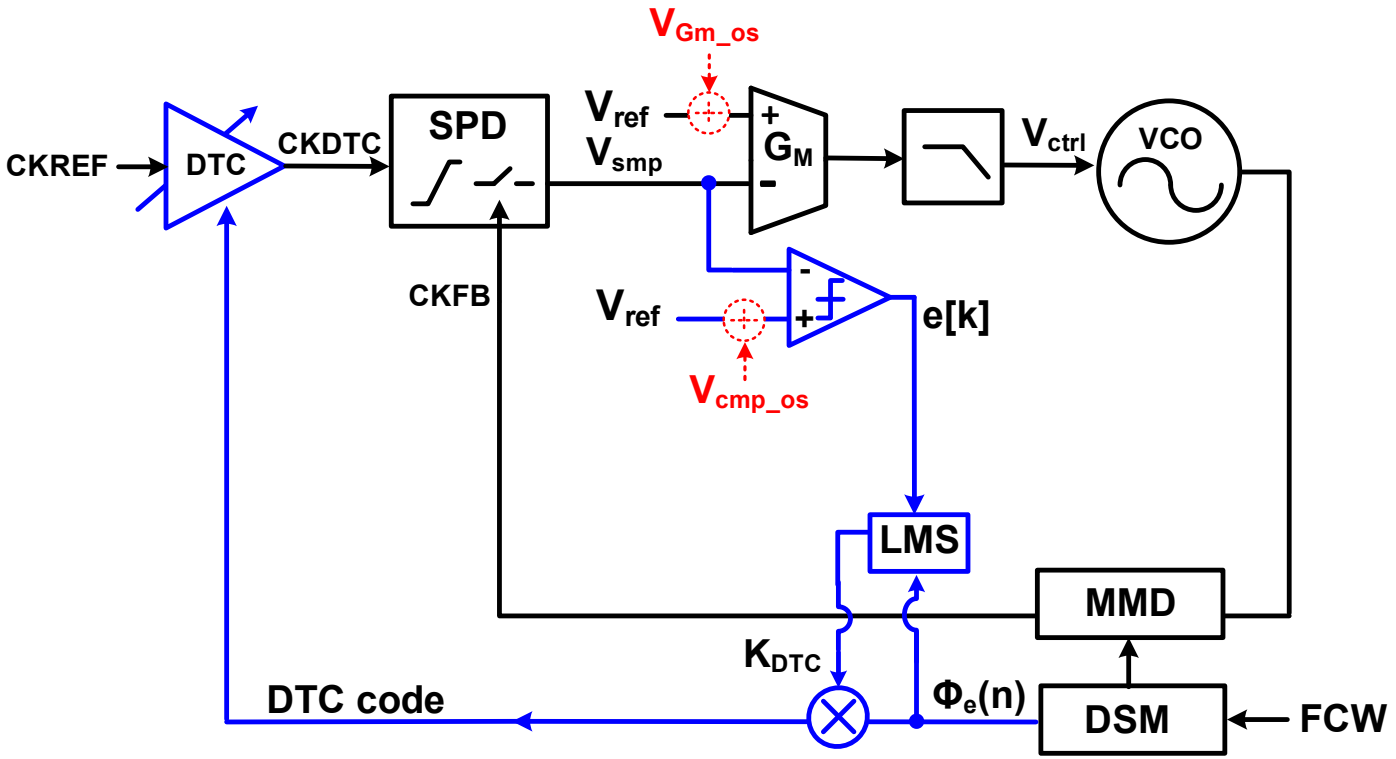


For DTC gain calibration:

- h(k) is K_{DTC}
- Input signal x(k): accumulated QE due to DSM, i.e., Φe.
- Error signal e(k): phase error between CKREF and CKFB
- CKDTC phase is the output signal y(k)
- CKFB phase is the desired output signal d(k)

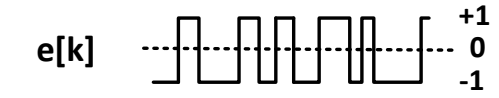


DTC Gain CAL in Analog Sampling PLL [1]



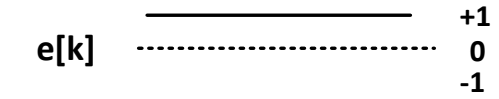
- **Issues of comparator, G_M offset**

$V_{cmp\_os} = V_{Gm\_os}$

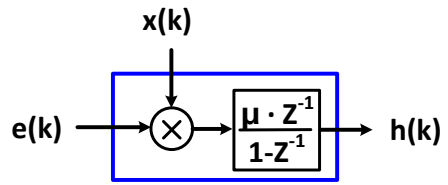


$V_{cmp\_os} < V_{Gm\_os}$

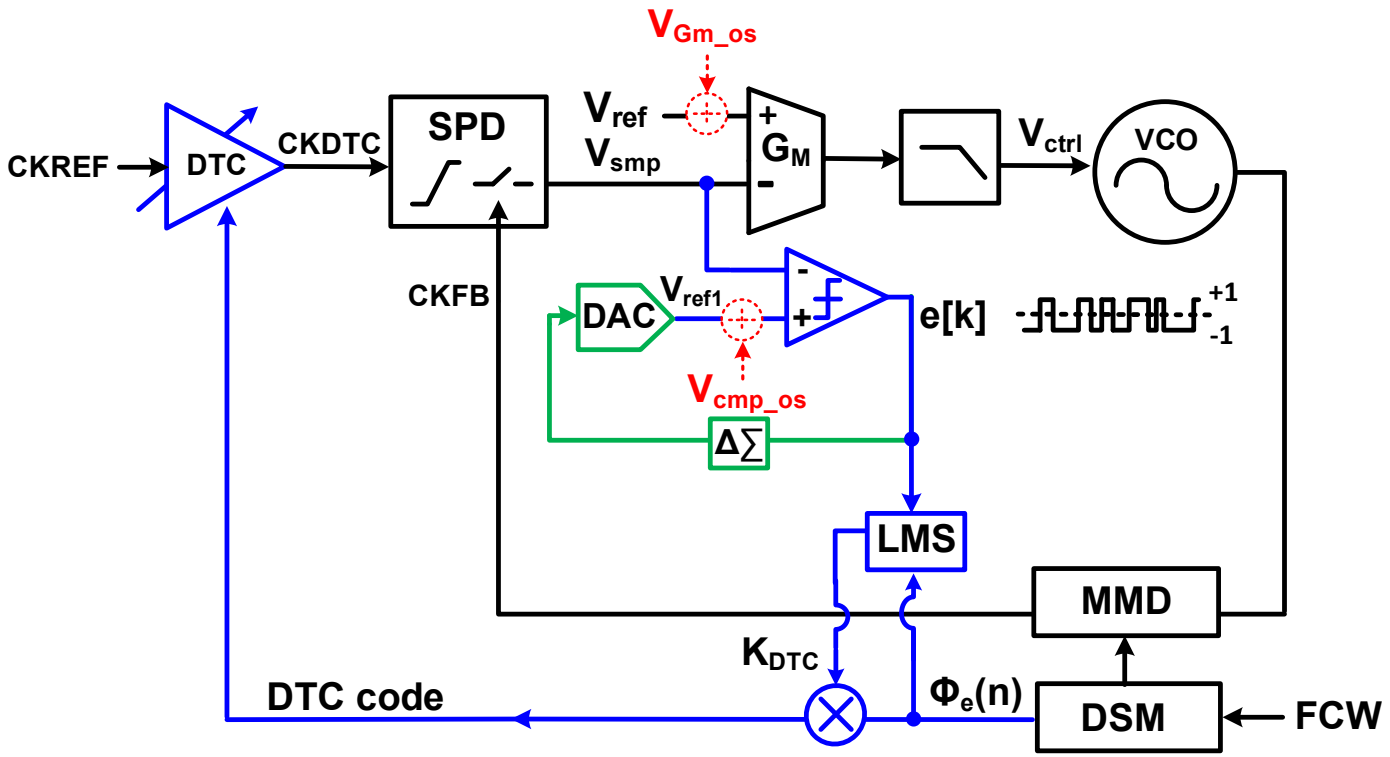
$V_{cmp\_os} > V_{Gm\_os}$



LMS adaptation



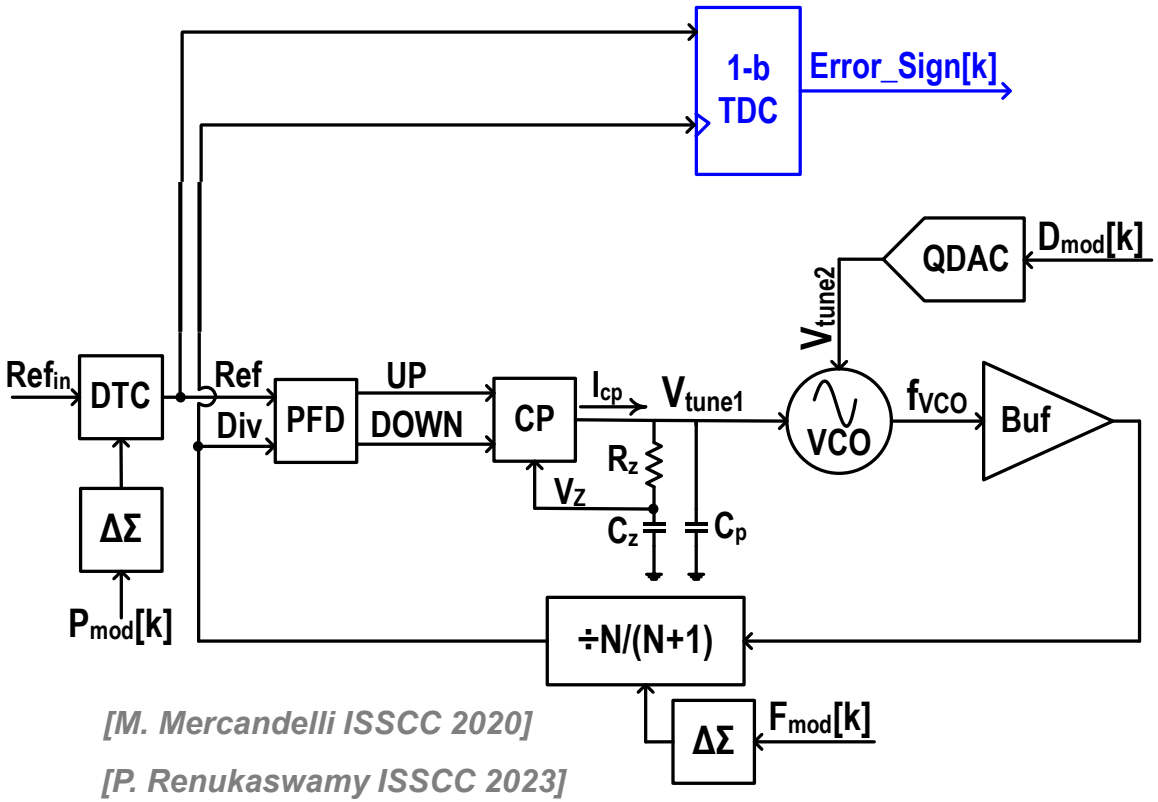
DTC Gain CAL in Analog Sampling PLL [2]



[W. Wu JSSC 2019]

- Single comparator gets sign of PHE, e[k] → LMS
- Remove DC offset in e[k] by adjusting V_{ref1}
- Simple 1-bit ΔV-DAC is sufficient

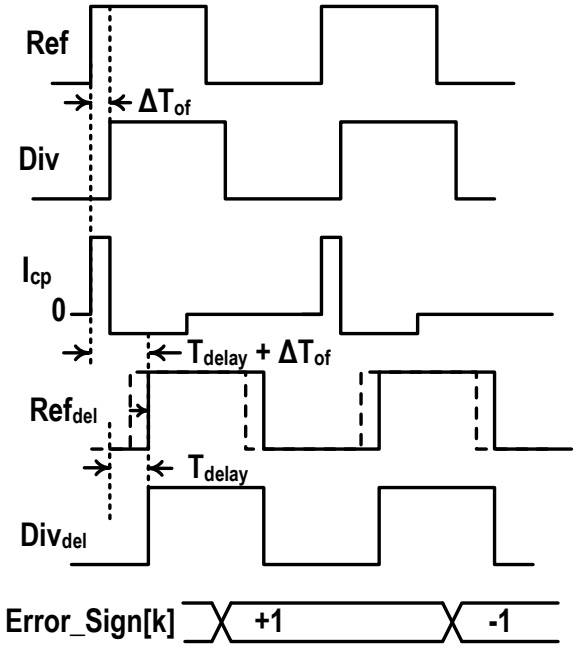
Alternative Way to Get Zero-Mean PHE Sign [1]



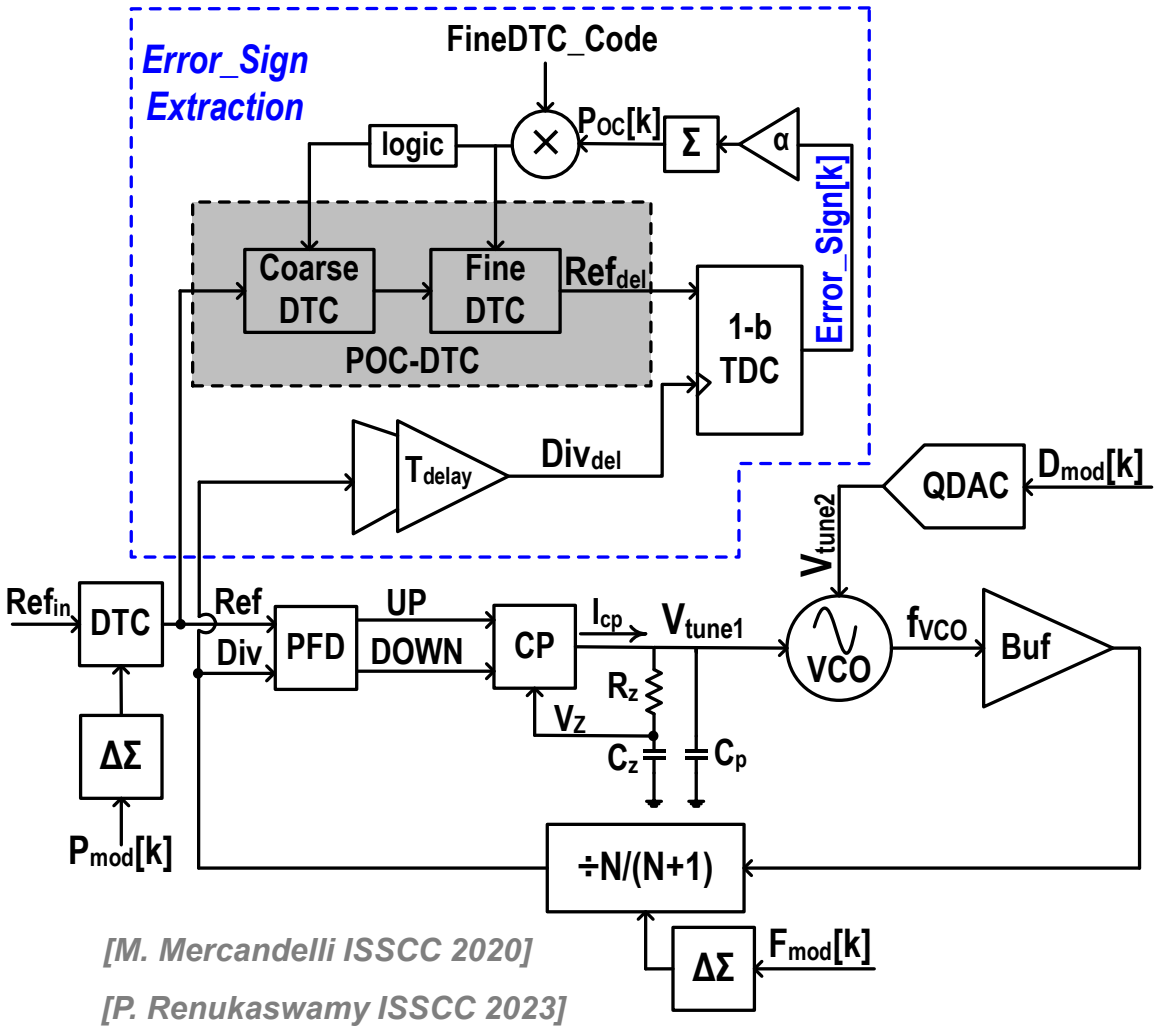
[M. Mercandelli ISSCC 2020]

[P. Renukaswamy ISSCC 2023]

- Phase offset (ΔT_{of}) varies over PVT
- Use coarse-fine DTC to compensate ΔT_{of} → POC-DTC tracks ΔToff over PVT
- Error_Sign[k] is zero-mean after convergence



Alternative Way to Get Zero-Mean PHE Sign [2]



[M. Mercandelli ISSCC 2020]

[P. Renukaswamy ISSCC 2023]

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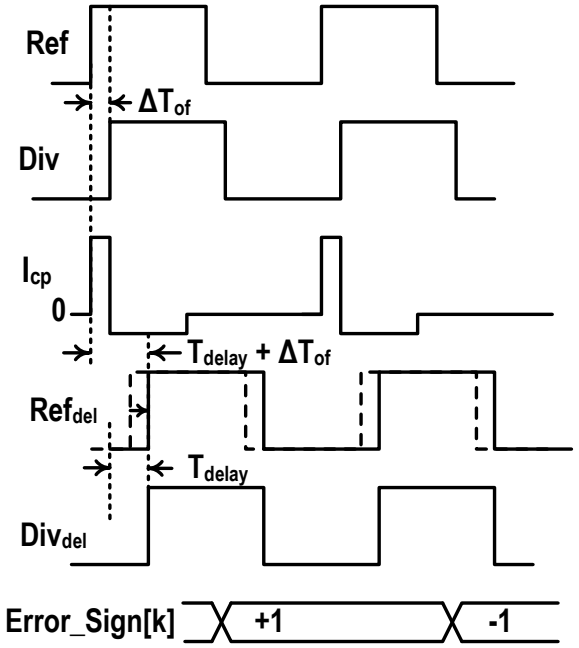
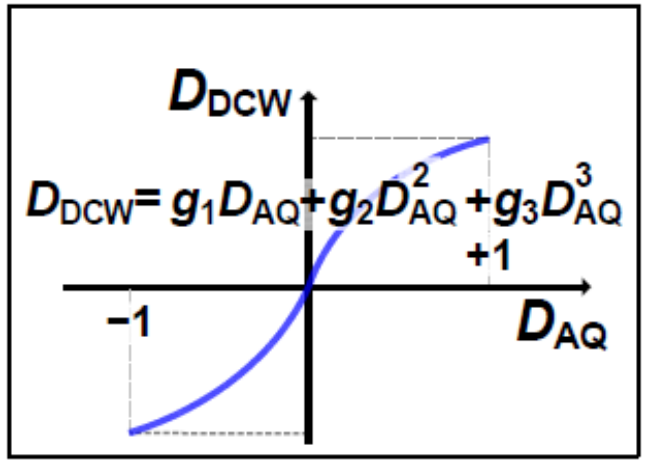
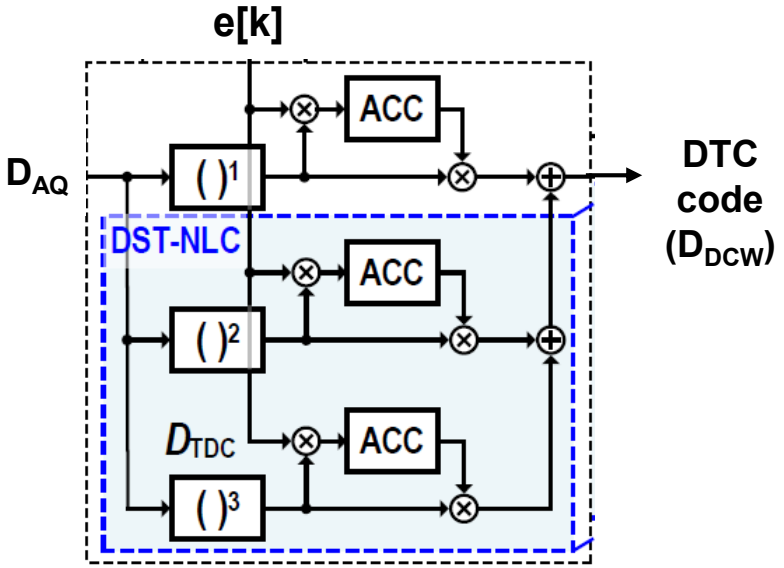


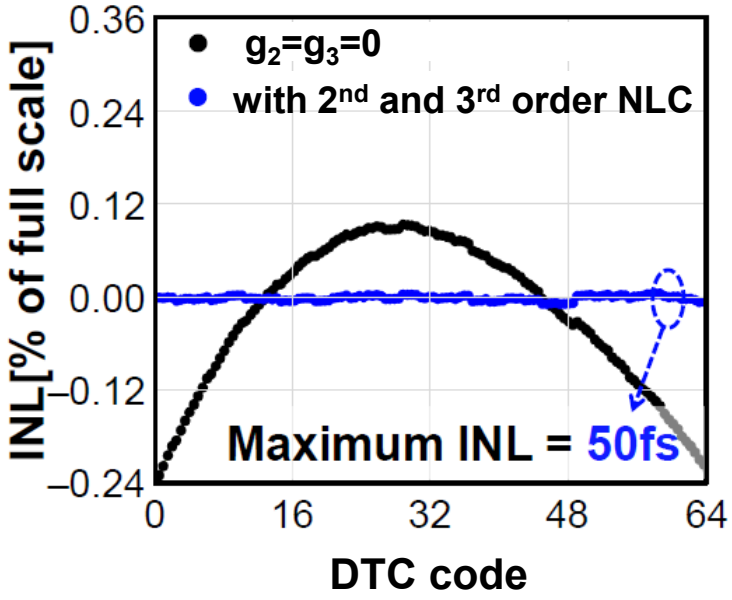
DTC NLC – Polynomial CAL

- Intrinsic INL of a RC-delay based DTC has strong 2nd order NL
- Use LMS loop to get DTC gain (g_1), as well as its 2nd and 3rd order component (g_2 and g_3); D_{AQ} is accumulated DSM phase error, $\Phi_e(n)$



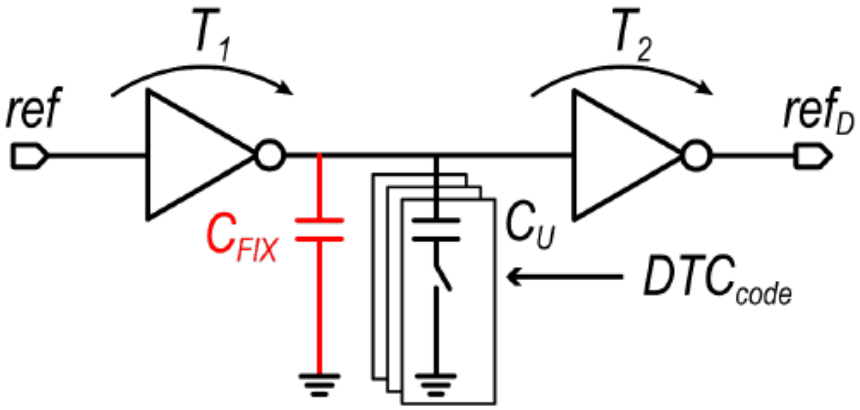
[H. Park ISSCC 2021]

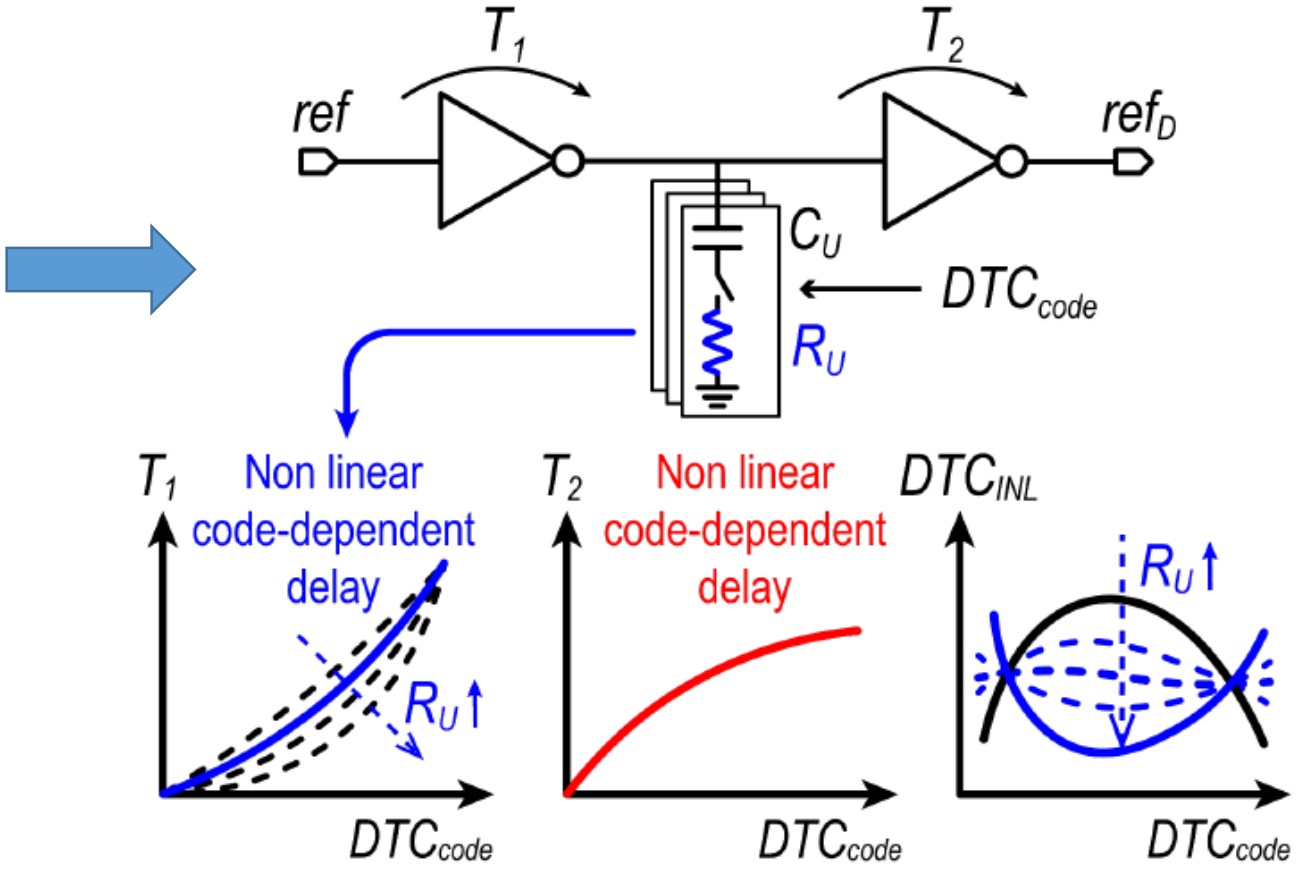




Reverse-Concavity Variable-Slope DTC

- **Conventional variable-slope DTC**





- **Change R_U to compensate NL**

  Voltage DAC controls R_U

  Adaptation loop find DAC code

[M.Rossoni ISSCC 2024]

DTC Range Reduction for Better Linearity

Recap DTC tradeoffs

- DTC Delay Range (*DR*): $DR \propto T_{VCO}$, DSM order
- DTC QN $\propto {t_{res}}^2$

$$DR = 2^n \cdot t_{res} = 2^n \cdot ln2 \cdot RC_{LSB}$$

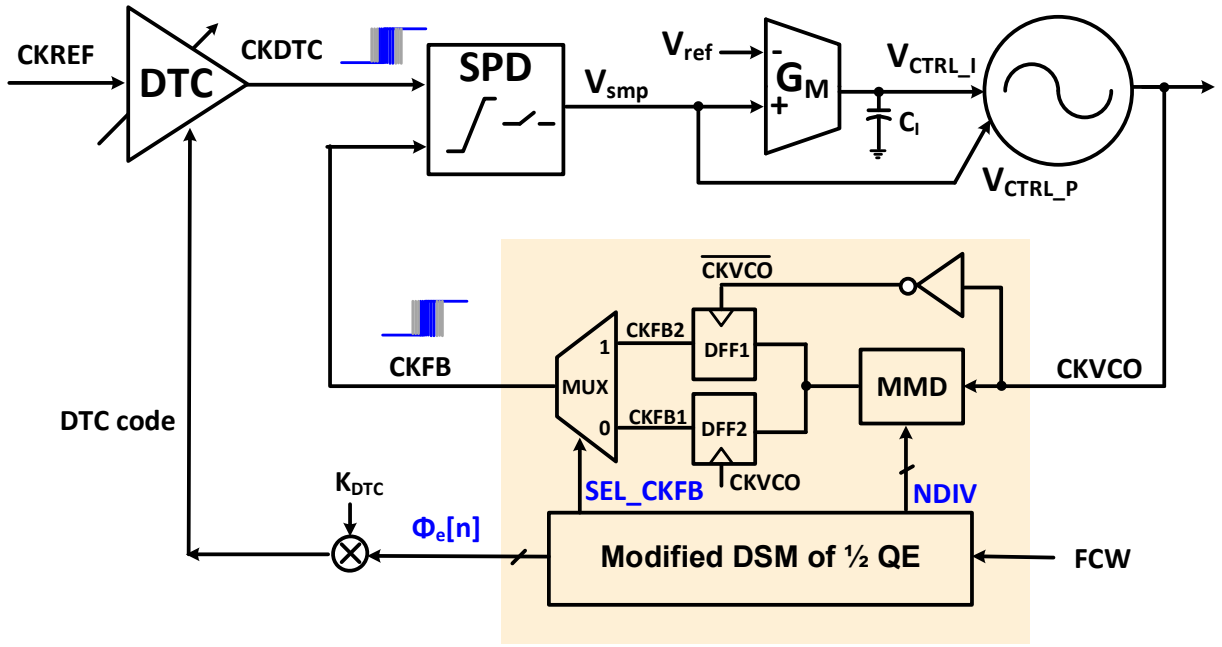
- DTC thermal noise $\mathcal{L} \propto DR$:

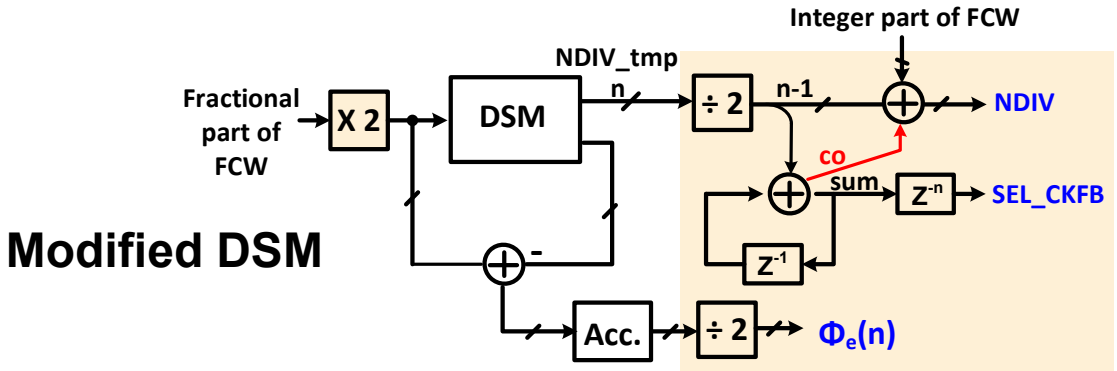
$$\mathcal{L} \cong 10 \cdot log_{10}\left[2kT \cdot f_{ref}\frac{(2\pi)^2}{ln\,2} \cdot DR \cdot R\right]$$

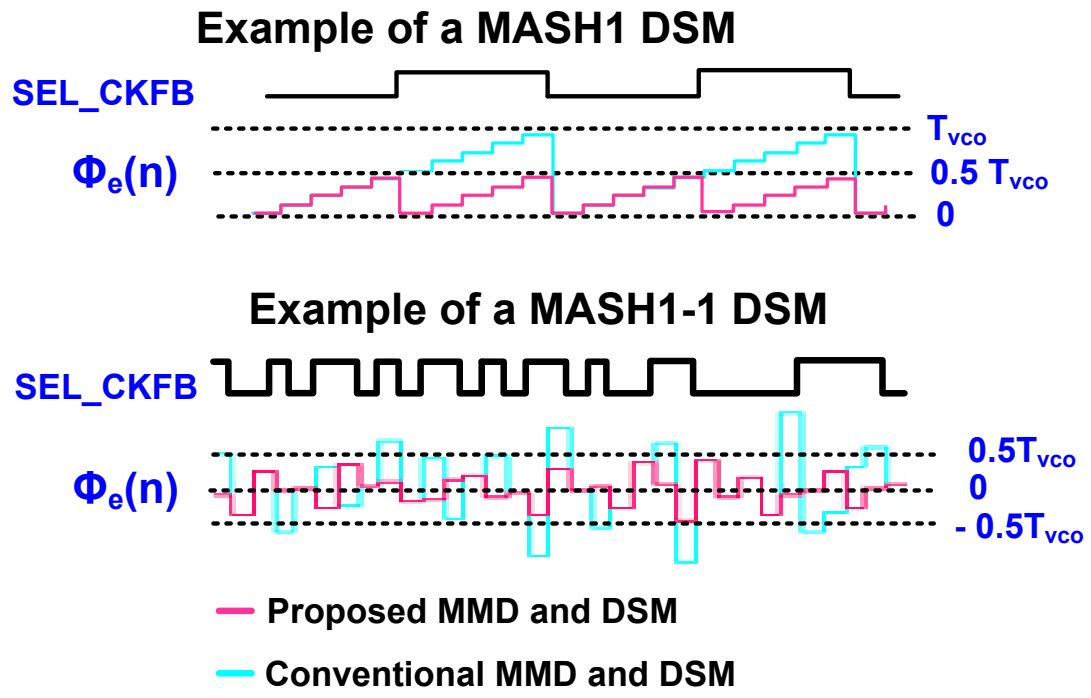
- DTC linearity better for smaller DR
- DTC power $\propto DR^2$

DR↓→ less bits, faster slope, lower noise and power, more linear

Half DTC Range with Two VCO Phases



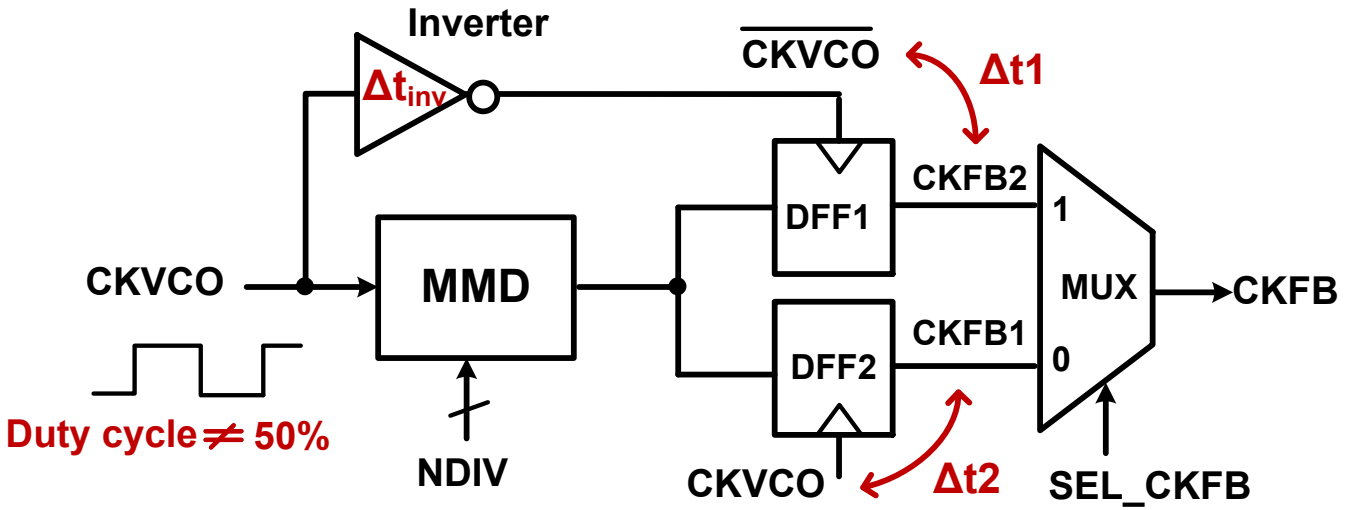


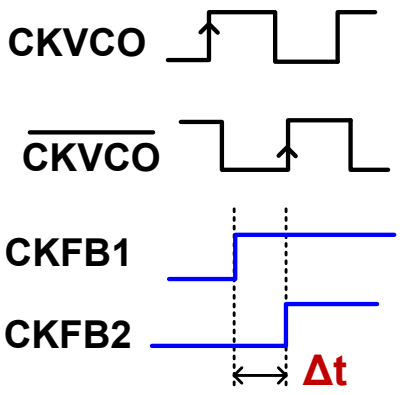


- **Switching from CKFB1 to CKFB2 introduces a half-period delay**

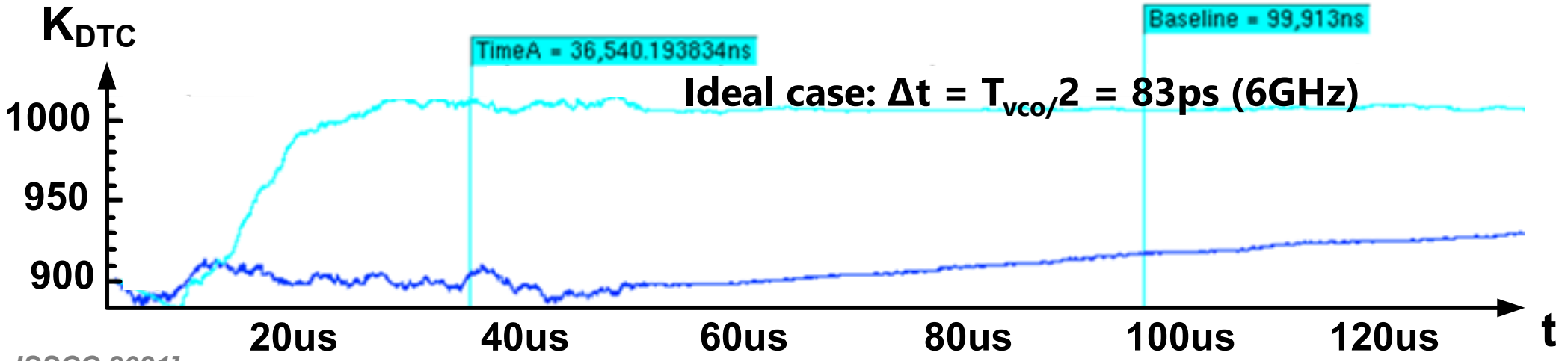
[W. Wu ISSCC 2021]

VCO Duty Cycle Error Disrupts K_{DTC} CAL



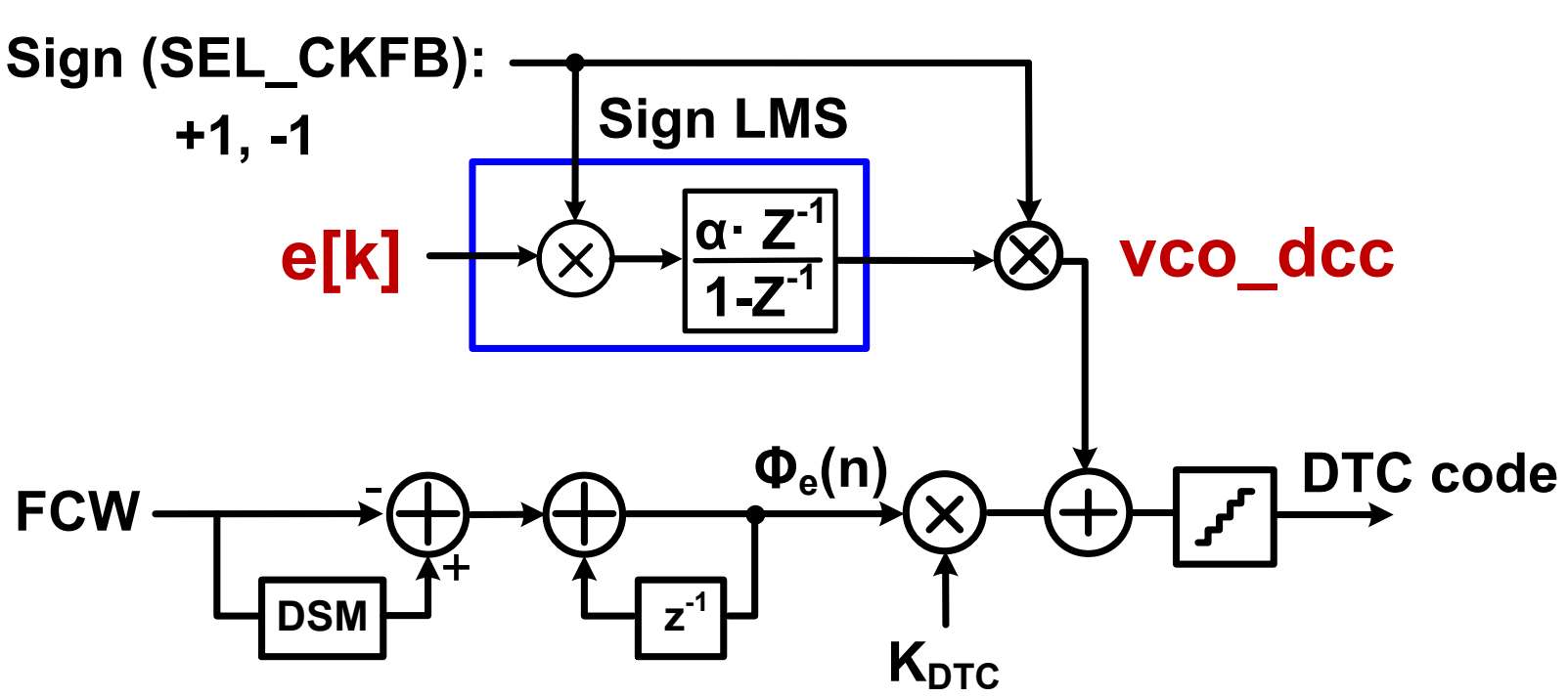


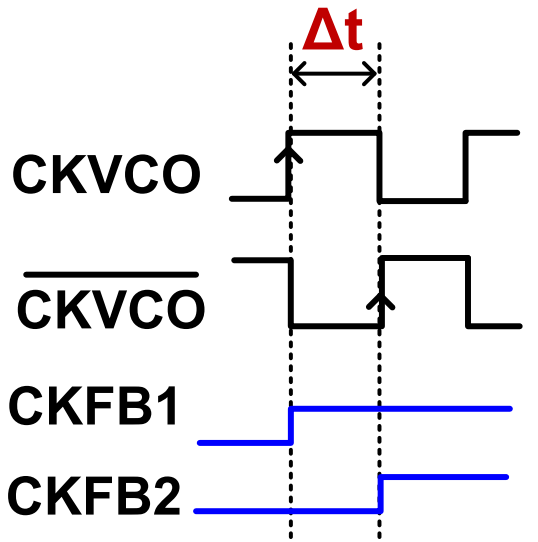
$\Delta t_{err} = \Delta t - T_{vco}/2$



[W. Wu ISSCC 2021]

VCO Duty Cycle Calibration



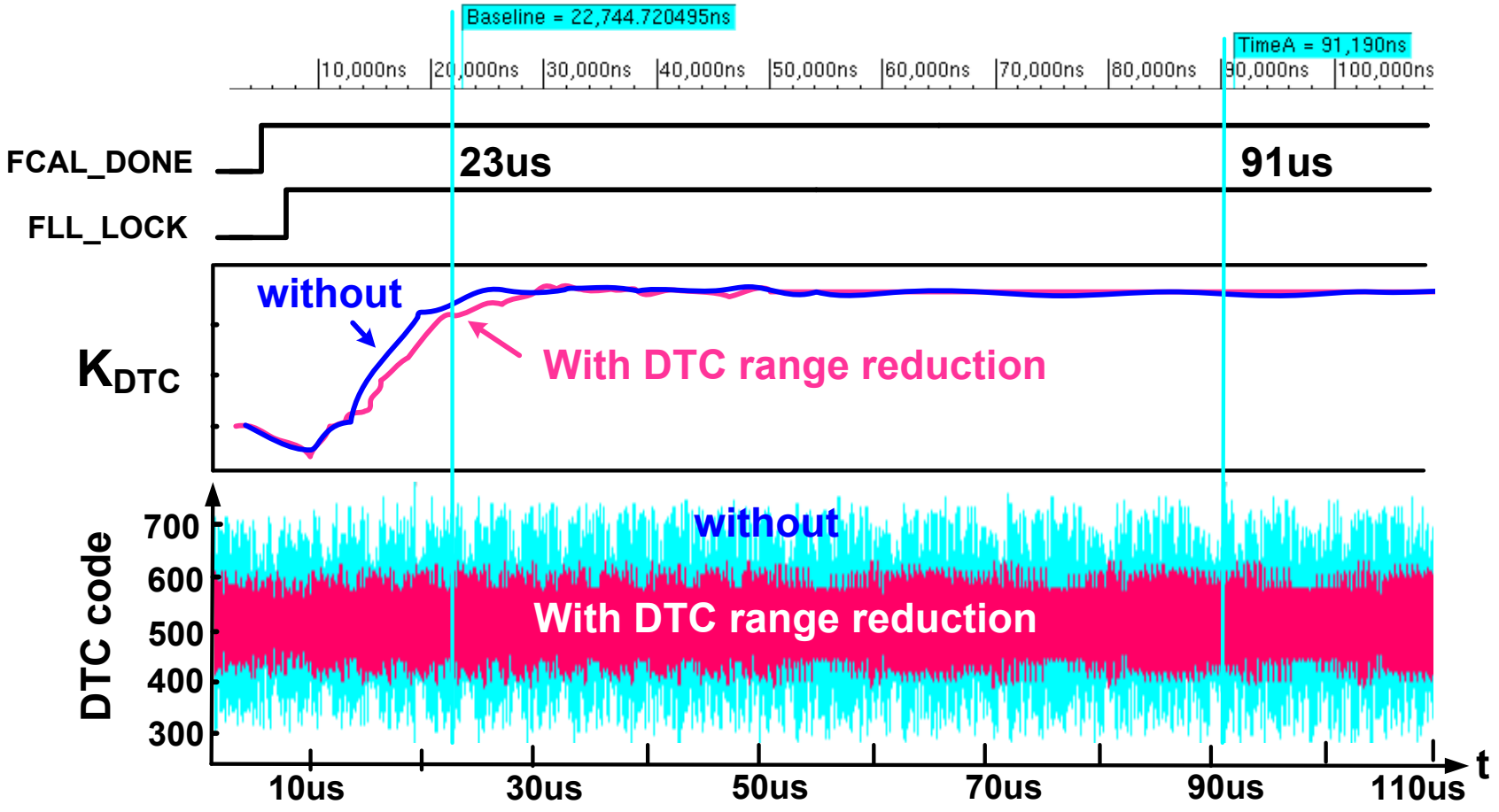


$\Delta t_{err} = \Delta t - T_{vco}/2$

- SEL_CKFB = +1 → push back CKDTC by $\Delta t_{err}/2$
- SEL_CKFB = -1 → pull-in CKDTC by $\Delta t_{err}/2$

[W. Wu ISSCC 2021]

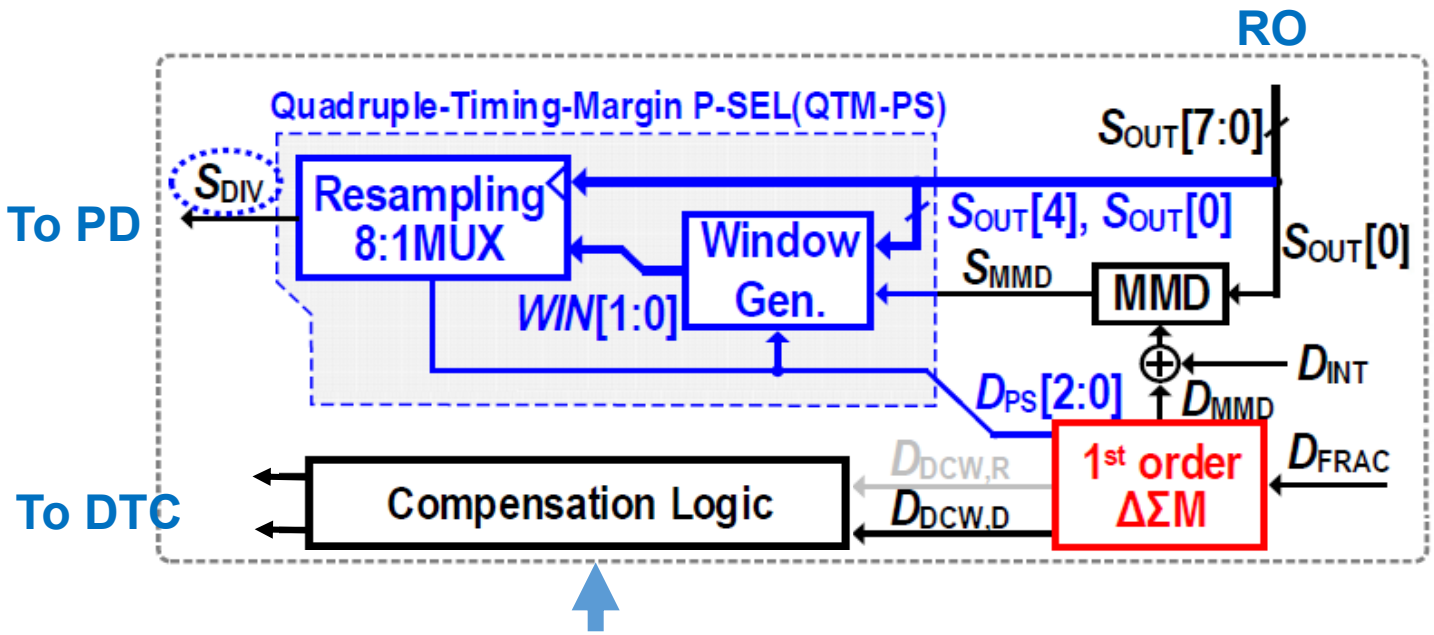
Simulated K_{DTC} CAL and DTC Code



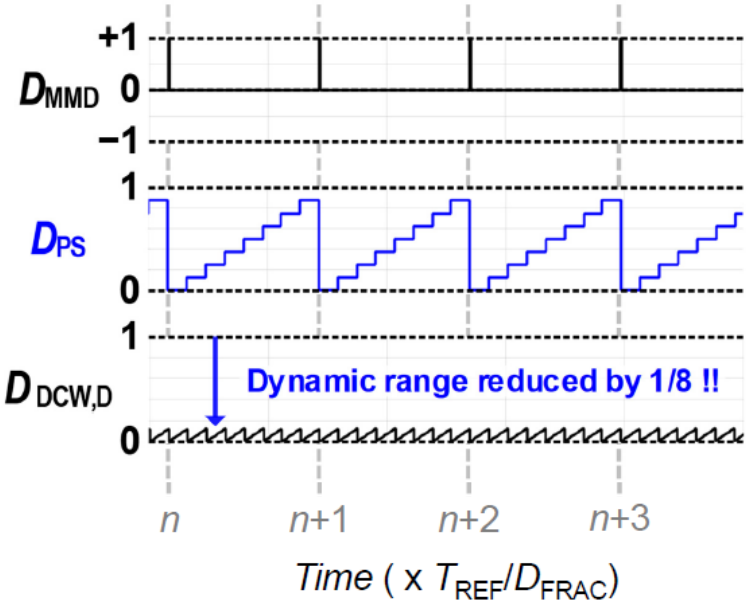
- KDTC converges < 30µs, even with 12% VCO duty cycle error
- DTC code range is halved

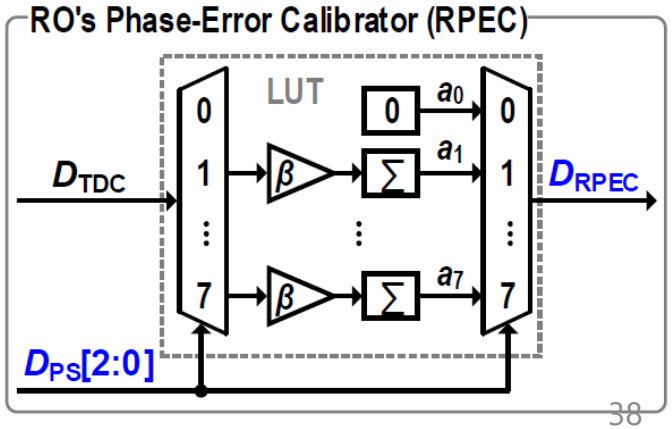
1/8 DTC Range Reduction Using 8 RO Phases

- $S_{OUT}[7:0]$ are 8 phases from differential ring oscillator
- Timing of QTM-PS is stringent



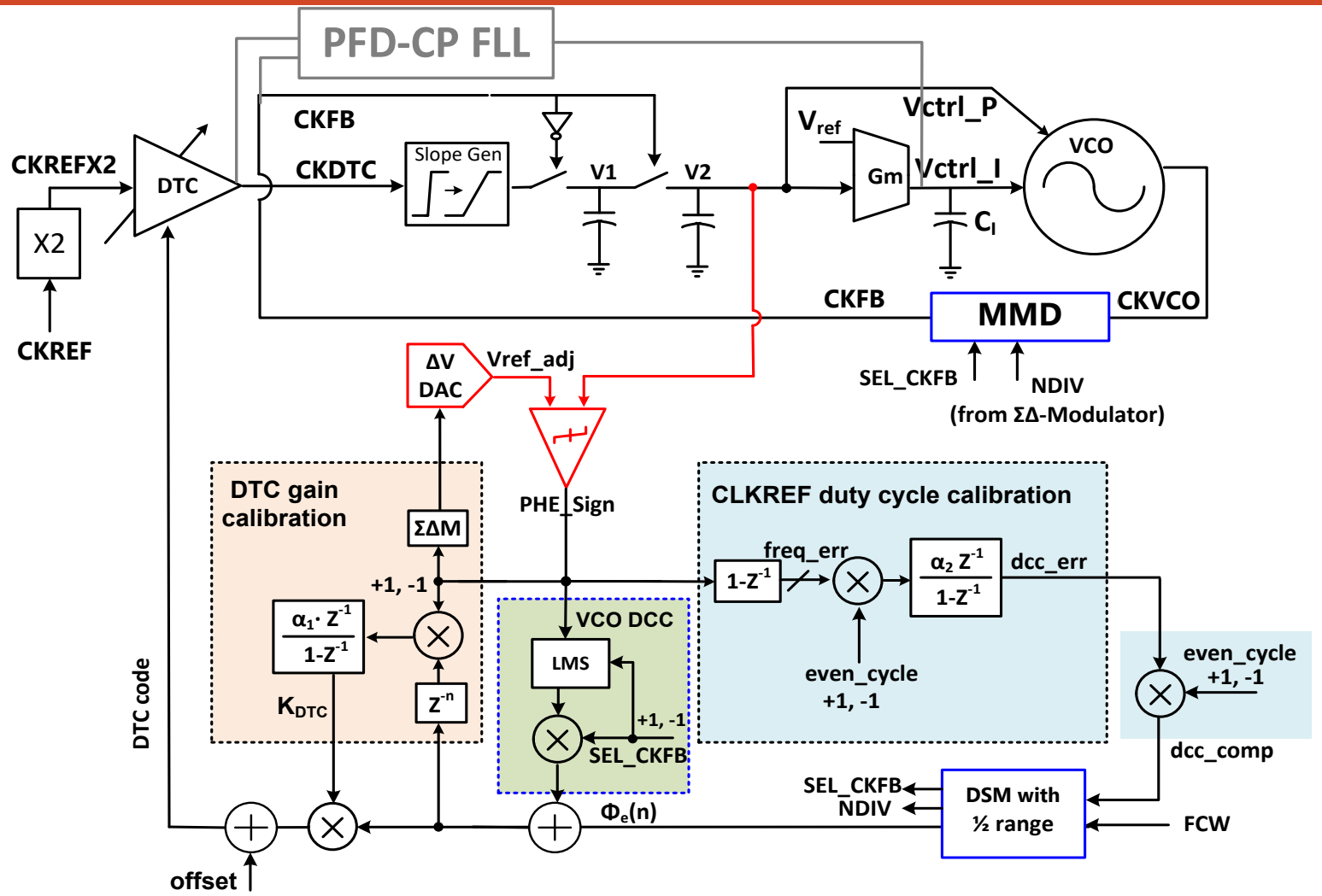
Codes for DTC gain, RO phase mismatch (D_{RPEC}) from background LMS-based calibrations





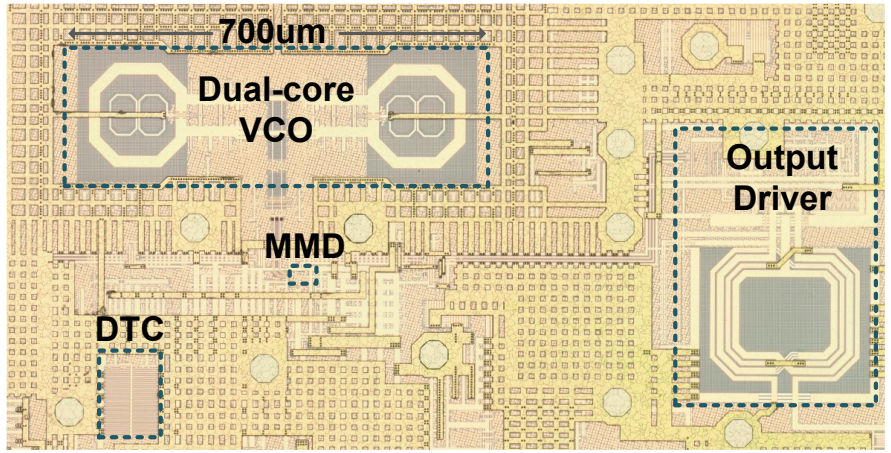
[C. Hwang ISSCC 2022]

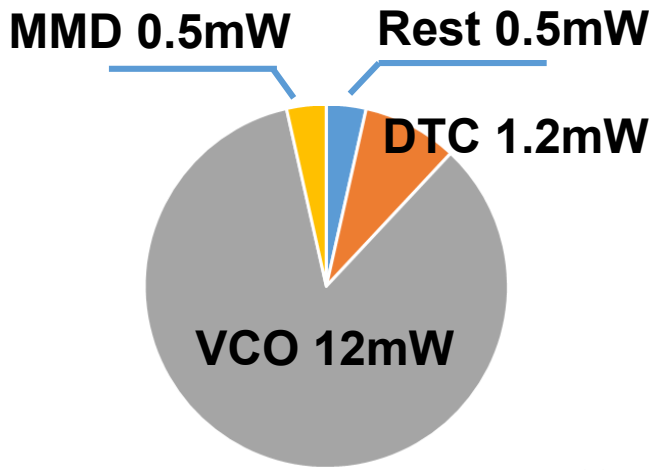
Low Jitter Sampling Analog PLL Example



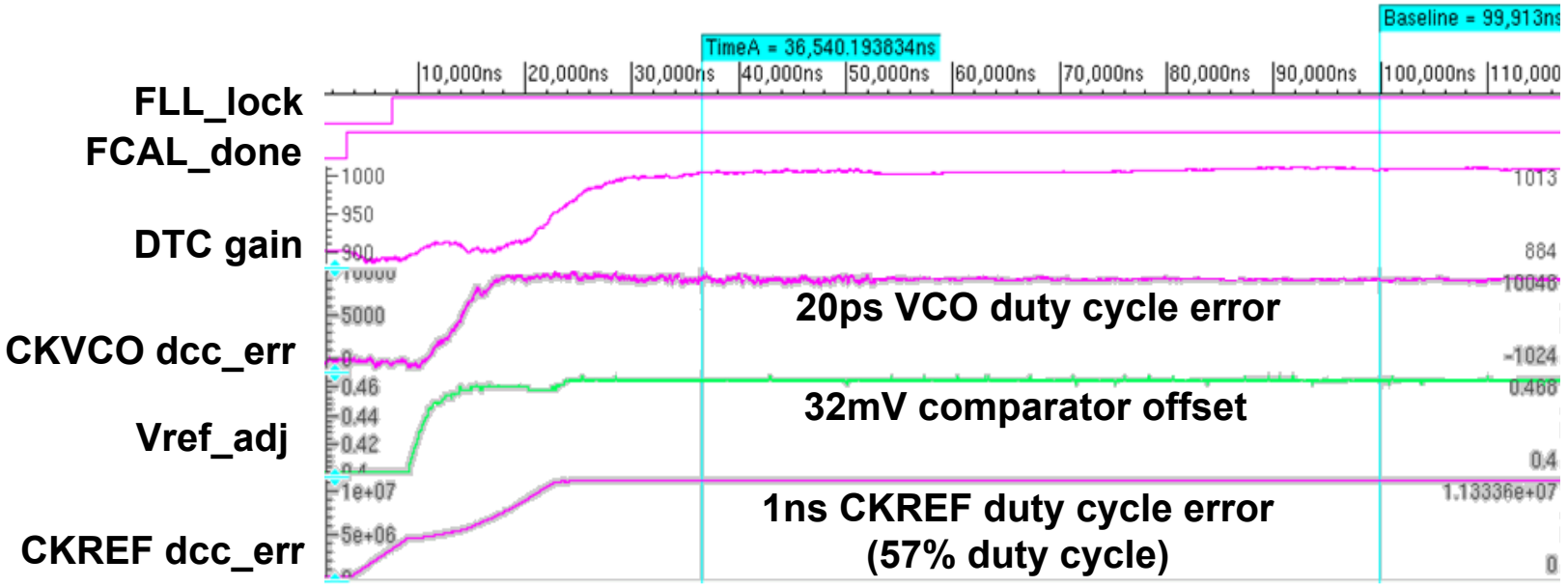
[W. Wu ISSCC 2021]

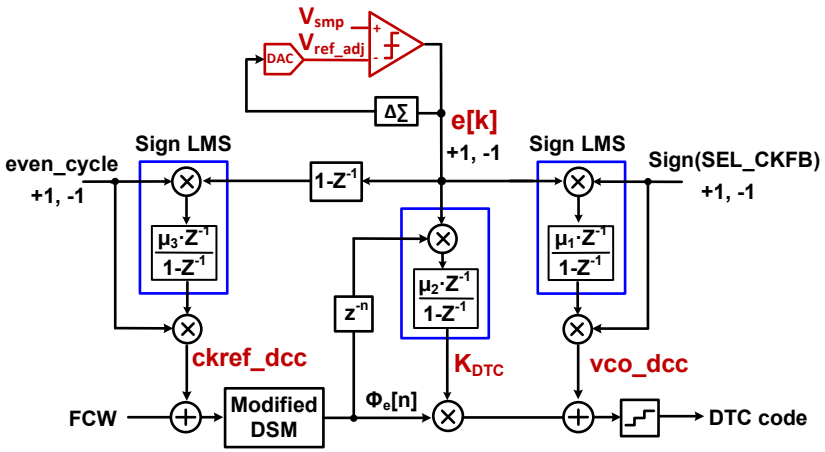
- 14nm FINFET, Core 0.31mm²





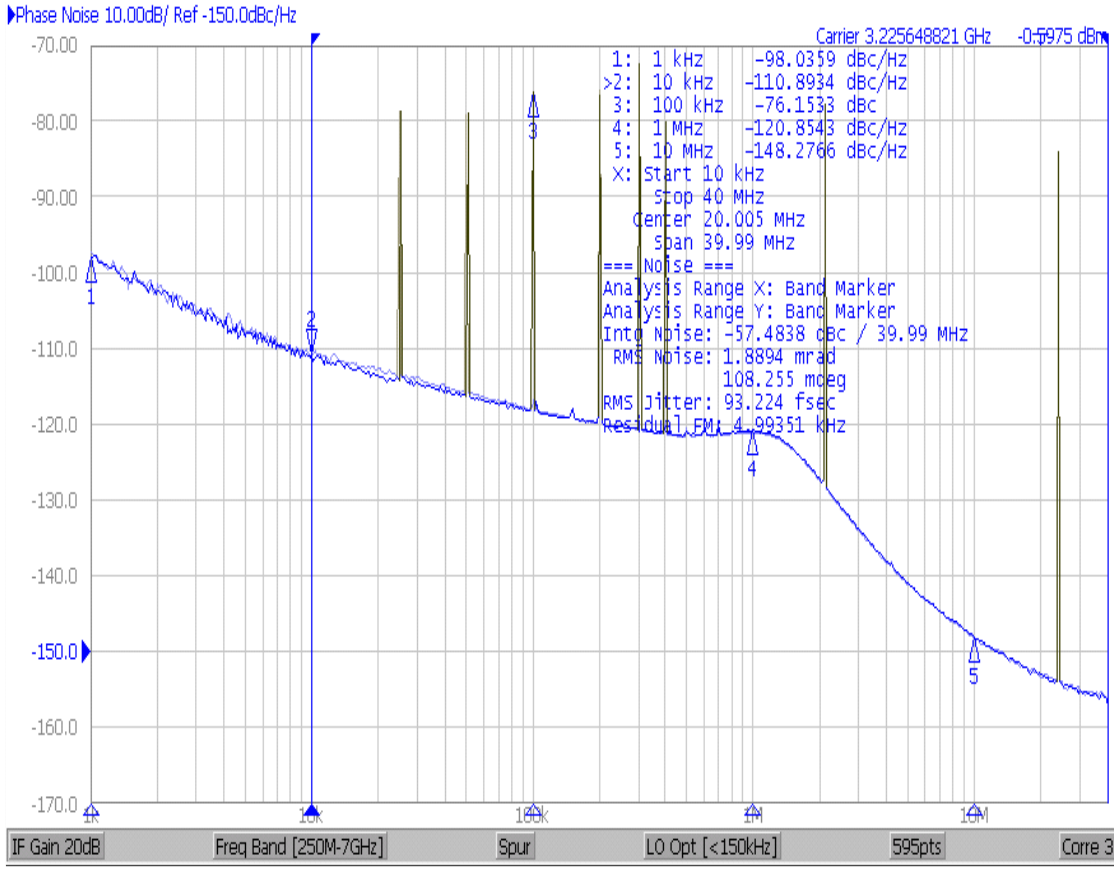
Simulated Background Calibration



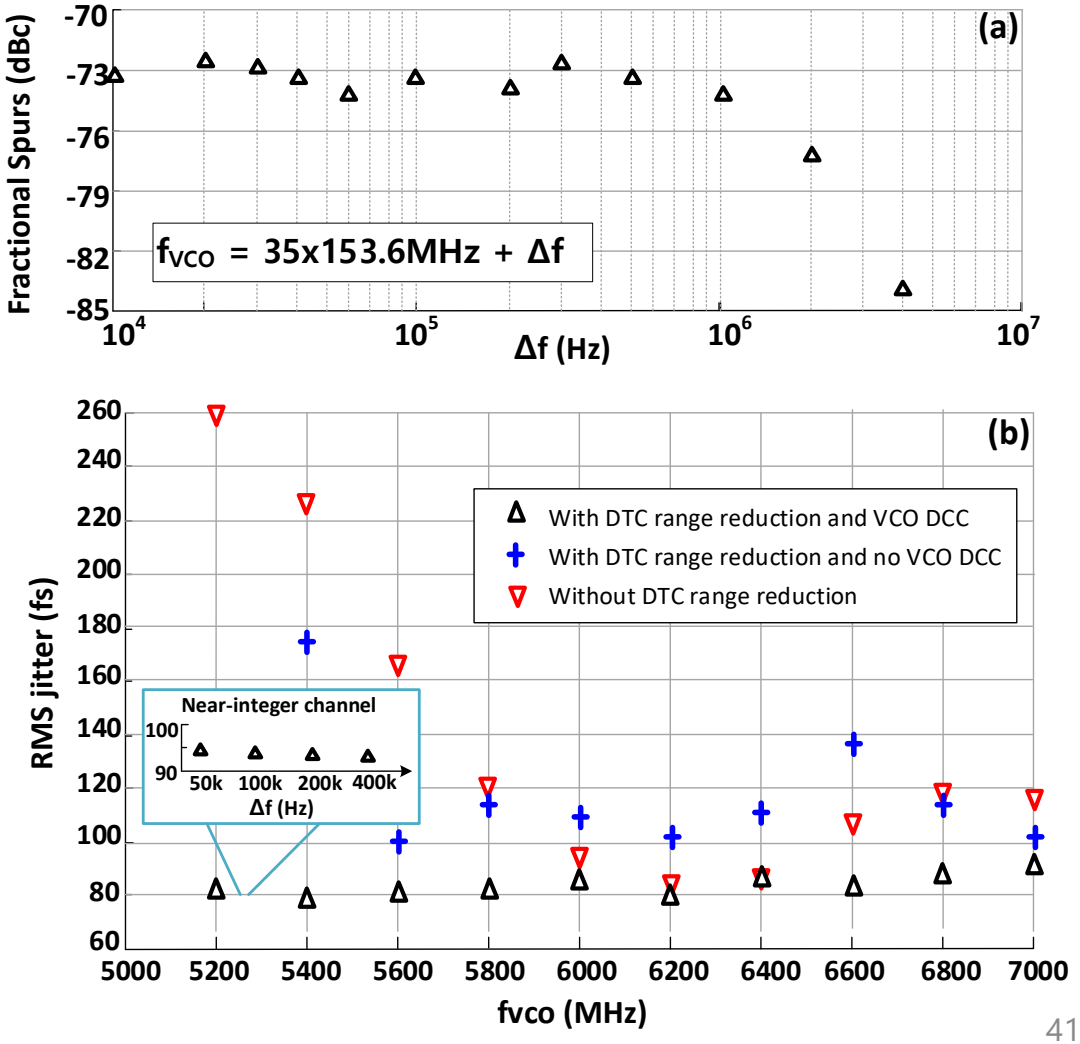


- All calibrations converge < 30us and track PVT
- Works robustly for both integer and fractional channels

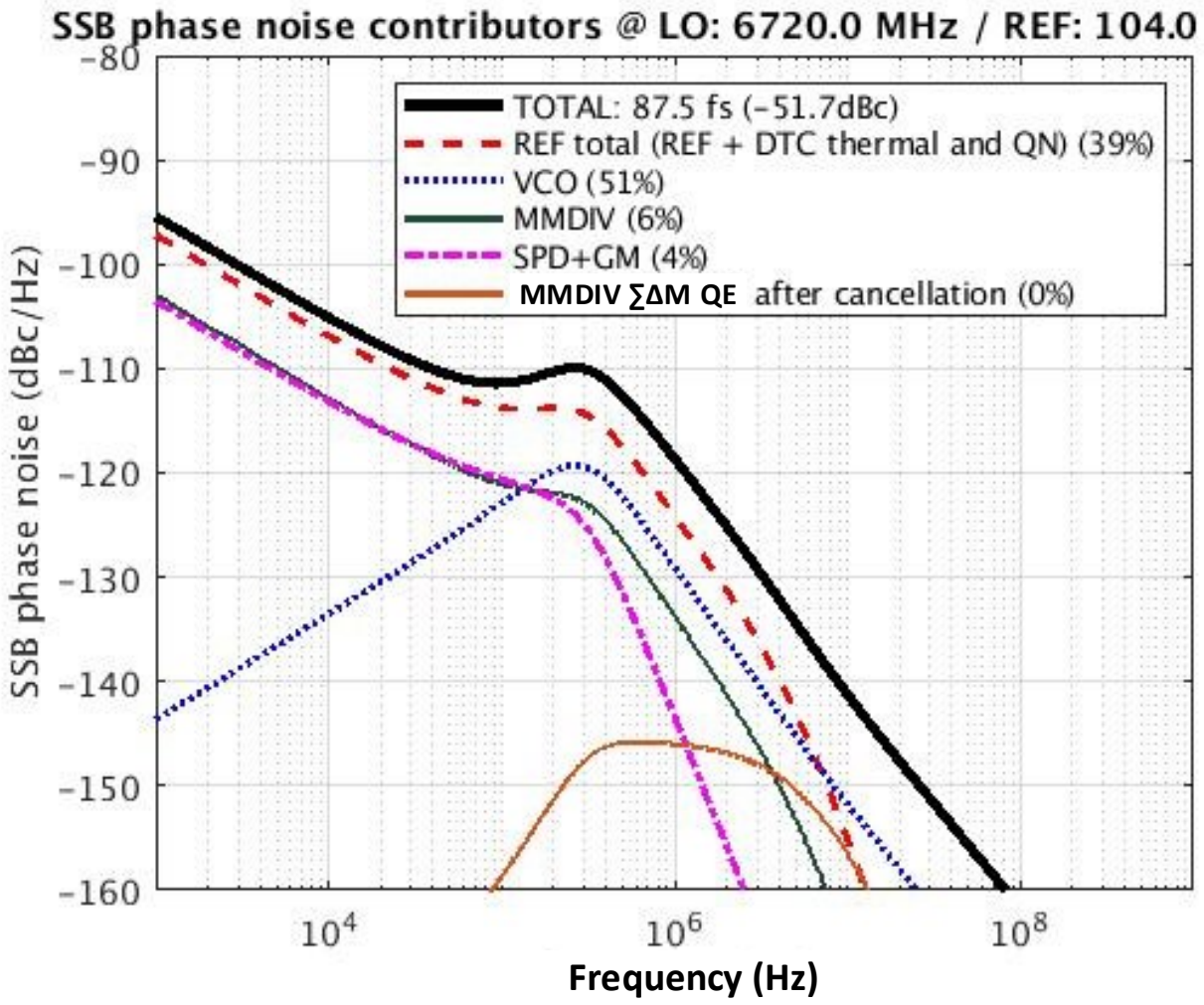
Measured Fractional-N Spurs and Jitter



[W. Wu ISSCC 2021]



PN Contributors in Low-Jitter DTC-Assisted PLL



After suppress noise from PD, DSM QN, MMD →

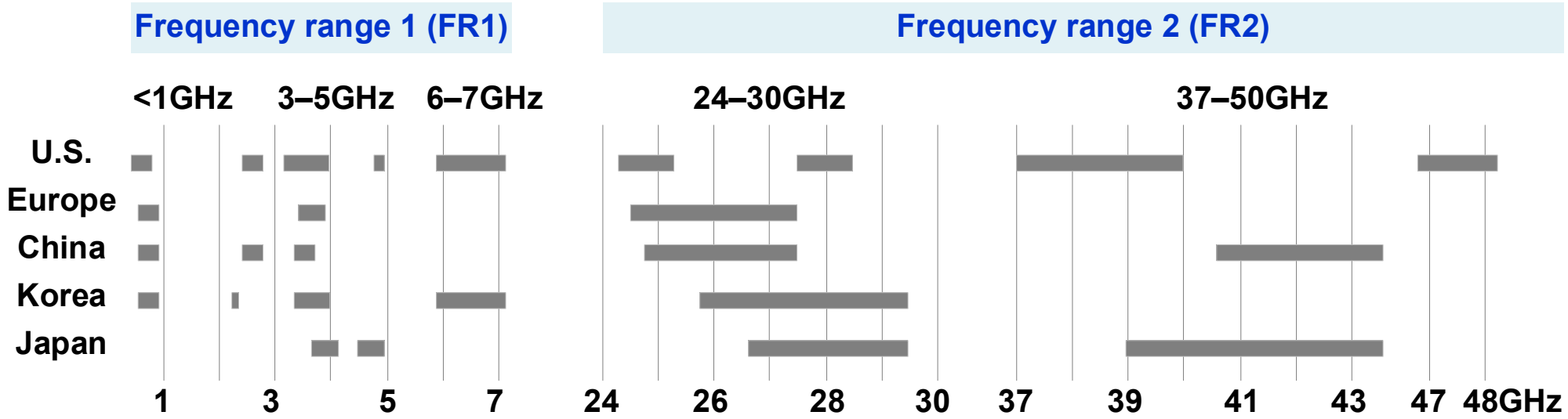
- ❑ **PLL IPN is dominated by**
  - ■ **CKREF – external clock ref.**
  - ■ **VCO/DCO**
- ❑ **PLL BW is chosen to tradeoff the contribution of the two**

→ Common for any PLLs

Outline

- Fractional-N PLL Design Challenges
- PLL Architecture Review
- DTC-Assisted Phase Detector Design
- Digital Calibrations to Enhance PLL Performance
- **LO Chain Design Example for 5G NR**

5G New Radio Frequency Bands

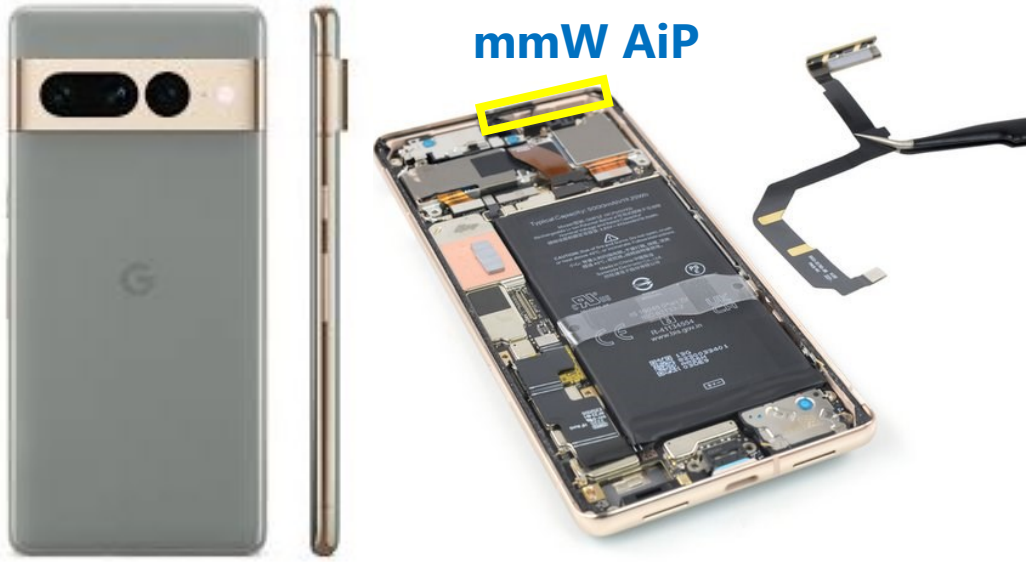


5G FR2 Band	Uplink/Downlink (GHz)	Channel bandwidth (MHz)
N257	TDD 26.5 – 29.5	50, 100, 200, 400
N258	TDD 24.25 – 27.5	50, 100, 200, 400
N259	TDD 39.5 – 43.5	50, 100, 200, 400
N260	TDD 37.0 – 40.0	50, 100, 200, 400
N261	TDD 27.5 – 28.35	50, 100, 200, 400

Smart Phones with 5G mmW Chipset

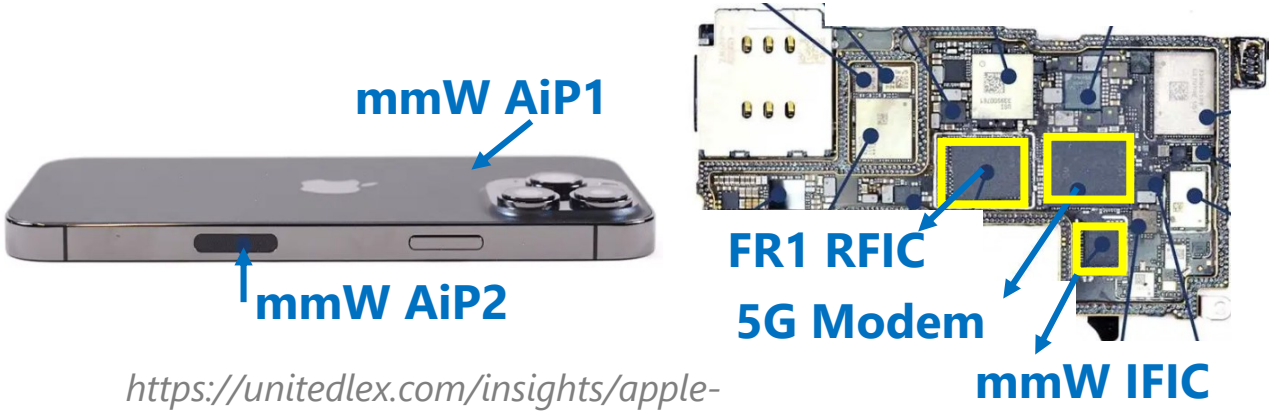
- **FR2 system**

  Modem + mmW IFIC + mmW AiP



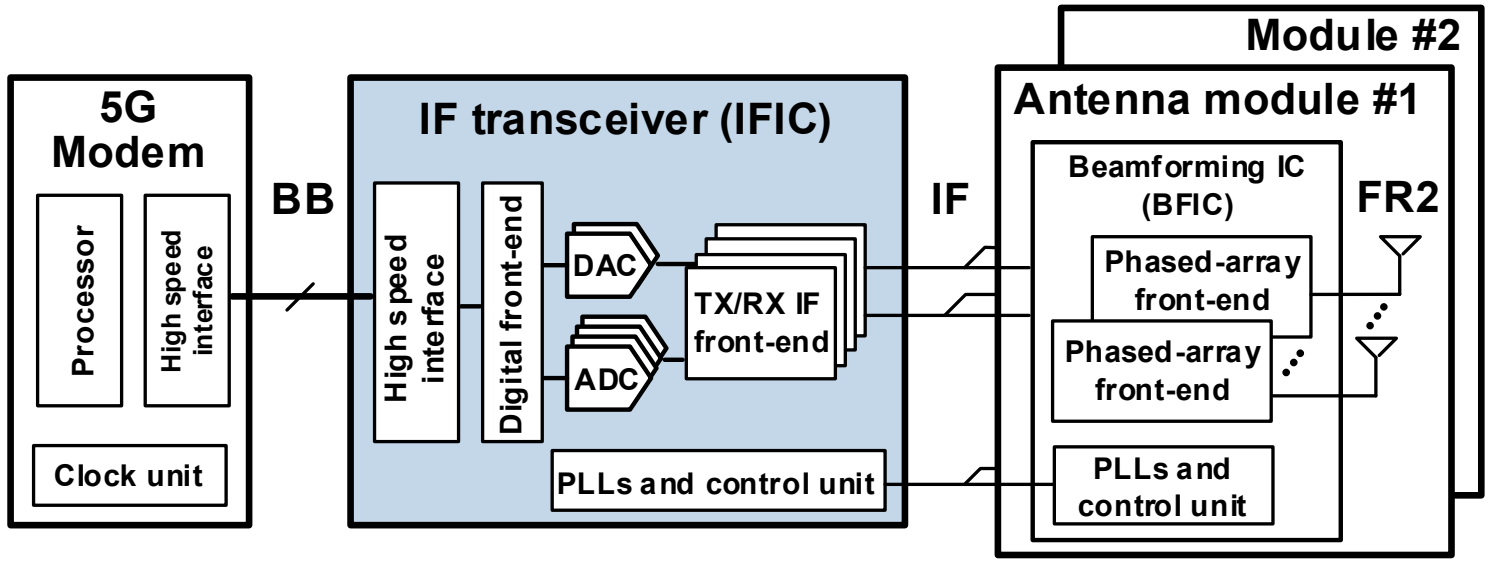
https://www.ifixit.com/Guide/Google+Pixel+7+Pro+5G+mmWave+Antenna+Replacement/154719

https://www.techinsights.com/blog/muratasamsung-2nd-gen-mmwave-aip-discovered-samsung-galaxy-a53



https://unitedlex.com/insights/apple-iphone-13-pro-max-teardown-report/

LO Design Challenges for 5G mmW

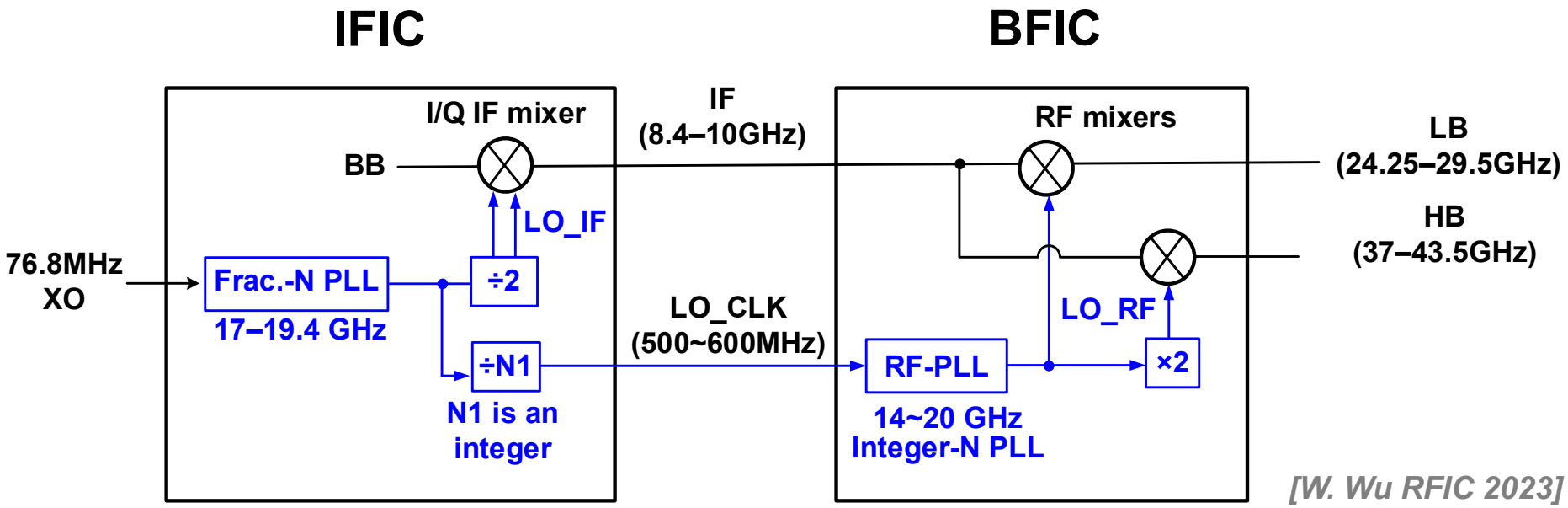


FR2 Band	Uplink/Downlink (GHz)	
N257	TDD 26.5 – 29.5	LB
N258	TDD 24.25 – 27.5	
N261	TDD 27.5 – 28.35	
N260	TDD 37.0 – 40.0	HB
N259	TDD 39.5 – 43.5	

- mmW LO circuitry on both IFIC and BFIC
- Transceiver SNR is limited by LO IPN
- Multi-band support with low power and low cost
- 256-QAM support demands low jitter LO

LO Topology Considerations

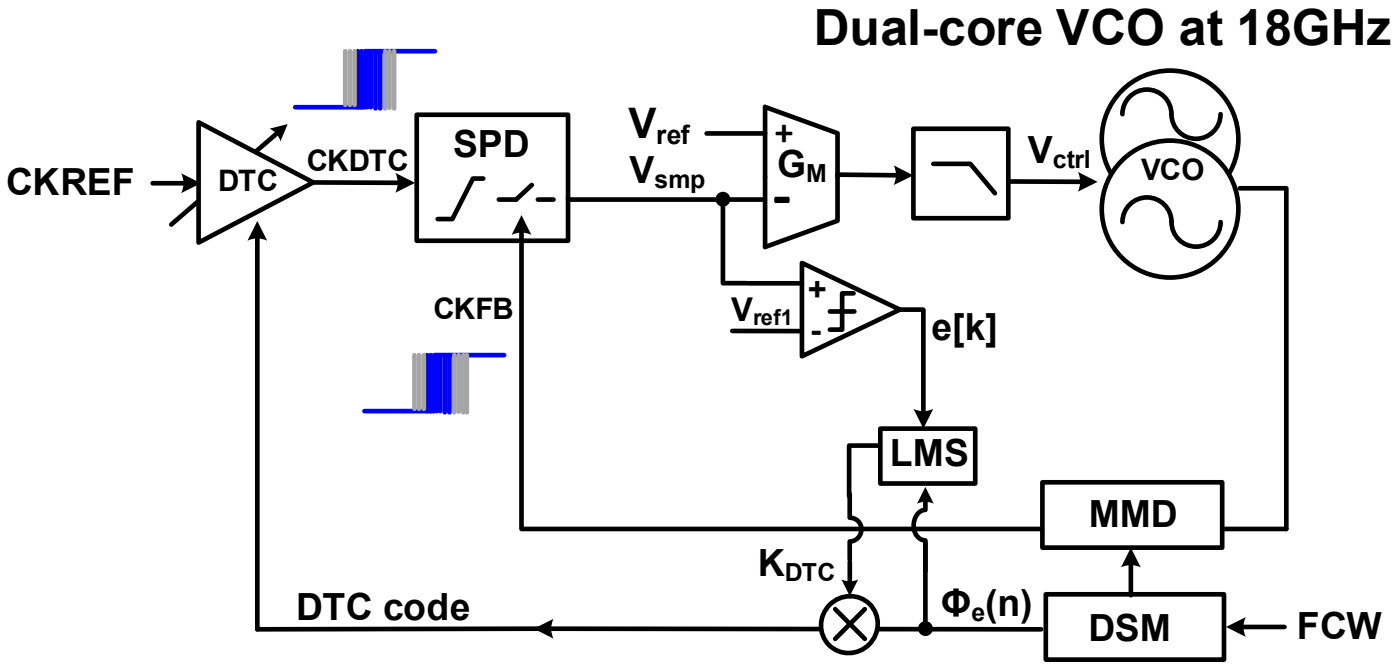
- IFIC generates LO_IF & reference clock (LO_CLK) for BFIC
- Low-jitter frac.-N PLL dominates LO chain IPN
- BFIC PLL simplifies to an integer-N of wide BW (e.g., SSPLL)
  - Low-power as VCO PN is relaxed
  - Compact area: one wideband VCO for both LB and HB

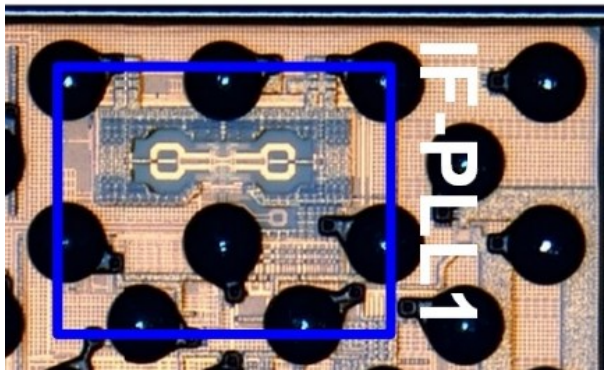


[W. Wu RFIC 2023]

Low-Jitter Fractional-N PLL Directly at mmW

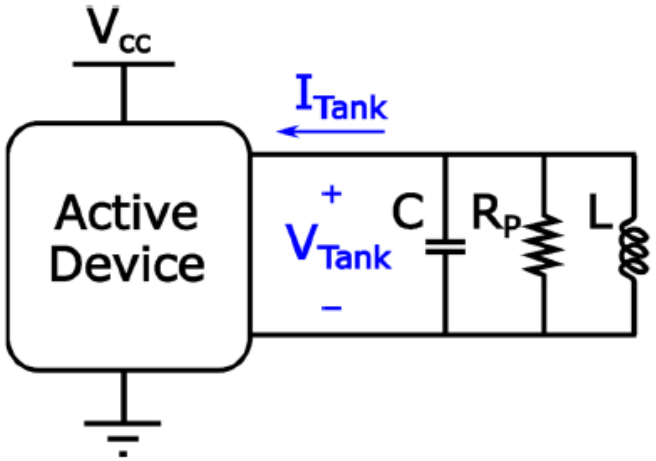
- DTC-based sampling PLL
  → low jitter
- VCO operates at 18 GHz
  → no multiplier, low power
- Dual-core VCO → low jitter





[W. Wu RFIC 2023]

Low PN LC Oscillator Design



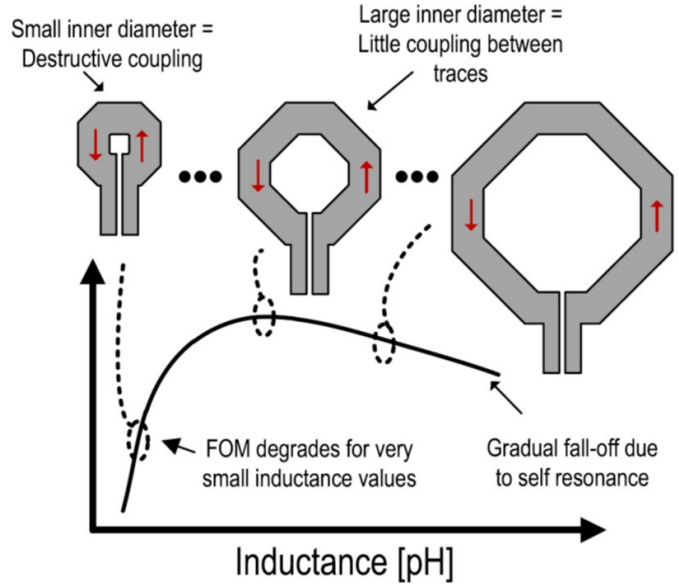
$$PN_{dB} = 10log_{10}\left[\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \frac{2FkT}{P}\right] = 10log_{10}\left[\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{FkT\omega_0}{V_{Tank}^2}\frac{L}{Q}\right]$$

Resonator power $P = \frac{V_{Tank}^2}{2R_p} = \frac{V_{Tank}^2}{2\omega_0 LQ}$

- V_{Tank}, F set by process
- Scaling L as long as $\frac{L}{Q}$ can be reduced to lower PN
- Beyond this limit → use multi-core oscillator

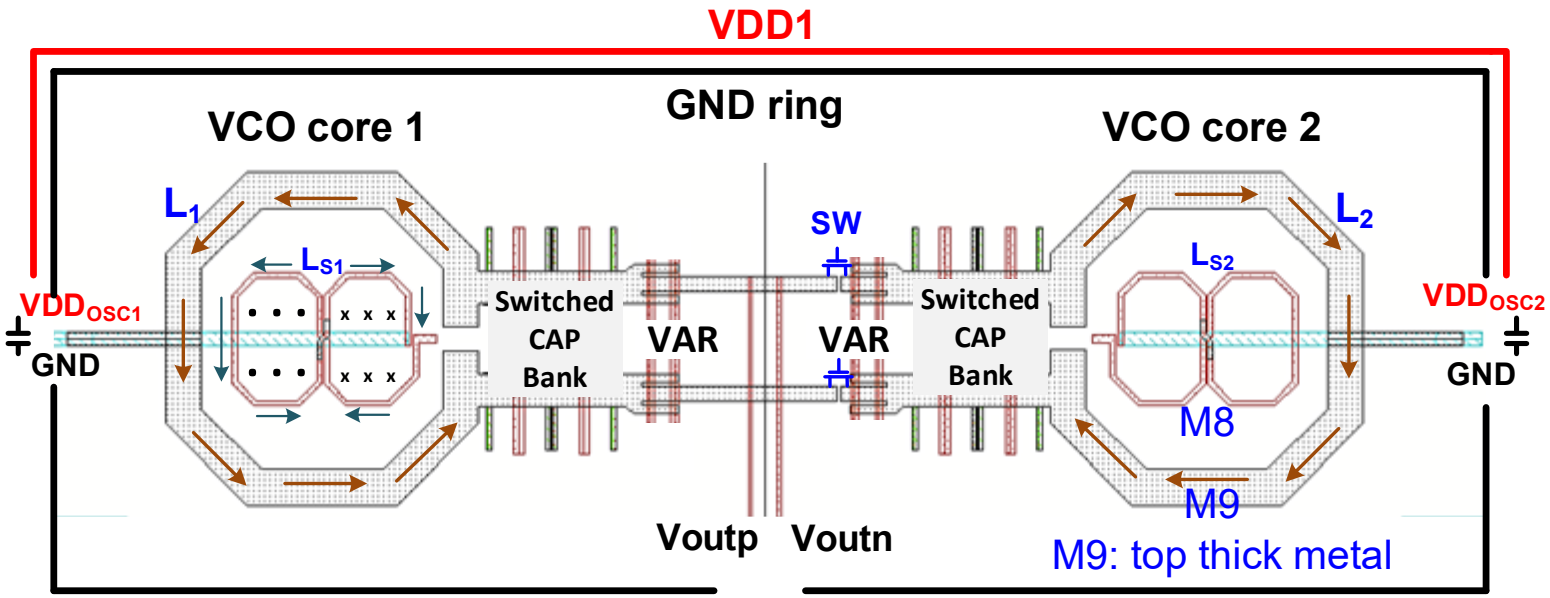
$L_{eq} = L/N, C_{eq} = N \cdot C$ → same ω_0, same Q

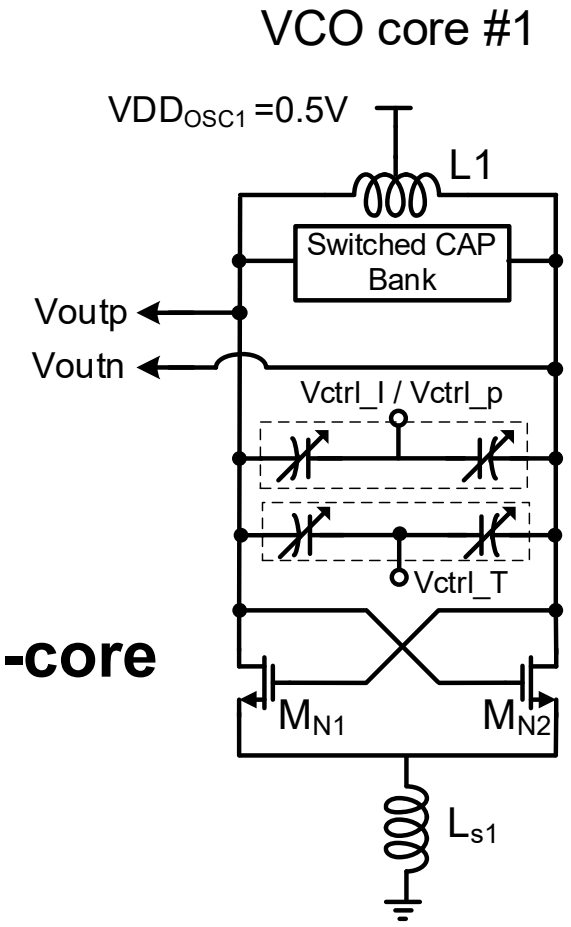
$$PN_{multi-core} = PN_0 - 10log_{10}(N)$$



[D. Murphy JSSC Nov 2018]

Switchable Dual-core VCO for Power, PN Tradeoff





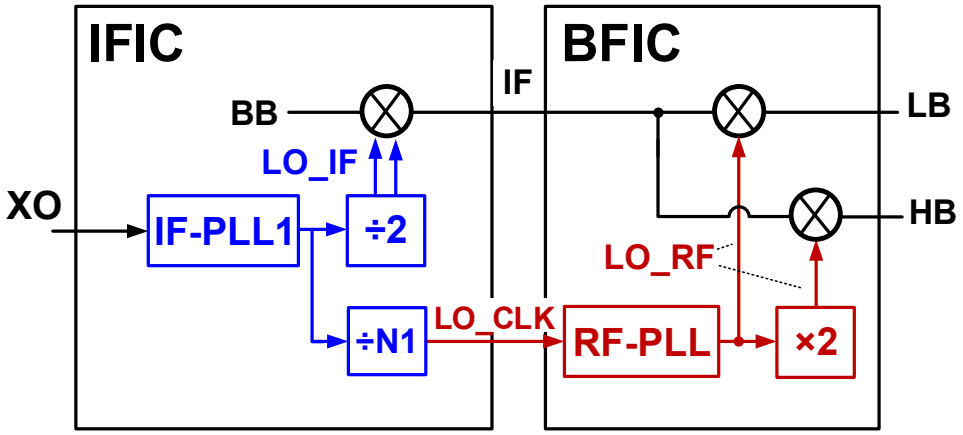
- Good EM isolation, symmetrical → same f_{vco} for 1- or 2-core
- Figure-8 tail L_s put inside main L to save area
- N=1: -120 dBc/Hz @1MHz measured at 6GHz
- N=2: -122.5 dBc/Hz

[W. Wu ISSCC 2021]

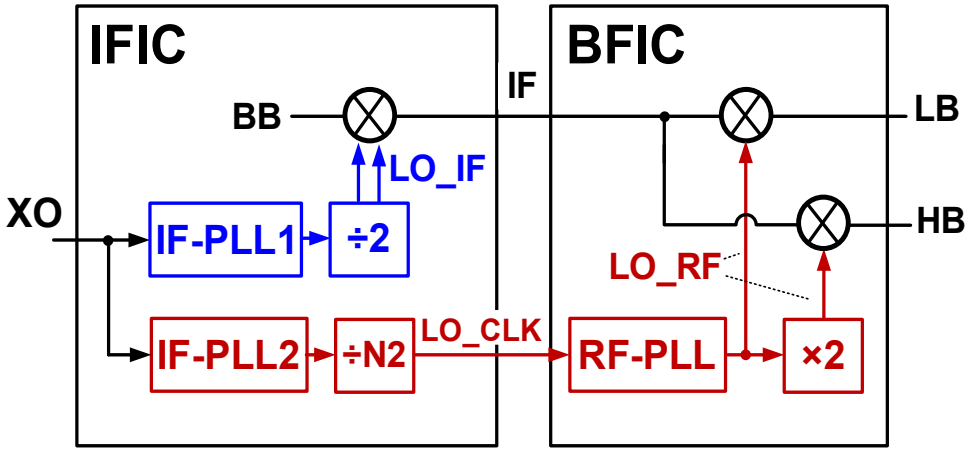
LO Configuration to Further Improve IPN

- 256-QAM requires rms jitter of ~100 fs
- Hard to further reduce rms jitter of IF-PLL → use two IF-PLLs
- PN of LO_IF and LO_RF are mostly uncorrelated → lower chain IPN

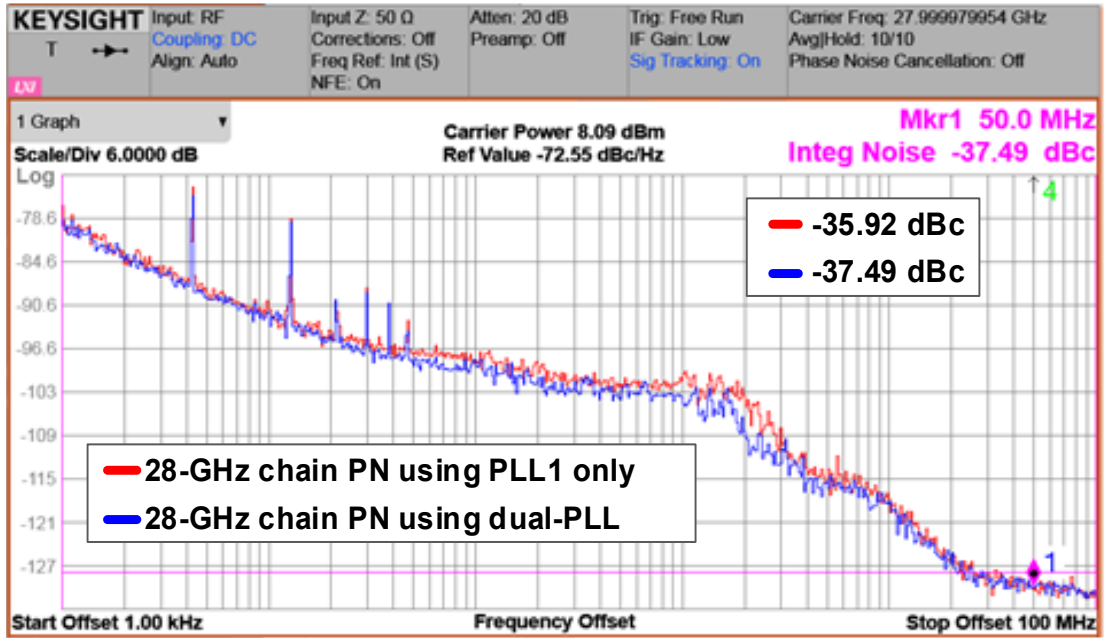
Low-power mode for 64-QAM/QPSK

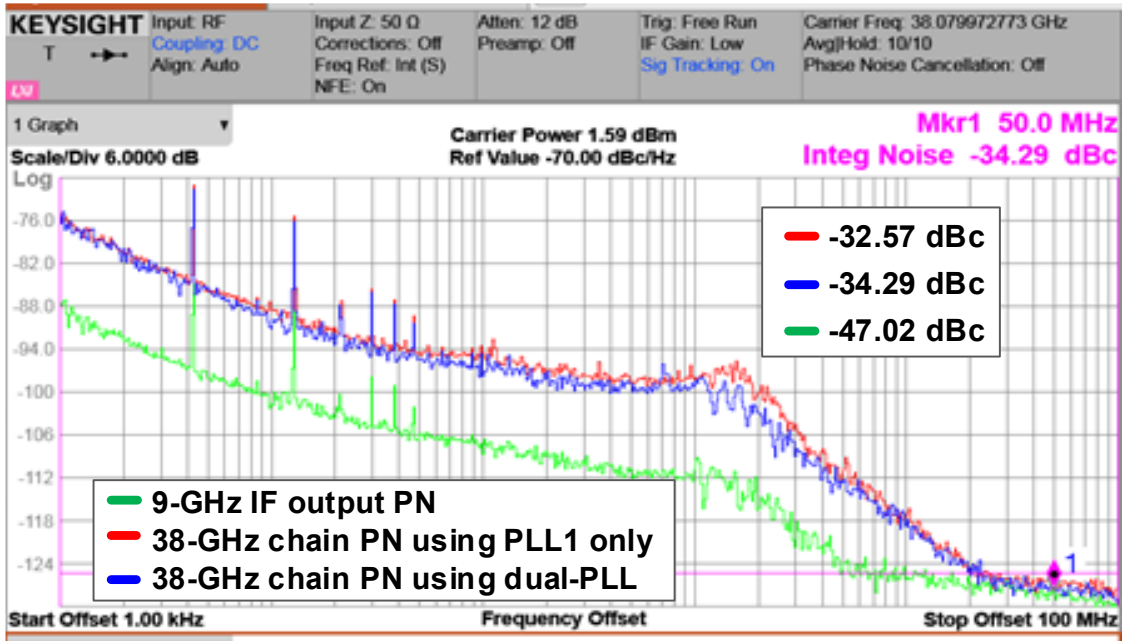


Low-jitter mode for 256-QAM



Measured Chain IPN at 28 GHz and 38 GHz





[W. Wu RFIC 2023, Samsung]

- **Dual-PLL results in ~1.6 dB lower chain IPN**
- **-37.49 dBc IPN at 28 GHz → EVM floor of 1.34%**
- **-34.29 dBc IPN at 38 GHz → 112 fs rms jitter, EVM floor of 1.9%**

Summary

- Advanced wireless application requires frac. N PLLs of < 100 fs_{rms}
- PLLs with DTC-assisted PD have demonstrates low jitter, high FoM
- DTC cancels DSM QE → eases PD design
- Various design techniques aim to improve DTC linearity
- Intensive digital calibrations enhance PLL performance
- Multi-core VCO breaks design limit of single core with same VCO FoM

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