VIETNAM NATIONAL UNIVERSITY HANOI (VNU)
VNU INFORMATION TECHNOLOGY INSTITUTE

Design-to-Tapeout

using Open-Source Design Tools

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AIoT Research Laboratory

Outline

- Design with Caravel Harness
  - caravel_user_project
  - caravel_user_project_analog
  - SRAM macros
- Mixed-signal design implementation using the digital flows
  - Module implementation
  - Top-level integration
  - DRC/LVS debugging
- Some layout techniques to use the digital router
  - Layout analog blocks for digital flow
  - Exporting GDS and abstract view (LEF)

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Fabricate a chip in less than three months

early, 2021

- Heard about Google Open MPW & intereted

April, 2021

- Call for Google Open MPW-2 submission
- Form a team & decided to submit VCO-based ADC

June 18, 2021

- Submit the design for Google Open MPW

June 24, 2021

- Get sponsored by SSCS PICO program

Oct., 2021

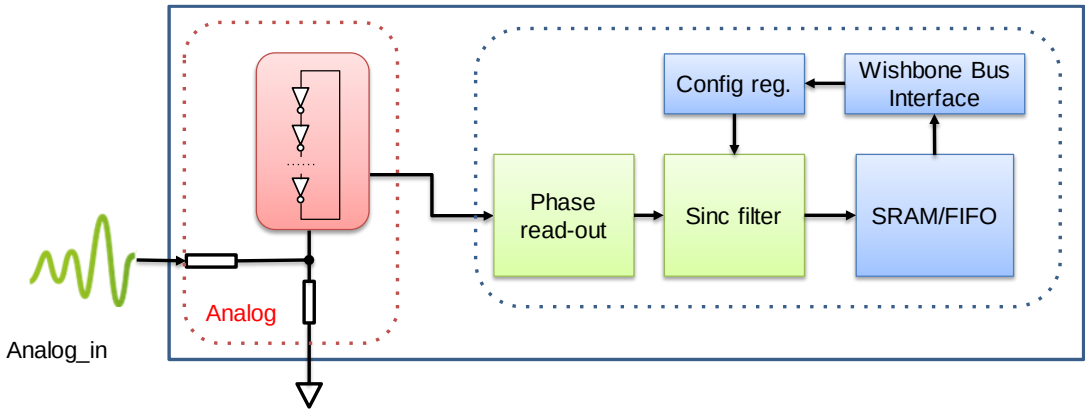
- Timing issue with MPW-2 discovered

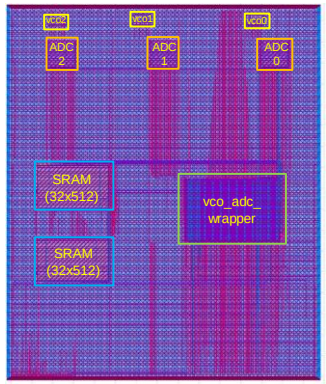
Nov., 2021

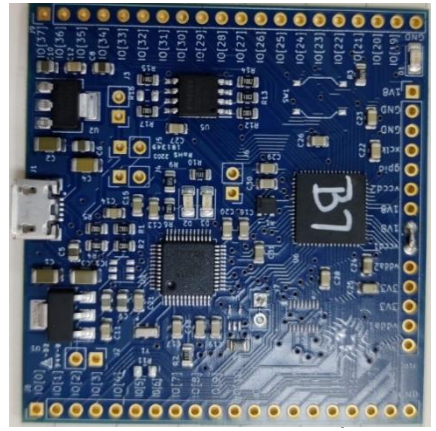
- Resubmission for MPW-3

Feb., 2022

- Receive the chips & testboard

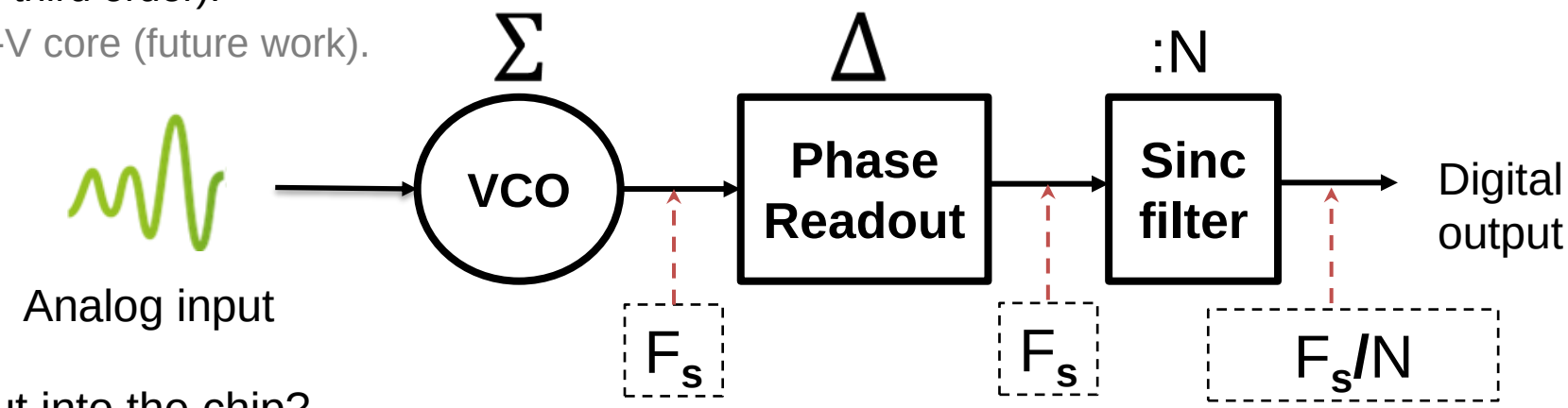






Proposal VCO-Base ADC 130nm for IoT

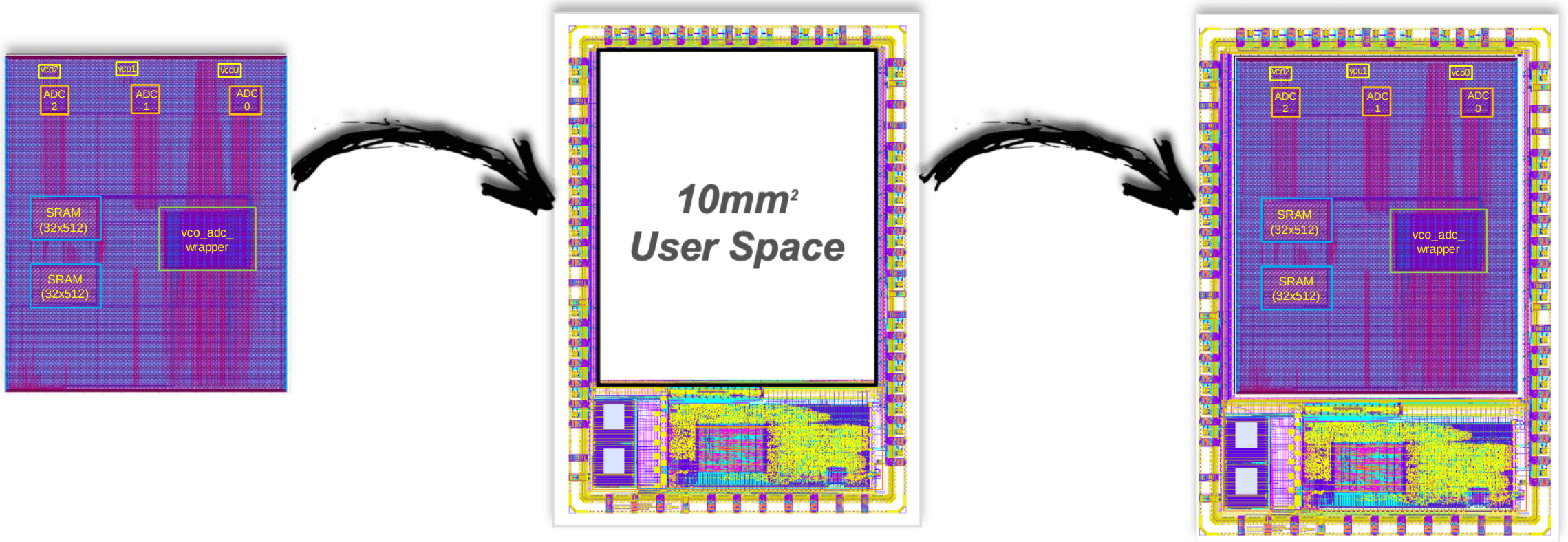
- Target <100 KHz bandwidth applications(Speech recording, sensor readout).
- Effective number of bit: 12 bit (speech recording)
- ADC specifications:
  - First order noise shaping Delta-Sigma ADC.
  - Clock oversampling: F_s = 24.576MHz,
  - Sampling rate default: 48KHz (OVS=512); configurable
  - Voltage Control Oscillator(VCO): From 2 to 10 MHz, 11 delay cell.
  - Phase readout 11 phases.
  - 32bit decimation filter(sinc third order).
  - Digital calibration by RISC-V core (future work).



- ❑ How to send the analog input into the chip?
- ❑ How to read out the results from the chip to do analysis (FFT in our case)?

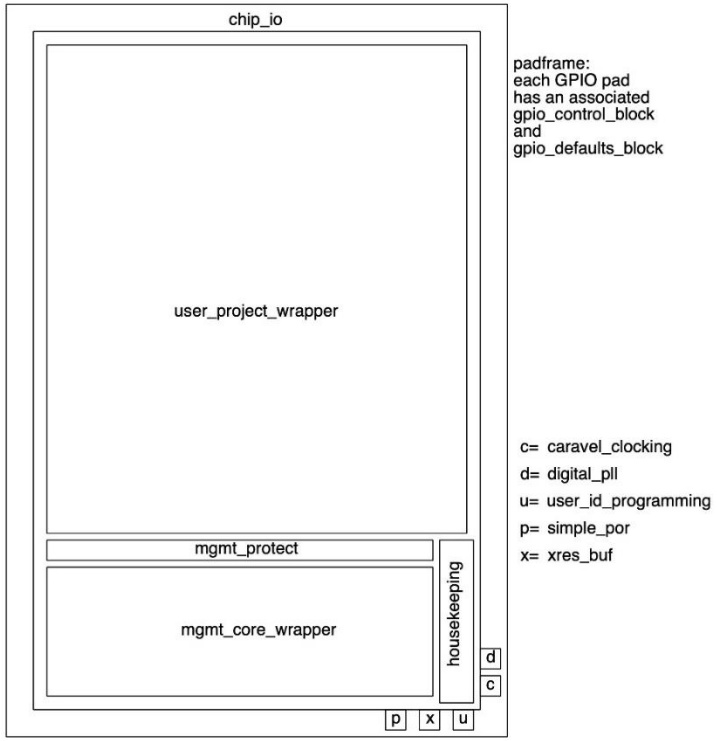
Caravel harness

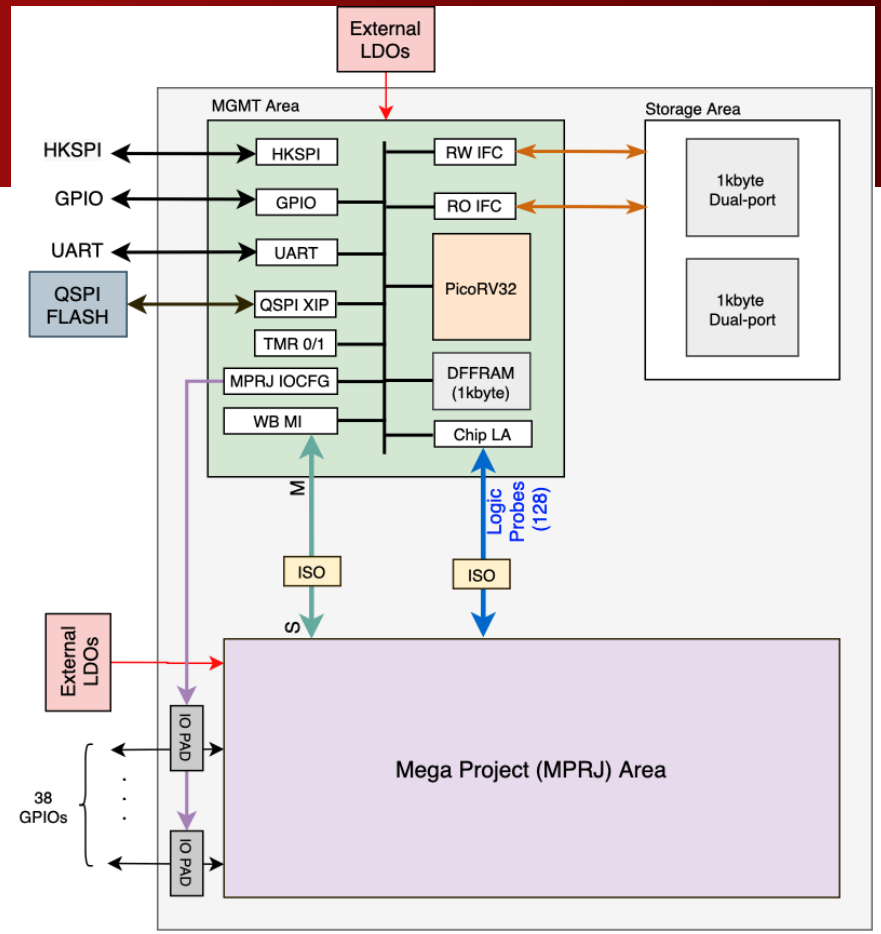
- Designers can focus on their designs
- Used in Open MPW & ChipIgnite program



Caravel SoC Harness

- Provided by caravel
  - Integrated RISC-V core
  - Wishbone bus interface
  - Simple Logic Analyzer
  - Simulation environment provided
  - Manual layout for Analog designers





Sending inputs/receiving outputs

- IO PADs:
- Logic Analyzer (LA)
- Wishbone Bus (WB)
  - Memory mapped

Writing a C Program to

- Config the IO Pads
- Read/write LA
- Read/write WB
- Read/write to UART on MGMT Area

Examples:

- io_ports (verilog/dv/io_ports)
- la_test1/la_test2 (verilog/dv/la_test1)
- wb_port (verilog/dv/wb_port)
- mprj_stimulus (verilog/dv/mprj_stimulus)

Ref: https://github.com/efabless/caravel_user_project

Run the examples

- Check out caravel_user_project

  $ git clone https://github.com/efabless/caravel_user_project
- Set things up

  $ cd caravel_user_project

  $ mkdir dependencies

  $ export PDK_ROOT=$PWD/dependencies/pdks

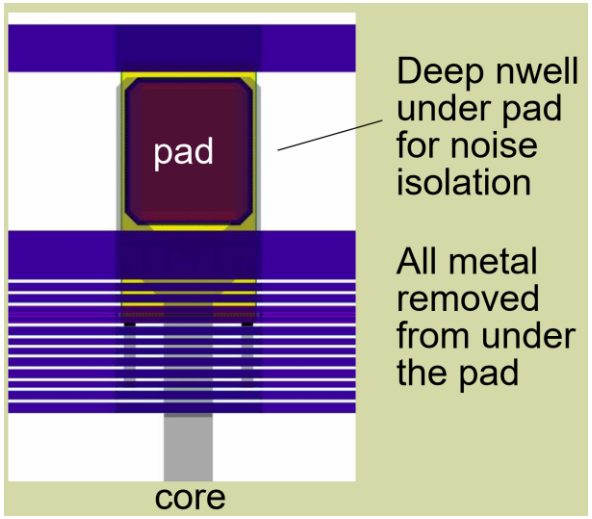
  $ export OPENLANE_ROOT=$PWD/dependencies/openlane

  $ make setup
- Run the RTL simulation
  - io_ports: make verify-io_ports-rtl
  - la_test1: make verify-la_test1-rtl
  - la_test2: make verify-la_test2-rtl
  - wb_port: make verify-wb_port-rtl
  - mprj_stimulus: make verify-mprj_stimulus-rtl
- Guide to integrate your own design
  - https://unic-cass.github.io/04-digital-design-flow.html

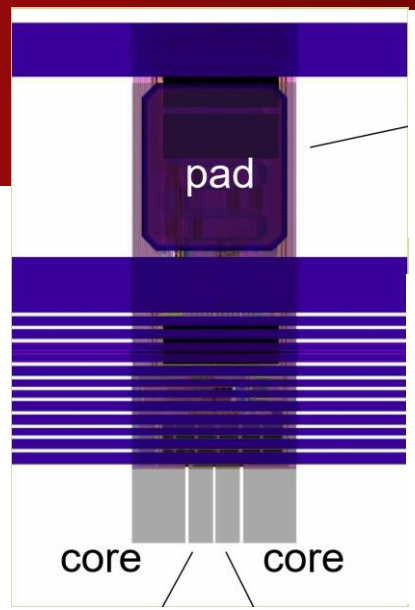
Ref: https://github.com/efabless/caravel_user_project/blob/main/docs/source/quickstart.rst

Caravel_user_project_analog

- Targeting Analog/mixed-signal projects
  - High speed
  - High voltage
  - Noise sensitive
- Main features
  - 11 GPIO pads as Analog I/O
  - 18 GPIOs have direct pad connection available to users
  - 3 pads include 5V ESD clamp connections
  - All Analog connection is ESD sensitive



Simple Analog PADs

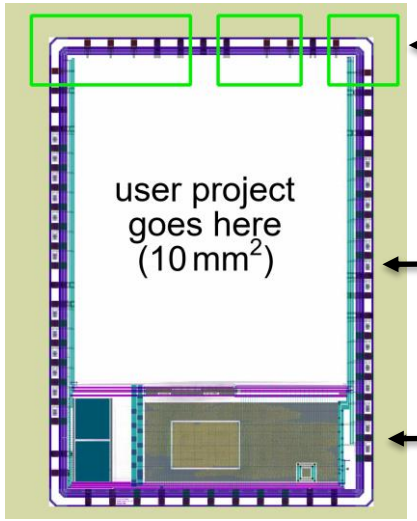


High voltage (3.3–5.5V) clamp under the pad, not connected.

Intended as a power pad, but can be used for any analog signal (but not GHz range)

Clamp high Clamp low

Undedicated power/ Analog PADs



These pads on the top have been repuposed for analog

Same GPIO for the rest

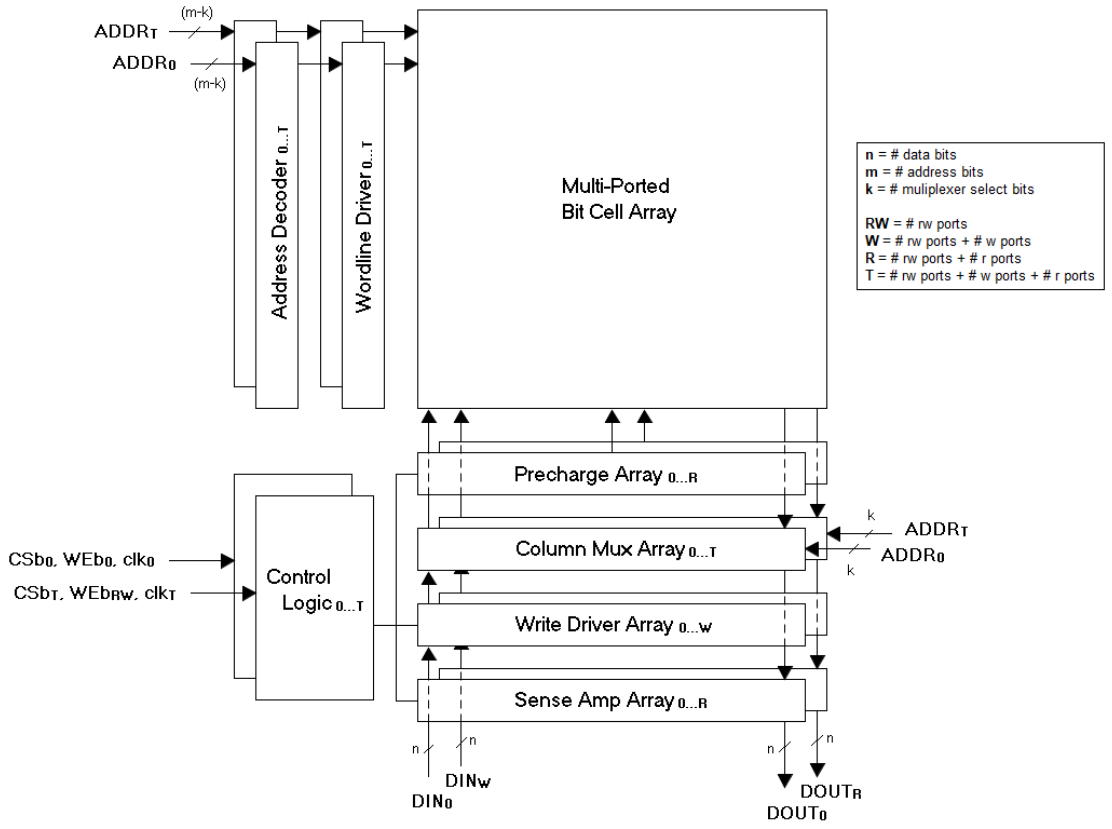
Same RISC-V management

Caravel testboard: https://github.com/efabless/caravel_board/tree/main
Caravel document: https://caravel-harness.readthedocs.io/en/latest/index.html
Ref: https://youtu.be/jBrBqhVNgDo?t=2048

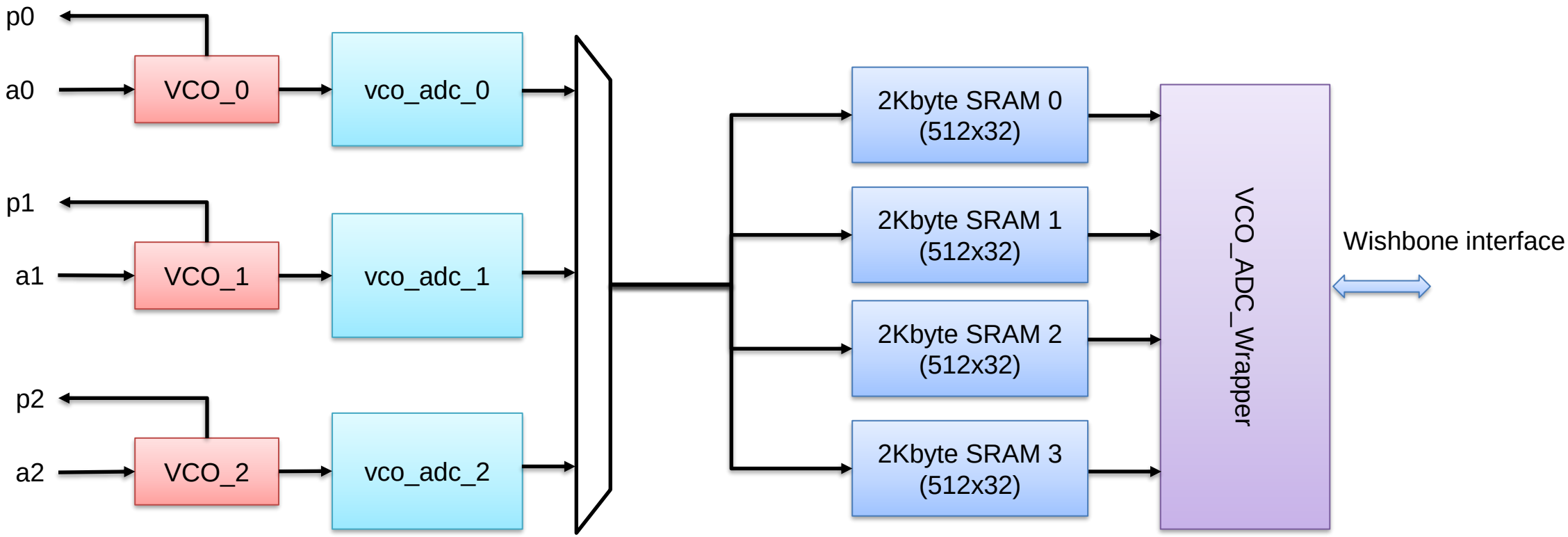
SRAM: OpenRAM from PDK

- Location: $PDK_ROOT/sky130A/libs.ref/sky130_sram_macros

```
├── gds
│   ├── sky130_sram_1kbyte_1rw1r_32x256_8.gds
│   ├── sky130_sram_1kbyte_1rw1r_8x1024_8.gds
│   ├── sky130_sram_2kbyte_1rw1r_32x512_8.gds
│   └── sram_1rw1r_32_256_8_sky130.gds
├── lef
│   ├── sky130_sram_1kbyte_1rw1r_32x256_8.lef
│   ├── sky130_sram_1kbyte_1rw1r_8x1024_8.lef
│   ├── sky130_sram_2kbyte_1rw1r_32x512_8.lef
│   └── sram_1rw1r_32_256_8_sky130.lef
├── lib
│   ├── sky130_sram_1kbyte_1rw1r_32x256_8_TT_1p8V_25C.lib
│   ├── sky130_sram_1kbyte_1rw1r_8x1024_8_TT_1p8V_25C.lib
│   ├── sky130_sram_2kbyte_1rw1r_32x512_8_TT_1p8V_25C.lib
│   ├── …
├── spice
└── verilog
    ├── sky130_sram_1kbyte_1rw1r_32x256_8.v
    ├── sky130_sram_1kbyte_1rw1r_8x1024_8.v
    ├── sky130_sram_2kbyte_1rw1r_32x512_8.v
    └── sram_1rw1r_32_256_8_sky130.v
```

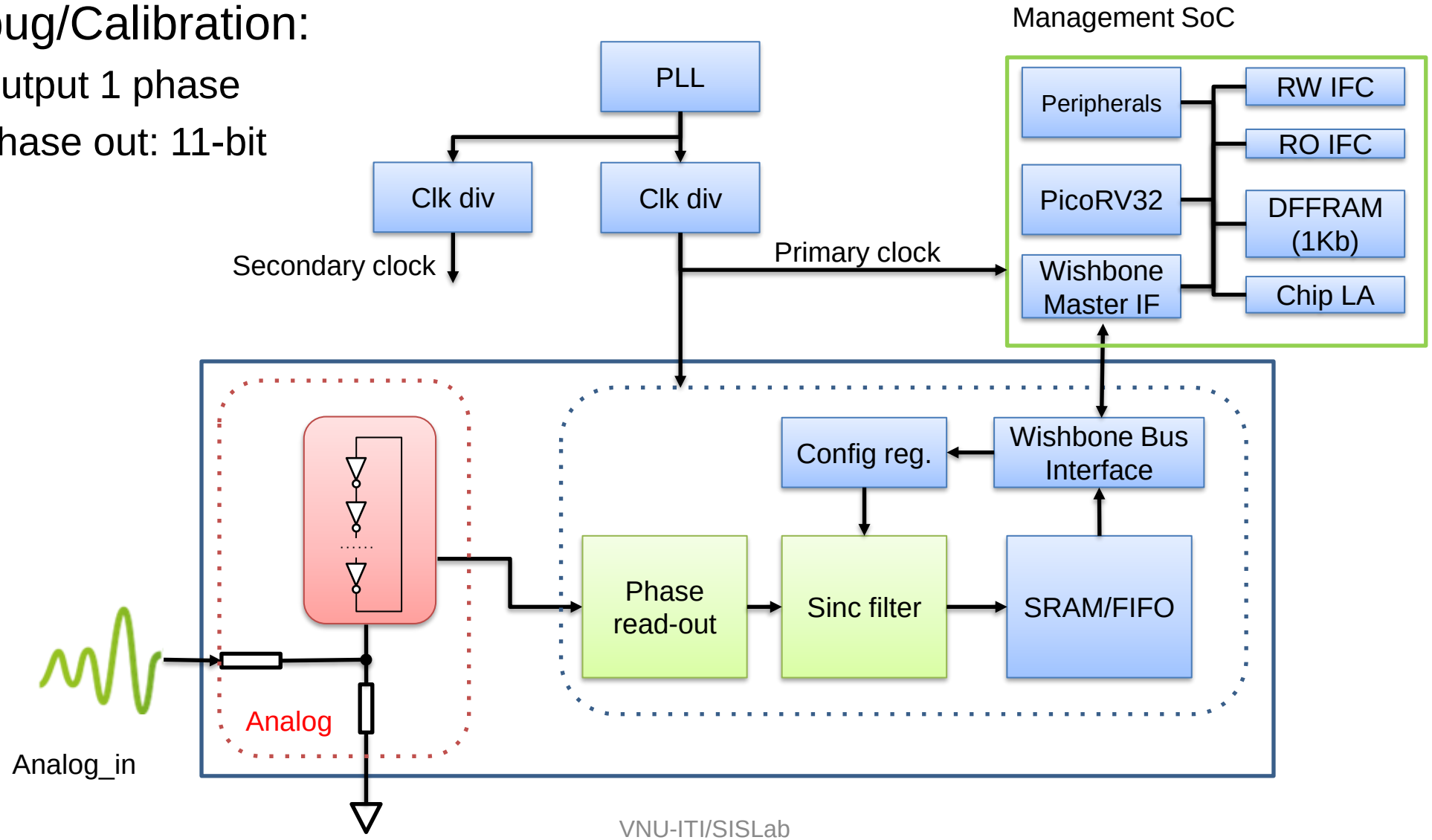


Chip architecture & test facilities



System Architecture

- Debug/Calibration:
  - Output 1 phase
  - Phase out: 11-bit



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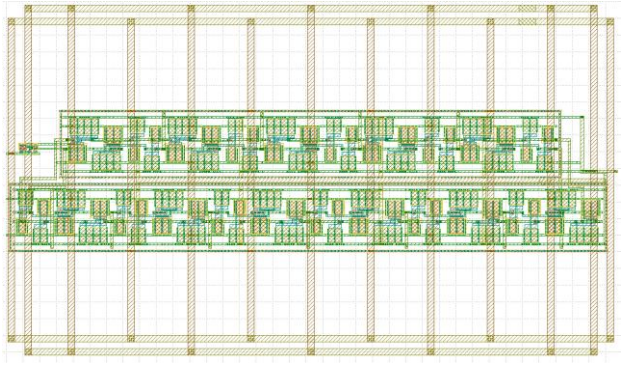
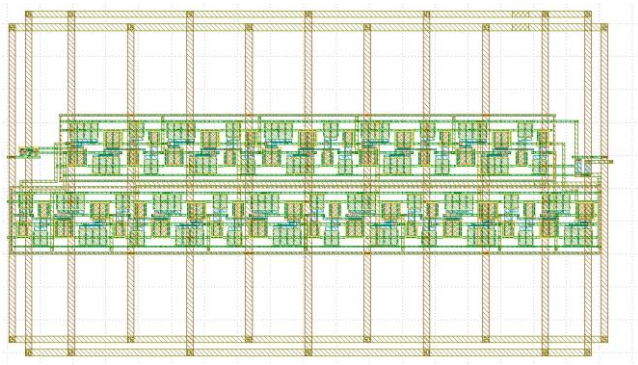
VCO modules

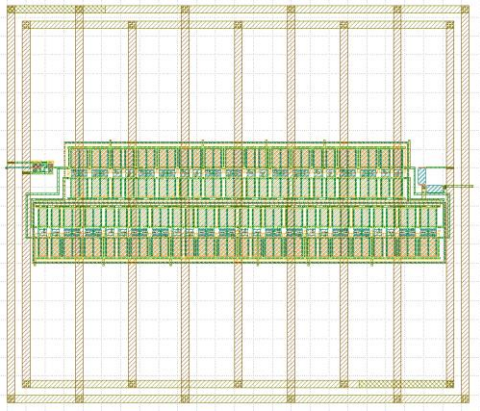
- VCO: VCO without resistors
- VCO_r100: VCO with two integrated resistor (100ohm each)
- VCO_w6_r100: more compact ring oscillator
  - Current design failed with tritonRoute in Openlane => not integrated
  - Solutions: pin must be aligned to the track for routing



VCO (183x108 um2)



VCO_r100 (183x108 um2)



VCO_w6_r100
(122x106 um2)

Openlane config: vco_adc

```
{
    "DESIGN_NAME": "vco_adc",
    "DESIGN_IS_CORE": 0,
    "VERILOG_FILES": [
        "dir::../../verilog/rtl/defines.v",

"dir::../../verilog/rtl/phase_readout.v",
        "dir::../../verilog/rtl/phase_diff.v",
        "dir::../../verilog/rtl/phase_sum.v",
        "dir::../../verilog/rtl/sinc_sync.v",
        "dir::../../verilog/rtl/vco_adc.v"
    ],
    "CLOCK_PERIOD": 25,
    "CLOCK_PORT": "clk",
    "CLOCK_NET": "ref::$CLOCK_PORT",
    "FP_SIZING": "absolute",
    "DIE_AREA": "0 0 340 340",
    "FP_PIN_ORDER_CFG": "dir::pin_order.cfg",
    "MAX_TRANSITION_CONSTRAINT": 1.0,
    "MAX_FANOUT_CONSTRAINT": 16,
    "PL_TARGET_DENSITY": 0.4,
    "PL_RESIZER_SETUP_SLACK_MARGIN": 0.4,
    "GLB_RESIZER_SETUP_SLACK_MARGIN": 0.2,
    "GLB_RESIZER_HOLD_SLACK_MARGIN": 0.2,
    "PL_RESIZER_HOLD_SLACK_MARGIN": 0.4,
    "MAGIC_DEF_LABELS": 0,
    "SYNTH_BUFFERING": 0,
    "RUN_HEURISTIC_DIODE_INSERTION": 1,
    "HEURISTIC_ANTENNA_THRESHOLD": 110,
    "GRT_REPAIR_ANTENNAS": 1,
    "VDD_NETS": [
        "vccd1"
    ],
    "GND_NETS": [
        "vssd1"
    ],
    "IO_SYNC": 0,
    "BASE_SDC_FILE": "dir::base.sdc",
    "RUN_CVC": 1,
```

```
  "pdk::sky130*": {
        "FP_CORE_UTIL": 45,
        "RT_MAX_LAYER": "met4",
        "scl::sky130_fd_sc_hd": {
            "CLOCK_PERIOD": 25
        },
        "scl::sky130_fd_sc_hdll": {
            "CLOCK_PERIOD": 10
        },
        "scl::sky130_fd_sc_hs": {
            "CLOCK_PERIOD": 8
        },
        "scl::sky130_fd_sc_ls": {
            "CLOCK_PERIOD": 10,
            "SYNTH_MAX_FANOUT": 5
        },
        "scl::sky130_fd_sc_ms": {
            "CLOCK_PERIOD": 10
        }
    },
    "pdk::gf180mcuC": {
        "STD_CELL_LIBRARY": "gf180mcu_fd_sc_mcu7t5v0",
        "CLOCK_PERIOD": 24.0,
        "FP_CORE_UTIL": 40,
        "RT_MAX_LAYER": "Metal4",
        "SYNTH_MAX_FANOUT": 4,
        "PL_TARGET_DENSITY": 0.45
    }
}
```

vco_adc config.json

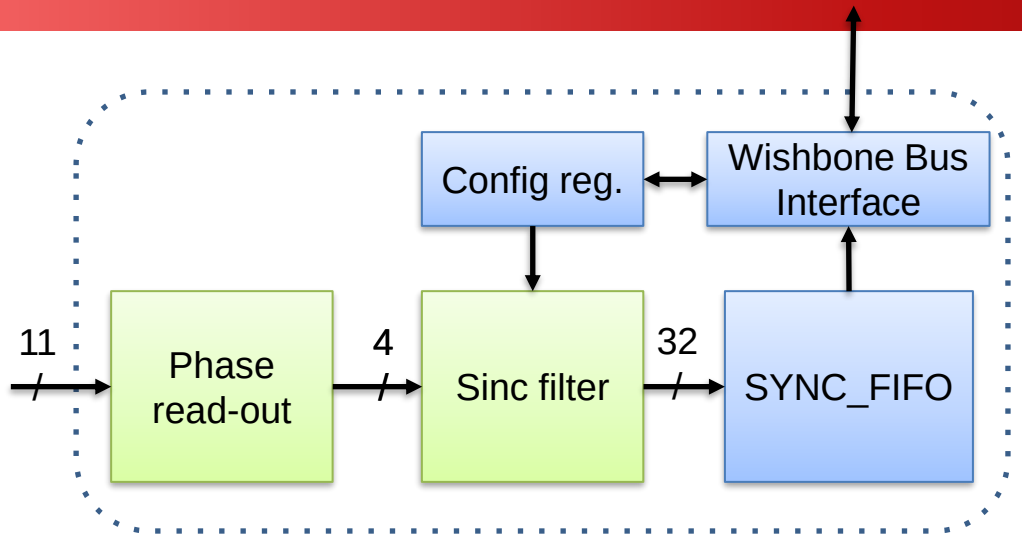
```
#BUS_SORT
#N
phase_.*
#W
clk
rst
enable_.*
oversample_.*
#S
data_.*
```

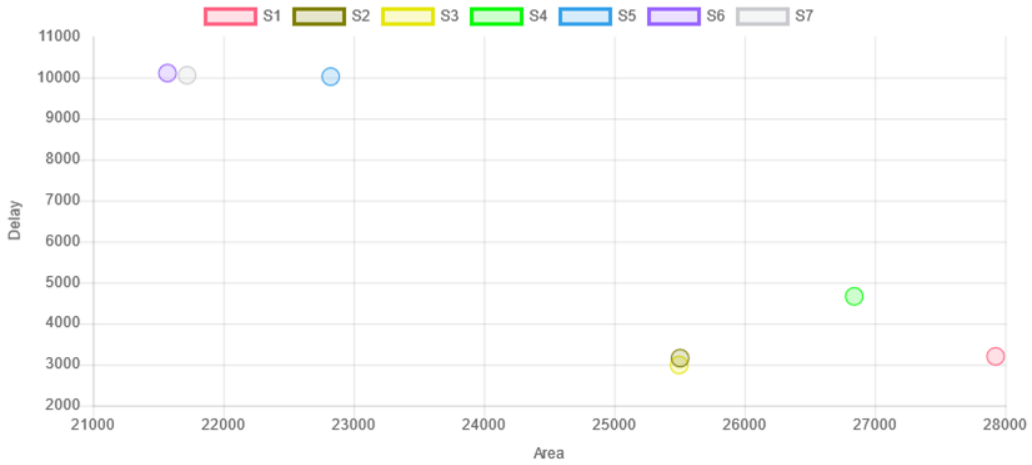
pin_order.cfg

```
set ::env(CLOCK_PERIOD) 10
set ::env(CLOCK_PORT) "clk"
set ::env(IO_PCT) 0.2
set ::env(SYNTH_DRIVING_CELL) "sky130_fd_sc_hd__inv_1"
set ::env(SYNTH_DRIVING_CELL_PIN) "Y"
set ::env(SYNTH_CAP_LOAD) "33.5"
set ::env(SYNTH_MAX_FANOUT) "4"

create_clock [get_ports $::env(CLOCK_PORT)]  -name $::env(CLOCK_PORT)  -period
$::env(CLOCK_PERIOD)
set_propagated_clock [get_clocks $::env(CLOCK_PORT)]

set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
puts "\[INFO\]: Setting input delay to: $input_delay_value"

set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]

set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
```

base.sdc

Synthesis exploration results





Startegy	Gate Count	Area (um^2)	Delay (ps)	Gates Ratio	Area Ratio	Delay Ratio
S1: -p	3164	27926.78	3198.34	1.156	1.294	1.07
S2: -p	3367	25505.71	3154.68	1.231	1.182	1.055
S3: -p	3360	25498.21	2987.84	1.228	1.182	1
S4: -p	3024	26841.99	4662.29	1.105	1.244	1.56
S5: -p	3013	22824.39	10022.18	1.101	1.058	3.354
S6: -p	2756	21571.94	10108.28	1.007	1	3.383
S7: -p	2735	21722.08	10055.86	1	1.006	3.365

Openlane config: user_project_wrapper

```
{
    "DESIGN_NAME": "user_project_wrapper",
    "VERILOG_FILES": [
        "dir::../../verilog/rtl/defines.v",
        "dir::../../verilog/rtl/user_project_wrapper.v"
    ],
    "ROUTING_CORES": 1,
    "CLOCK_PERIOD": 25,
    "CLOCK_PORT": "wb_clk_i",
    "CLOCK_NET": "ref::$CLOCK_PORT",
    "FP_PDN_MACRO_HOOKS": [
        "vco_adc_wrapper_1 vccd1 vssd1 vccd1 vssd1,",
        "vco_adc_0 vccd1 vssd1 vccd1 vssd1,",
        "vco_adc_1 vccd1 vssd1 vccd1 vssd1,",
        "vco_adc_2 vccd1 vssd1 vccd1 vssd1,",
        "vco_0 vccd1 vssd1 vccd1 vssd1,",
        "vco_1 vccd1 vssd1 vccd1 vssd1,",
        "vco_2 vccd1 vssd1 vccd1 vssd1,",
        "mem_0 vccd1 vssd1 vccd1 vssd1,",
        "mem_1 vccd1 vssd1 vccd1 vssd1,",
        "mem_2 vccd1 vssd1 vccd1 vssd1,",
        "mem_3 vccd1 vssd1 vccd1 vssd1"],
    "MACRO_PLACEMENT_CFG": "dir::macro.cfg",
    "MAGIC_DEF_LABELS": 0,
    "MAGIC_EXT_USE_GDS": 0,
    "VERILOG_FILES_BLACKBOX": [
        "dir::../../verilog/gl/vco_adc.v",
        "dir::../../verilog/gl/vco_adc_wrapper.v",
        "dir::../../verilog/rtl/vco.v",
        "dir::../../verilog/rtl/vco_w6_r100.v",
        "dir::../../verilog/rtl/vco_r100.v",
"ref::$PDKPATH/libs.ref/sky130_sram_macros/verilog/
sky130_sram_2kbyte_1rw1r_32x512_8.v"],
    "EXTRA_LEFS": ["dir::../../lef/vco_adc.lef",
                   "dir::../../lef/vco_adc_wrapper.lef",
                   "dir::../../lef/vco.lef",
                   "dir::../../lef/vco_w6_r100.lef",
                   "dir::../../lef/vco_r100.lef",
                  "ref::$PDKPATH/libs.ref/sky130_sr
am_macros/lef/sky130_sram_2kbyte_1rw1r_32x512_8.
lef"],
```

```
    "EXTRA_GDS_FILES": ["dir::../../gds/vco_adc.gds",
                        "dir::../../gds/vco_adc_wrapper.gds"
                        "dir::../../gds/vco.gds",
                        "dir::../../gds/vco_r100.gds",
                        "dir::../../gds/vco_w6_r100.gds",
                        "ref::$PDKPATH/libs.ref/sky130_sram_ma
cros/gds/sky130_sram_2kbyte_1rw1r_32x512_8.gds" ],
    "EXTRA_LIBS": ["dir::../../lib/vco_adc.lib",
                   "dir::../../lib/vco_adc_wrapper.lib",
"ref::$PDKPATH/libs.ref/sky130_sram_macros/lib/sky130_sra
m_2kbyte_1rw1r_32x512_8_TT_1p8V_25C.lib"],
    "EXTRA_SPEFS": [
        "vco_adc",
        "dir::../../spef/multicorner/vco_adc.min.spef",
        "dir::../../spef/multicorner/vco_adc.nom.spef",
        "dir::../../spef/multicorner/vco_adc.max.spef",
        "vco_adc_wrapper",
        "dir::../../spef/multicorner/vco_adc_wrapper.min.spef",
        "dir::../../spef/multicorner/vco_adc_wrapper.nom.spef",
        "dir::../../spef/multicorner/vco_adc_wrapper.max.spef"
    ],
    "SYNTH_READ_BLACKBOX_LIB": 1,
    "BASE_SDC_FILE": "dir::base_user_project_wrapper.sdc",
    "IO_SYNC": 0,
    "MAX_TRANSITION_CONSTRAINT": 1.5,
    "RUN_LINTER": 0,
    "QUIT_ON_SYNTH_CHECKS": 0,
    "FP_PDN_CHECK_NODES": 0,
    "SYNTH_ELABORATE_ONLY": 1,
    "PL_RANDOM_GLB_PLACEMENT": 1,
    "PL_RESIZER_DESIGN_OPTIMIZATIONS": 0,
    "PL_RESIZER_TIMING_OPTIMIZATIONS": 0,
    "GLB_RESIZER_DESIGN_OPTIMIZATIONS": 0,
    "GLB_RESIZER_TIMING_OPTIMIZATIONS": 0,
    "PL_RESIZER_BUFFER_INPUT_PORTS": 0,
    "FP_PDN_ENABLE_RAILS": 0,
    "GRT_REPAIR_ANTENNAS": 0,
    "RUN_FILL_INSERTION": 0,
    "RUN_TAP_DECAP_INSERTION": 0,
    "FP_PDN_VPITCH": 180,
    "FP_PDN_HPITCH": 180,
    "RUN_CTS": 0,
    "FP_PDN_VOFFSET": 5,
    "FP_PDN_HOFFSET": 5,
```

```
"MAGIC_ZEROIZE_ORIGIN": 0,
    "FP_SIZING": "absolute",
    "RUN_CVC": 0,
    "UNIT": 2.4,
    "FP_IO_VEXTEND": "expr::2 * $UNIT",
    "FP_IO_HEXTEND": "expr::2 * $UNIT",
    "FP_IO_VLENGTH": "expr::$UNIT",
    "FP_IO_HLENGTH": "expr::$UNIT",
    "FP_IO_VTHICKNESS_MULT": 4,
    "FP_IO_HTHICKNESS_MULT": 4,
    "FP_PDN_CORE_RING": 1,
    "FP_PDN_CORE_RING_VWIDTH": 3.1,
    "FP_PDN_CORE_RING_HWIDTH": 3.1,
    "FP_PDN_CORE_RING_VOFFSET": 12.45,
    "FP_PDN_CORE_RING_HOFFSET": 12.45,
    "FP_PDN_CORE_RING_VSPACING": 1.7,
    "FP_PDN_CORE_RING_HSPACING": 1.7,
    "FP_PDN_VWIDTH": 3.1,
    "FP_PDN_HWIDTH": 3.1,
    "FP_PDN_VSPACING": "expr::(5 * $FP_PDN_CORE_RING_VWIDTH)",
    "FP_PDN_HSPACING": "expr::(5 * $FP_PDN_CORE_RING_HWIDTH)",
    "VDD_NETS": [
        "vccd1",
        "vccd2",
        "vdda1",
        "vdda2"
    ],
    "GND_NETS": [
        "vssd1",
        "vssd2",
        "vssa1",
        "vssa2"
    ],
    "SYNTH_USE_PG_PINS_DEFINES": "USE_POWER_PINS",
    "pdk::sky130*": {
        "RT_MAX_LAYER": "met4",
        "DIE_AREA": "0 0 2920 3520",
        "FP_DEF_TEMPLATE":
"dir::fixed_dont_change/user_project_wrapper.def",
        "PL_OPENPHYSYN_OPTIMIZATIONS": 0,
....
```

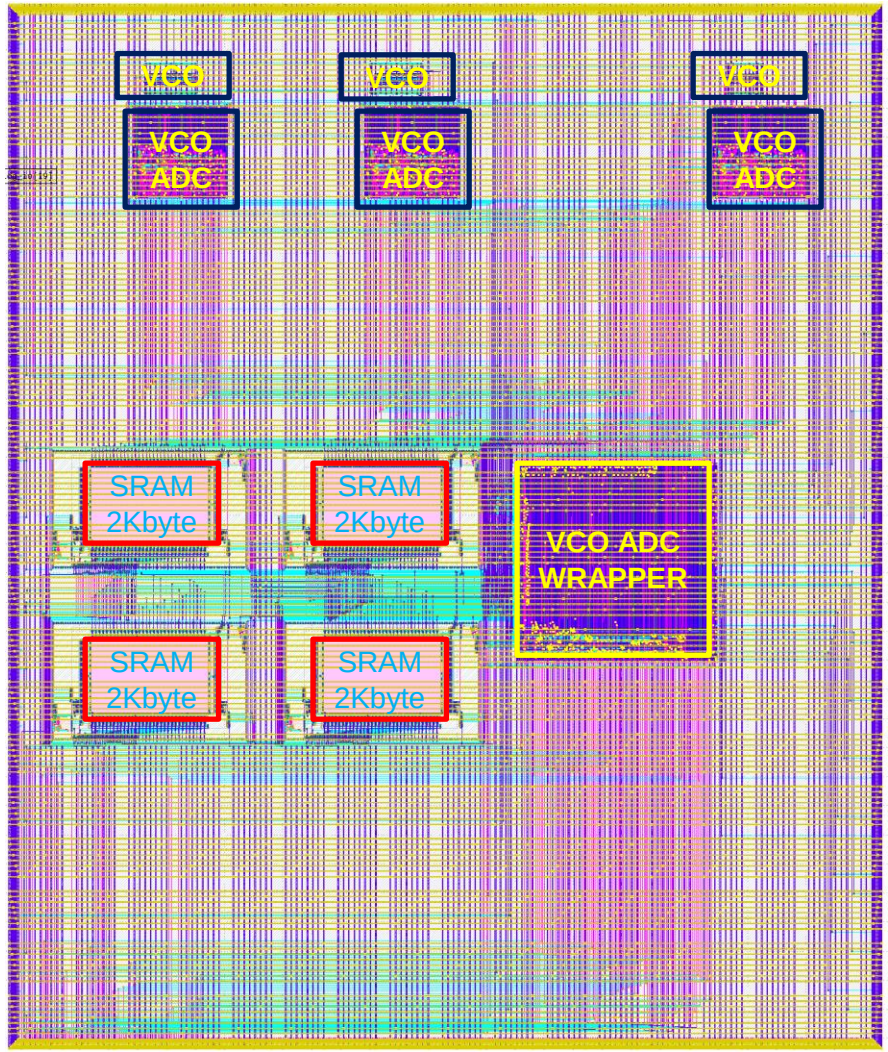
```
vco_adc_wrapper_1 1700 1290 N
vco_2 424.2 3248.0 N
vco_adc_2 376.46 2879.1 N
vco_1 1200.4 3248.0 N
vco_adc_1 1176.0 2879.1 N
vco_0 2431.19915 3248.0 N
vco_adc_0 2373.74 2879.1 N
mem_1 100 1612 N
mem_3 900 1612 N
mem_0 100 1020 N
mem_2 900 1020 N
```

macro.cfg

openlane/user_project_wrapper/config.json

User Project Wrapper

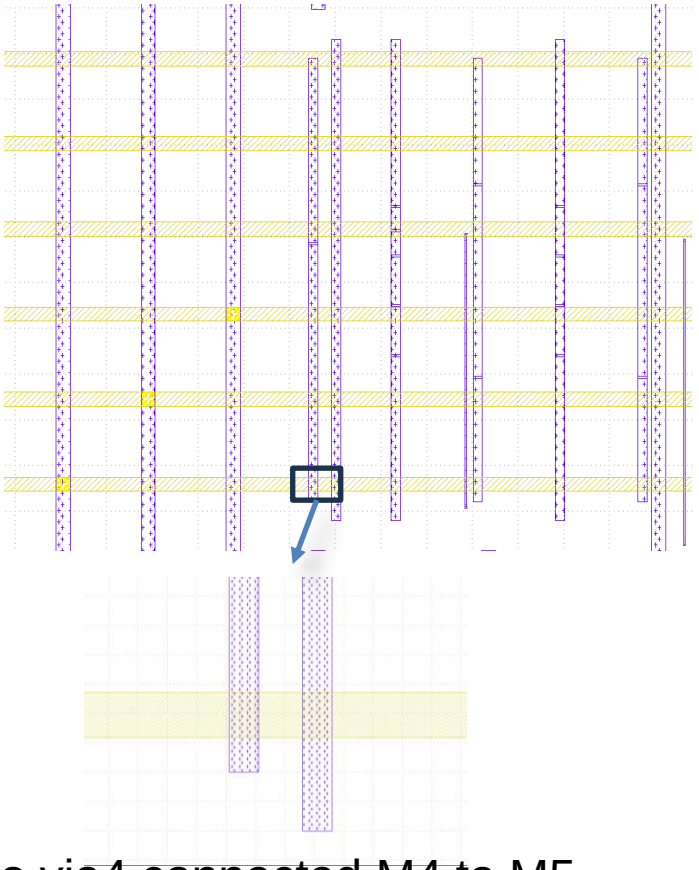
- Customed designs:
  - vco2: vco_r100
  - vco1: vco
  - vco0: vco_w6_r100
- Digital designs:
  - VCO-ADCs
  - vco_adc_wrapper
- Customed cells:
  - SRAM32x512 from OpenRAM



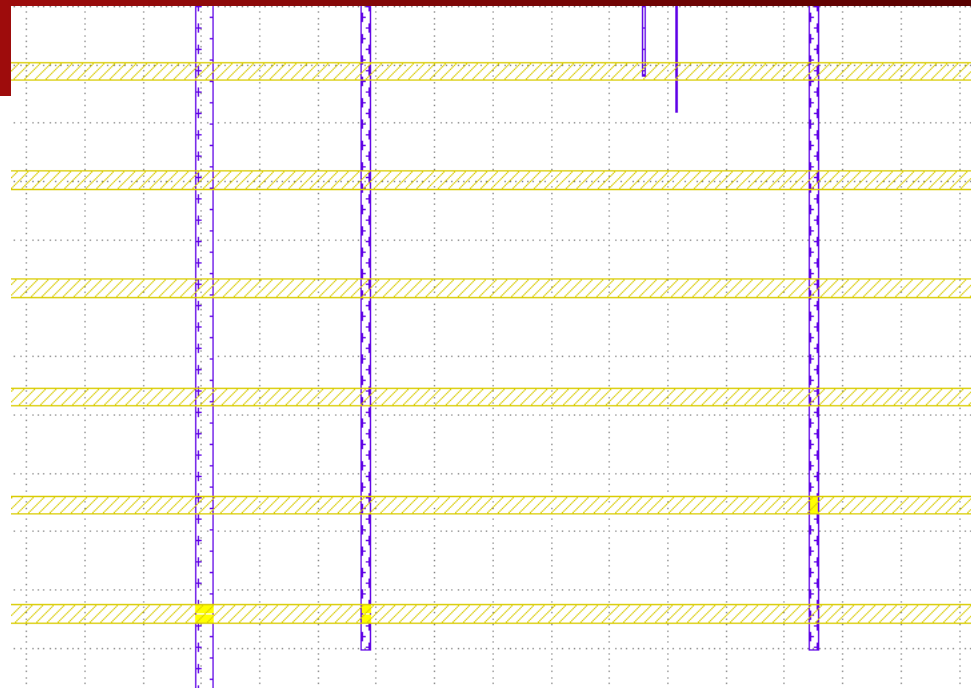
New version with 8Kbyte SRAM

Debug the layout

- Using Klayout/Magic
  - Import def/lef
  - View the GDS
  - Debug DRC
  - Debug LVS
- Common LVS errors:
  - power/ground is not connected



No via4 connected M4 to M5



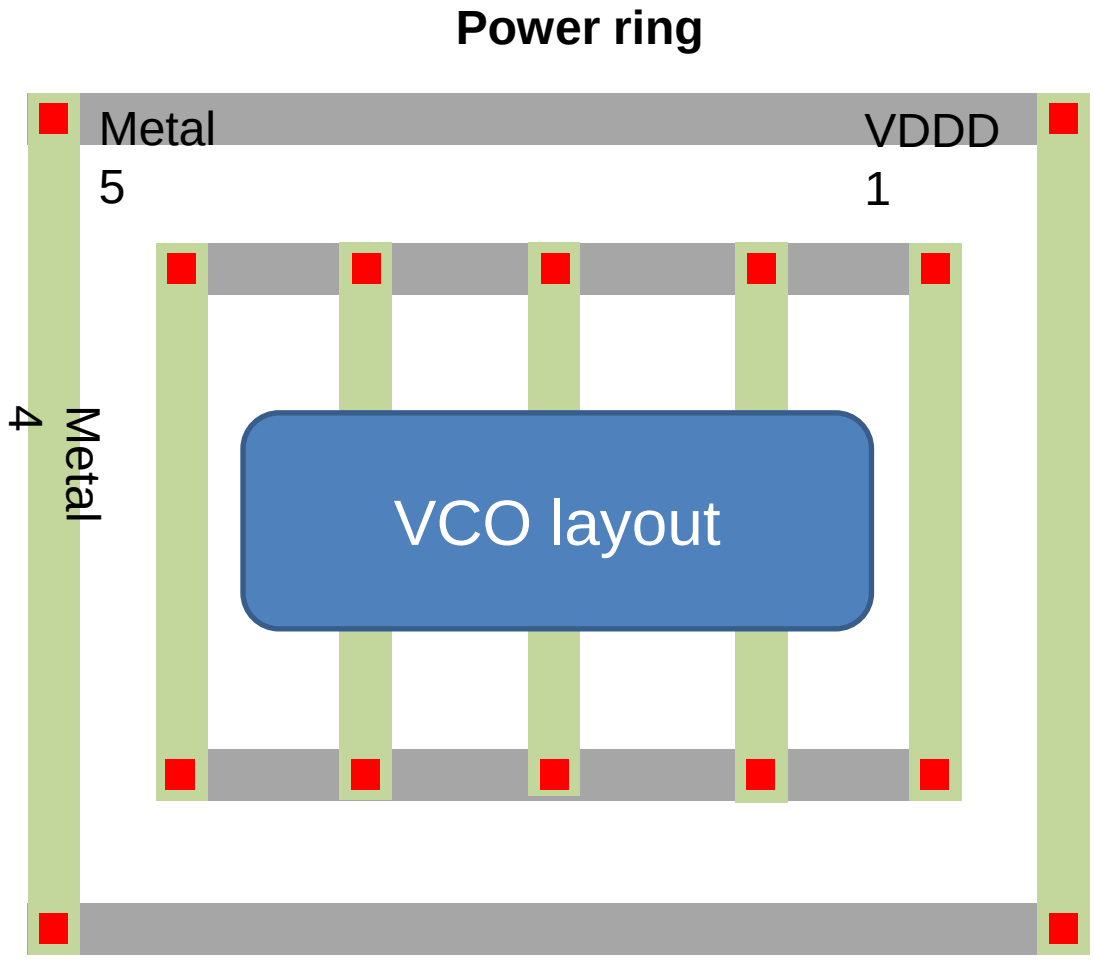
via4 connected M4 to M5

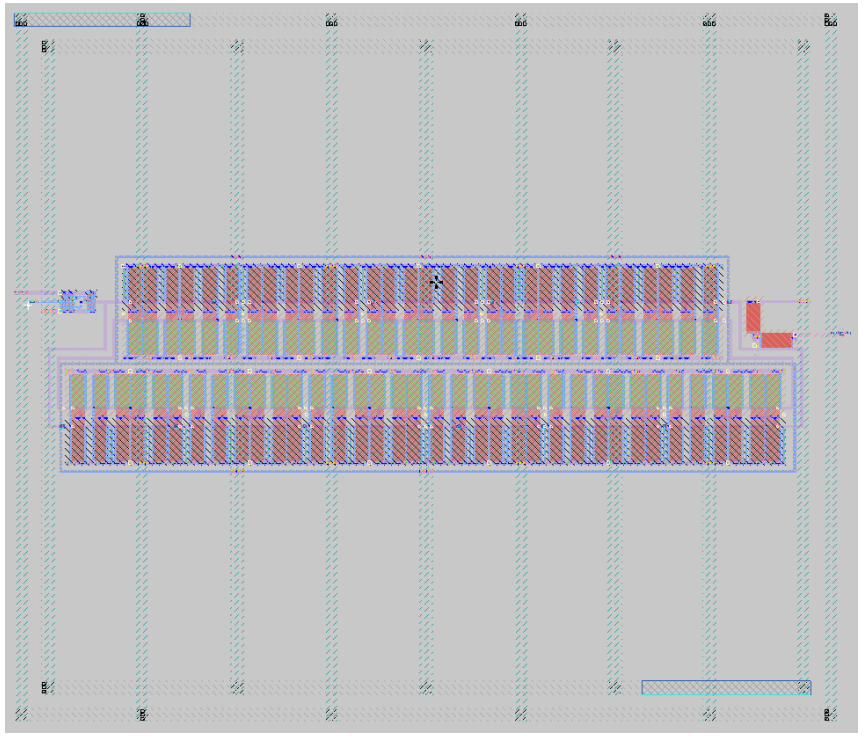
Outline

- Design with Caravel Harness
  - caravel_user_project
  - caravel_user_project_analog
  - SRAM macro
- Mixed-signal design implementation using the digital flows
  - Module implementation
  - Top-level integration
  - DRC/LVS debugging
- Some layout techniques to use the digital router
  - Layout analog blocks for the digital flow
  - Exporting GDS and abstract view (LEF)

Macro layout in Magic

VCO layout is small => need to extend the power straps to connect to the power net in user_project_wrapper





Pin guideline (grid)

File tracks.info file: library_name/tracks.info
Example:
$PDK_ROOT/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tracks.info

layer	offset	space
li1	X 0.23	0.46
li1	Y 0.17	0.34
met1	X 0.17	0.34
met1	Y 0.17	0.34
met2	X 0.23	0.46
met2	Y 0.23	0.46
met3	X 0.34	0.68
met3	Y 0.34	0.68
met4	X 0.46	0.92
met4	Y 0.46	0.92
met5	X 1.70	3.40
met5	Y 1.70	3.40

recommended direction

li1: Both
met1: Horizontal
met2: Vetical
met3: Horizontal
met4: Vetical
met5: Horizontal

Displaying grid in command:

Syntax:

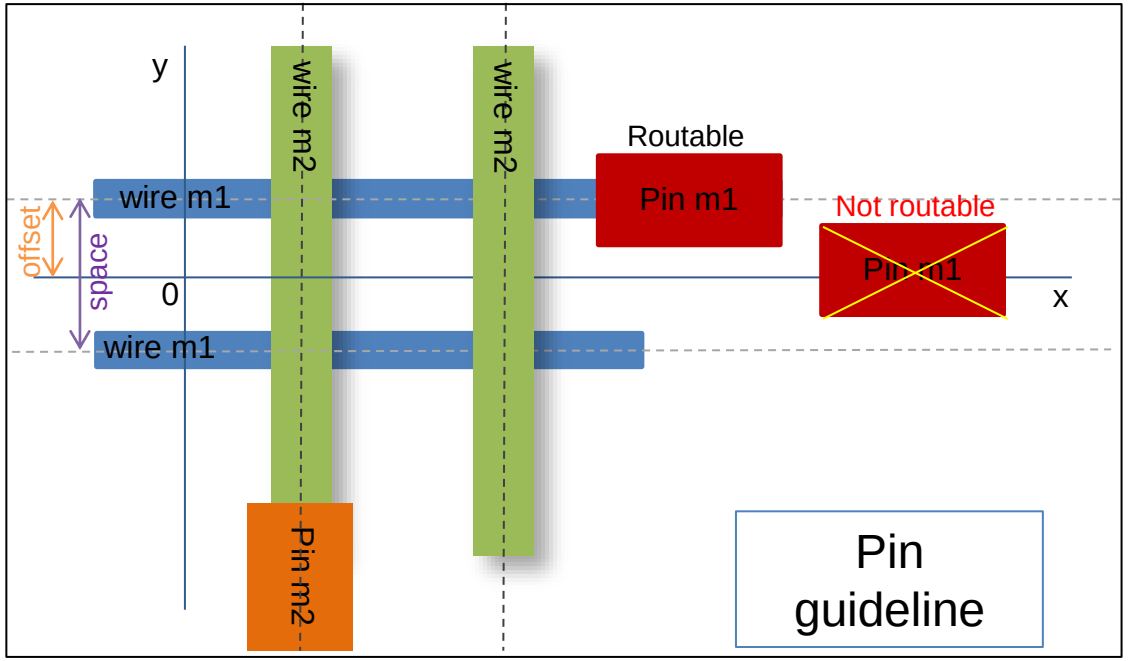
grid X_{space} y_{space} X_{offset} Y_{offset}

Example for only metal1

grid 0.34um 0.34um 0.17um 0.17um

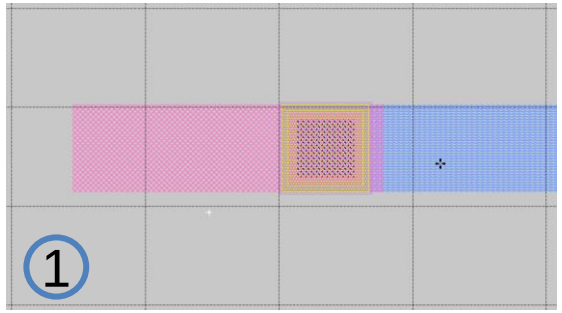
Example for metal1 and metal 2

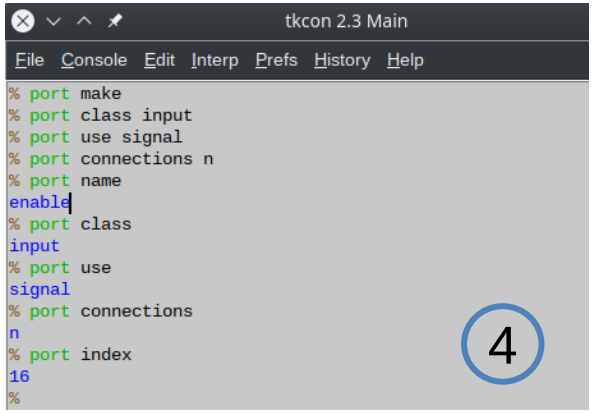
grid 0.46um 0.34um 0.23um 0.17um

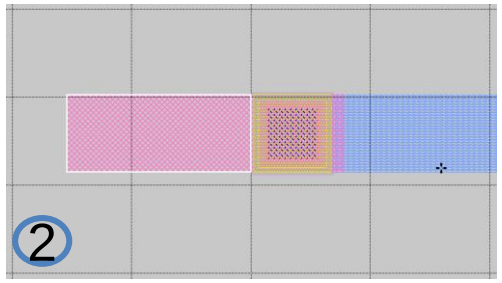


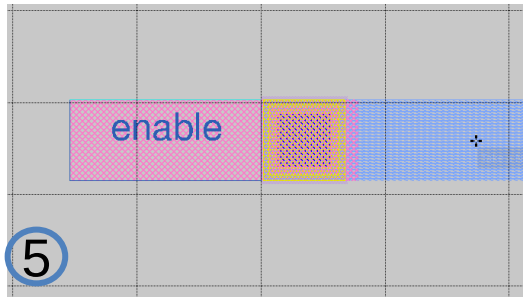
Ref: https://gitlab.com/gab13c/openlane-workshop#day-4-layout-timing-analysis-and-cts

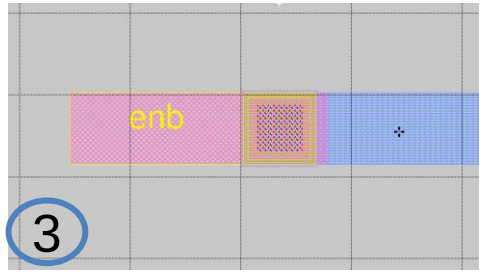
Pin guideline (label and port) in Magic

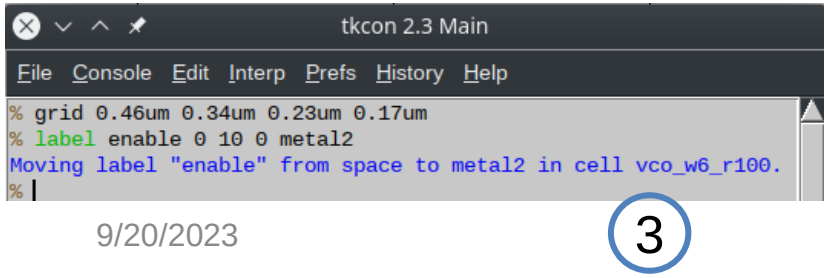












1. Create a pin that is route-able:
2. Select rectangular pin:
3. Label pin:

Syntax:

label <name> <font> <size> <direction> <layer>

Example : fig (3)

label enable 0 10 0 metal2

4. Init and verify port properties:

Syntax:

port make

port class <input, output bidirectional>

port use <signal, power, ground>

port connections <n w s e> (connection dir)

Example: fig (4)

5. Verifying:

- Pin color is blue
- File .mag has port define

Export GDS and LEF file for Openlane

Extract .gds file:

Syntax: gds write <design_name>.gds

example: gds write vco_w6_r100.gds

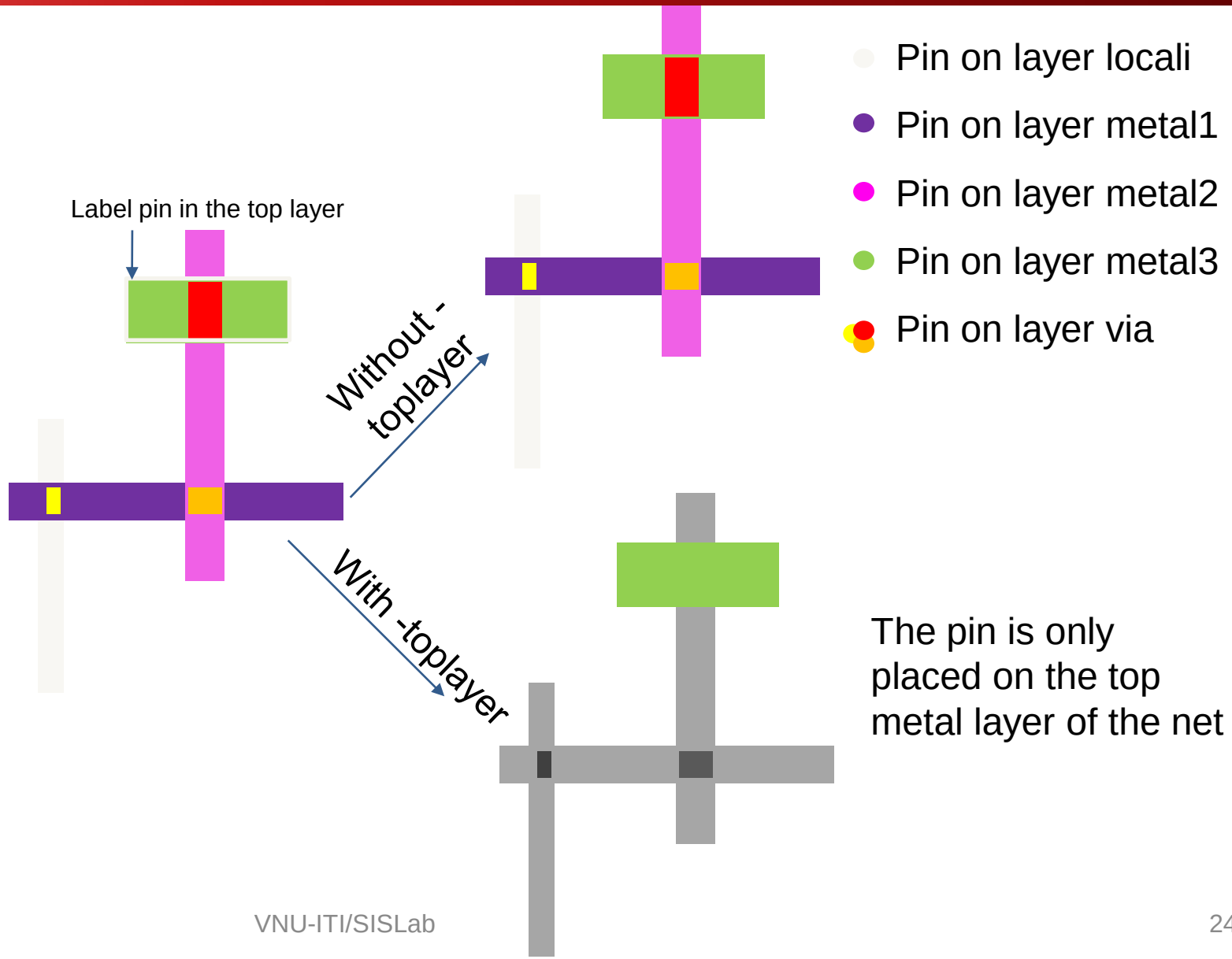
For more help: gds help

Extract .lef file:

Syntax: lef write <design_name>.lef

example: lef write vco_w6_r100.lef

For more help: lef help



Notice:

lef writeall -toplayer:

- Pins are placed on toplayer
- Easy to handle routing
- Hard to design io pin
- Example 1: with/without option -toplayer

The pin is only placed on the top metal layer of the net

Thank you for your attention!

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