UNIC-CASS Program

Design to Tapeout Mentoring
Mentoring Session # 5

Progress Questionnaire
Responses by Design Teams

Compiled on Sept 19, 2023
by

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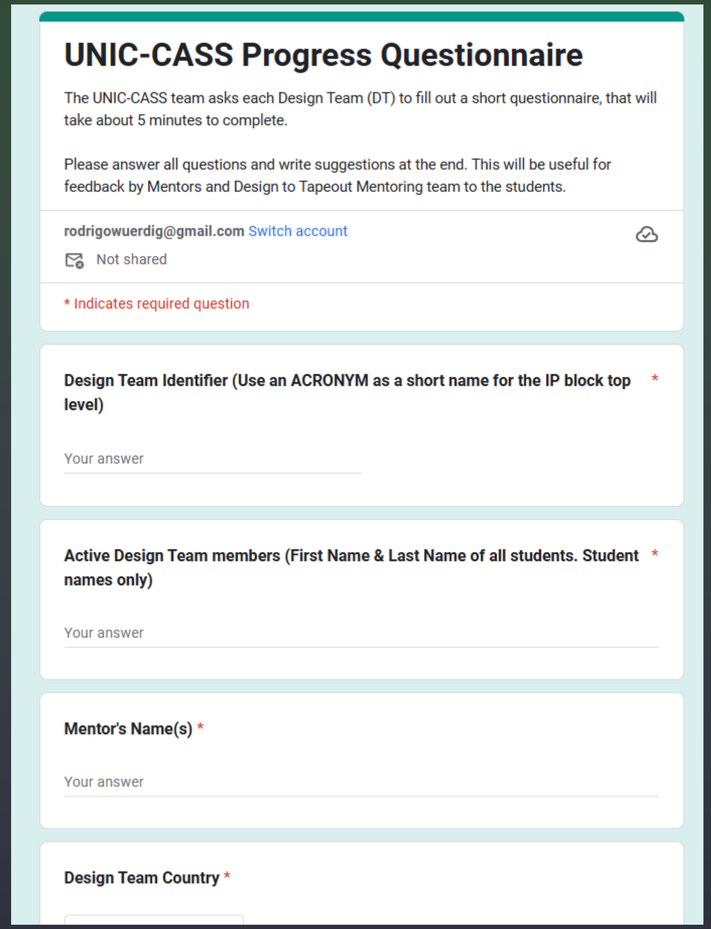
All Design Teams respond **ASAP**

RESPOND to this Google Form:

“UNIC-CASS Progress Questionnaire “

Enter ONE response per Design Team (DT)

https://forms.gle/jvCkMkUF9HNuegEA9



UNIC-CASS Progress Questionnaire

The UNIC-CASS team asks each Design Team (DT) to fill out a short questionnaire, that will take about 5 minutes to complete.

Please answer all questions and write suggestions at the end. This will be useful for feedback by Mentors and Design to Tapeout Mentoring team to the students.

rodrigowuerdig@gmail.com Switch account

Not shared

* Indicates required question

Design Team Identifier (Use an ACRONYM as a short name for the IP block top level) *

Your answer

Active Design Team members (First Name & Last Name of all students. Student names only) *

Your answer

Mentor's Name(s) *

Your answer

Design Team Country *

Respond in Google Forms (1 per DT)
https://forms.gle/jvCkMkUF9HNuegEA9

Part I :

- Design Team Identifier (provide an ACRONYM of your IP Block . Example: ALU32b)
- DT Student Members (list all active STUDENTS in the DT)
- Mentor´s Name
- Design Team Country

Is your Design ?

- Digital only
- Mixed Signal

Respond in Google Forms (1 per DT)

Part II : **for DIGITAL-only designs**

- Do you have your RTL completed already ?
- Have you completed the Logic Synthesis and the Place-and-Route steps?
- Provide an estimate of area (estimated so far – it may change later)
- Provide an estimate of total I/O pins of your block (do not count VDD and GND pads)
- Write two sentences about the status of your Design and the DT familiarity with the Digital Open-source EDA flow
- Write two sentences about difficulties, if any, the DT encountered with the Open-Source tools and Skywater PDK usage.

Respond in Google Forms (1 per DT)

Part II : **for Mixed-signal Analog-Digital designs**

- Is the circuit schematic for your design already completed in Xschem?
- Provide na estimate of toal I/O pins : (X digital pins, Y analog pins)
- Have you completed the layout of what percentage of your full-custom Design?
- For the digital blocks, if needed, are they completed in RTL (like Verilog or VHDL)?
- What part or blocks of your full custom design are already laid-out and DRC&LVS verified with Magic and Netgen tools??
- Write two sentences about the status of your Design and the DT familiarity with the Digital Open-source EDA flow. Provide and Area Estimate (it may change later)
- Write two sentences about difficulties, if any, the DT encountered with the Open-Source tools and Skywater PDK usage.

Respond in Google Forms (1 per DT)

Part III : **For all Design Teams**

- Suggestions: Write-in. Provide suggestions to the UNIC-CASS team and suggest topics you feel are necessary to cover with Mentors to finish your DT tapeout.

Progress Reports Compilation

Update until Sept 19, 2023
by Rodrigo Wuerdig

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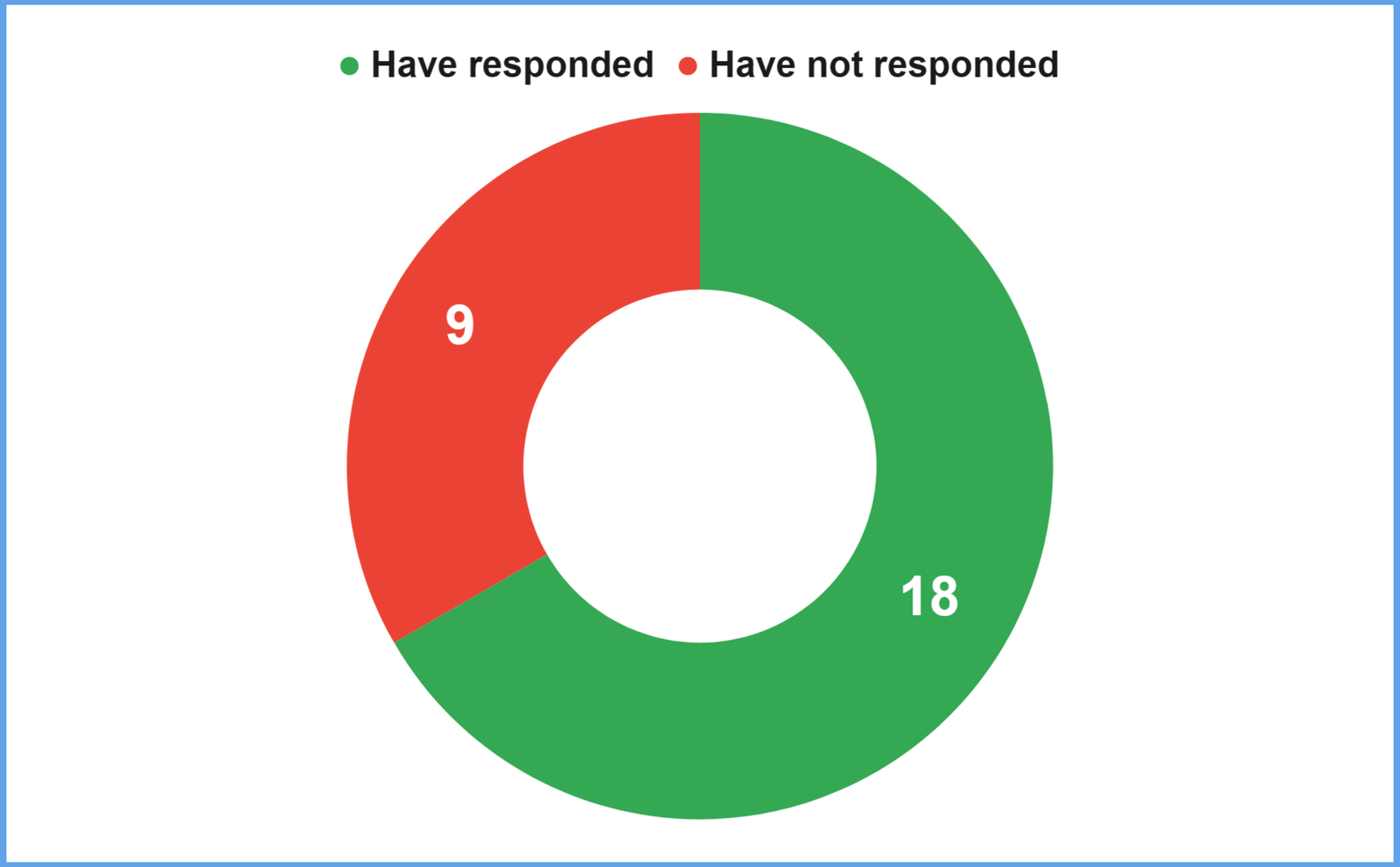
Have responded
Have not responded
9
18

DTs that have not responded by Sept 19 2023

- Development of a LDO for IoT Application (LDO_ITA)
- Design A Buck Converter for Mobile Phone Charging (B2C)
- Multi-channel analog readout
- Free DA converter
- OSIRIS I: A Low-Power 32-bit RISC Core Processor
- A Hierarchically Reconfigurable SRAM-Based Compute-in-Memory Macro for Edge Computing
- Design an 16-bit Kogge Stone Adder using GDI Technique.
- Robust 14-bit NS-SAR Converter for Process and Temperature Variations with 20 kS/s Conversion Rate.
- Development of a Device for Early Plague Detection and Plant Health Monitoring in Ecuadorian Banana Plantations

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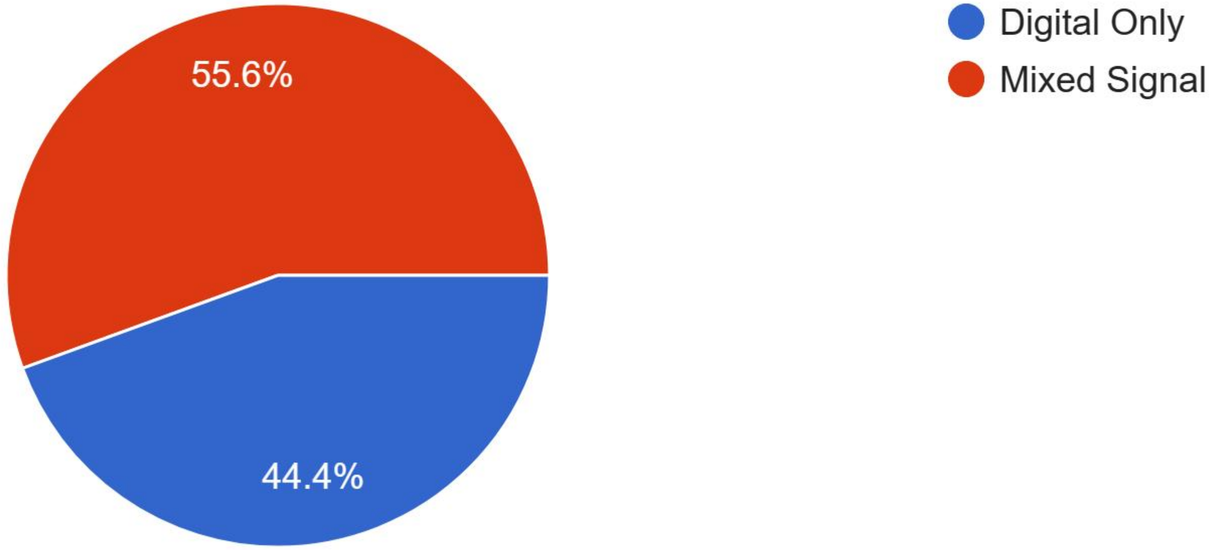
Is your design?

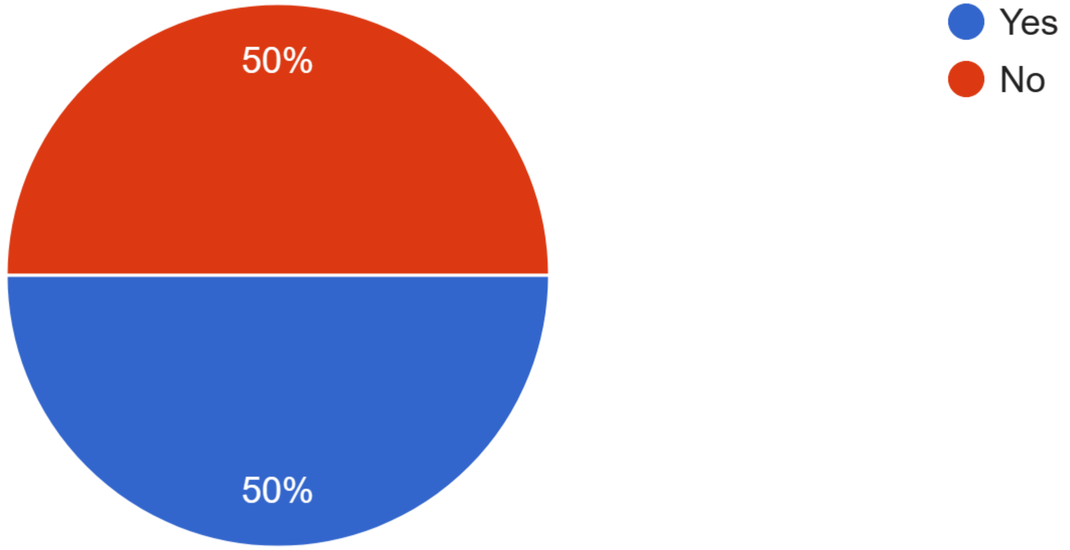
18 responses



Digital-Only

Do you have your RTL completed already?

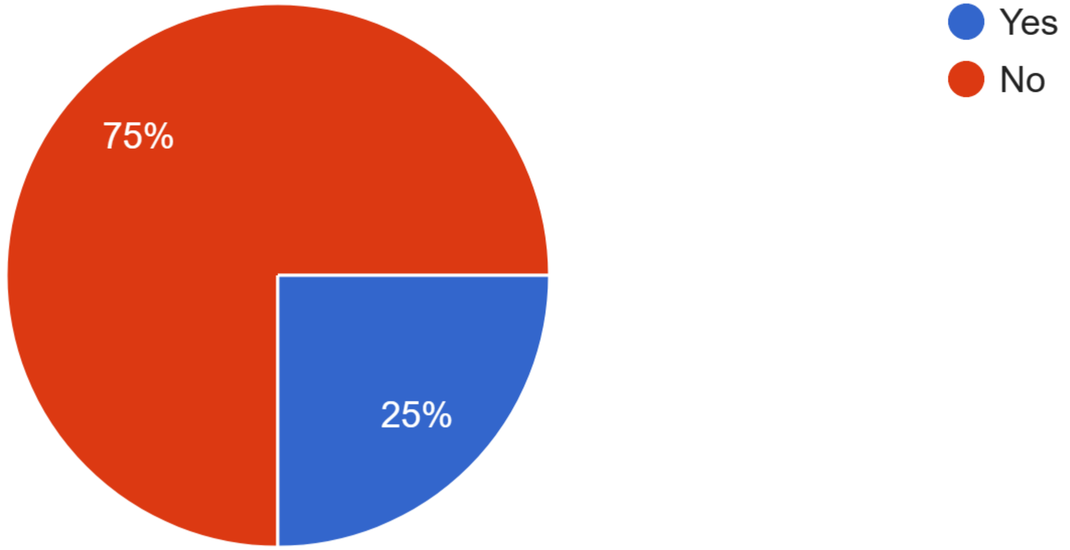
8 responses



Digital-Only

Have you completed the Logic Synthesis and the Place-and-Route steps?

8 responses



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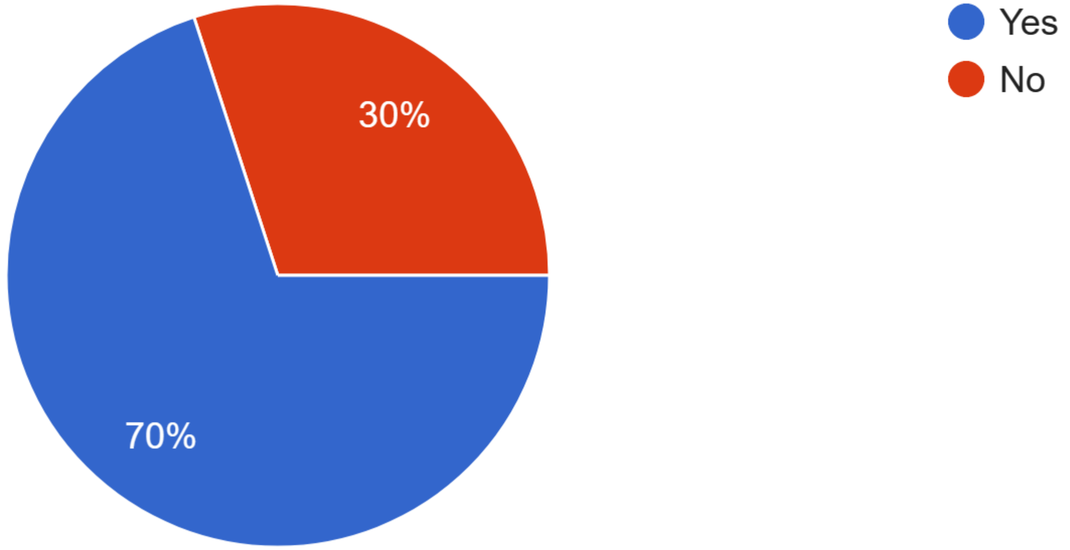
AMS-Only

Is the circuit schematic for your Design already completed in Xschem?

10 responses



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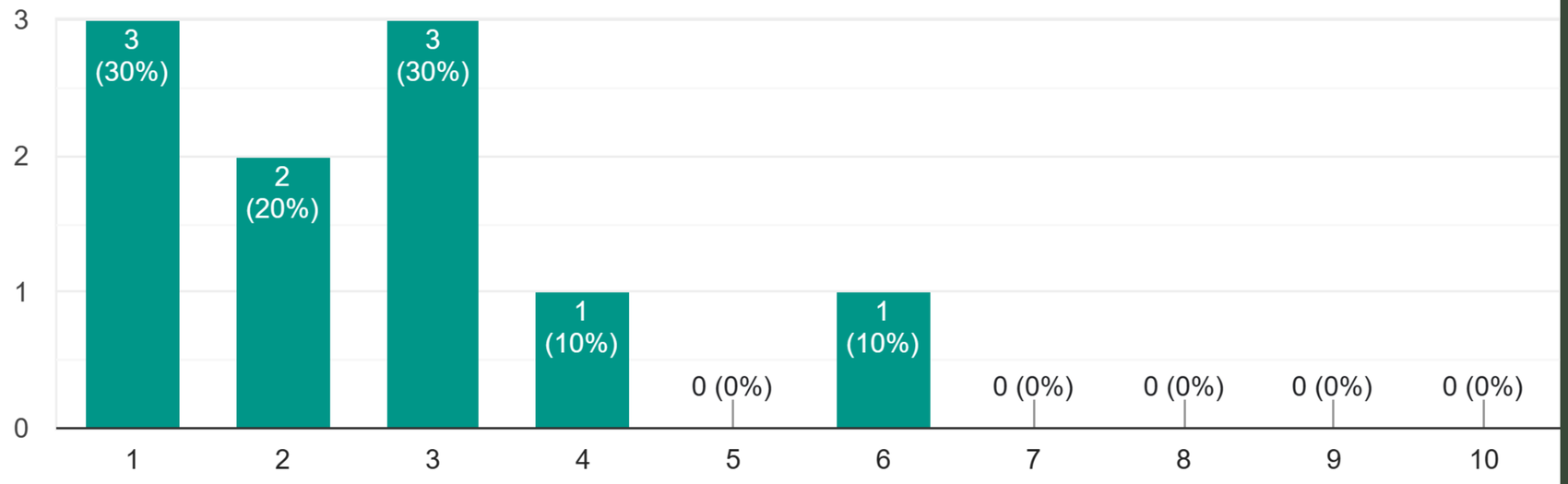
AMS-Only

Have you completed the layout of what percentage of your full custom Design (choose from 0 = 0% to 10 = 100%)

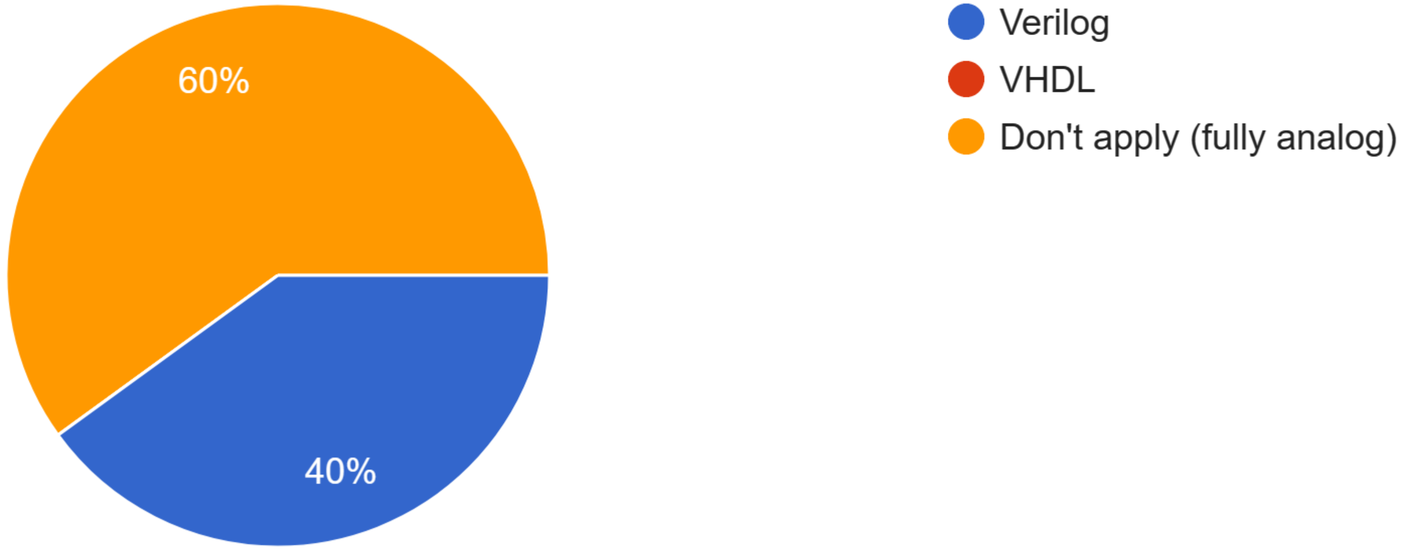
10 responses



AMS-Only

The digital blocks in your design, if needed, are they completed in RTL (like Verilog, VHDL)?

10 responses



Main Suggestions made by responding DTs

- More information about the eFabless Harness
- Tips for Mixed-Signal Integration
- More Info about DRC, LVS, and PEX
- Several Questions about Klayout
- Documentation
- Create an Interactive Zoom Session so DTs could exchange know-how among them.