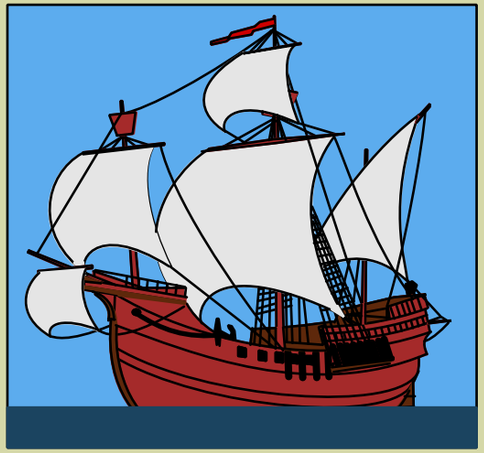
Efabless “Caravel”: Making Open Source Chips Possible

(Updated for 2024)

Tim Edwards
SVP Analog
Efabless

efabless

efabless.com



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Open source PDKs (Process Design Kits)

https://github.com/google/skywater-pdk	130nm
https://github.com/google/globalfoundries-pdk	180nm
https://github.com/IHP-GmbH/IHP-Open-PDK	130nm

Public forum:

open-source-silicon.slack.com

Join here:

https://join.skywater.tools

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https://efabless.com

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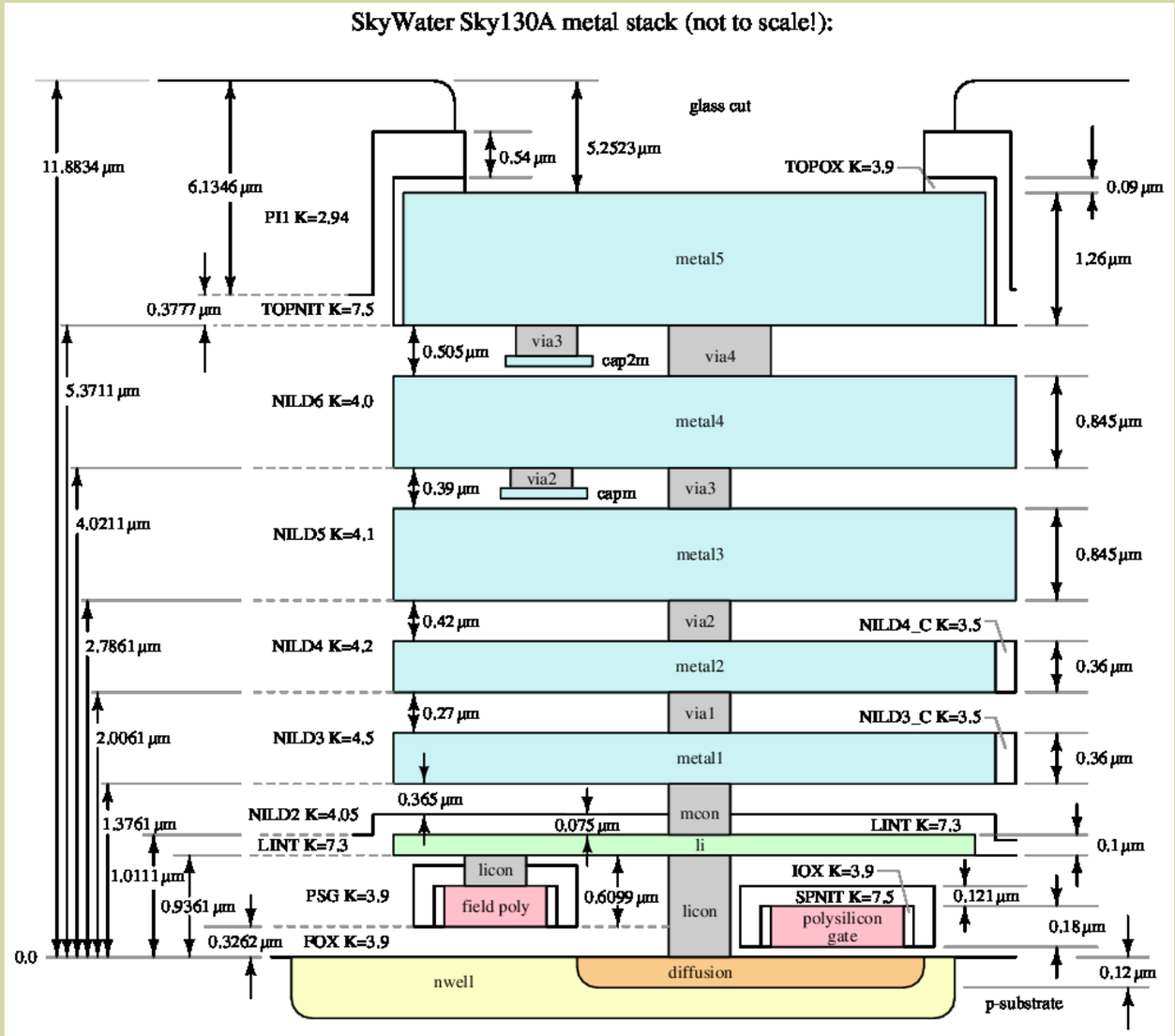

skywater

Sky130

130 nm, 6 metal stack process

double-layer MiM cap

high sheet rho poly resistors

deep n-well

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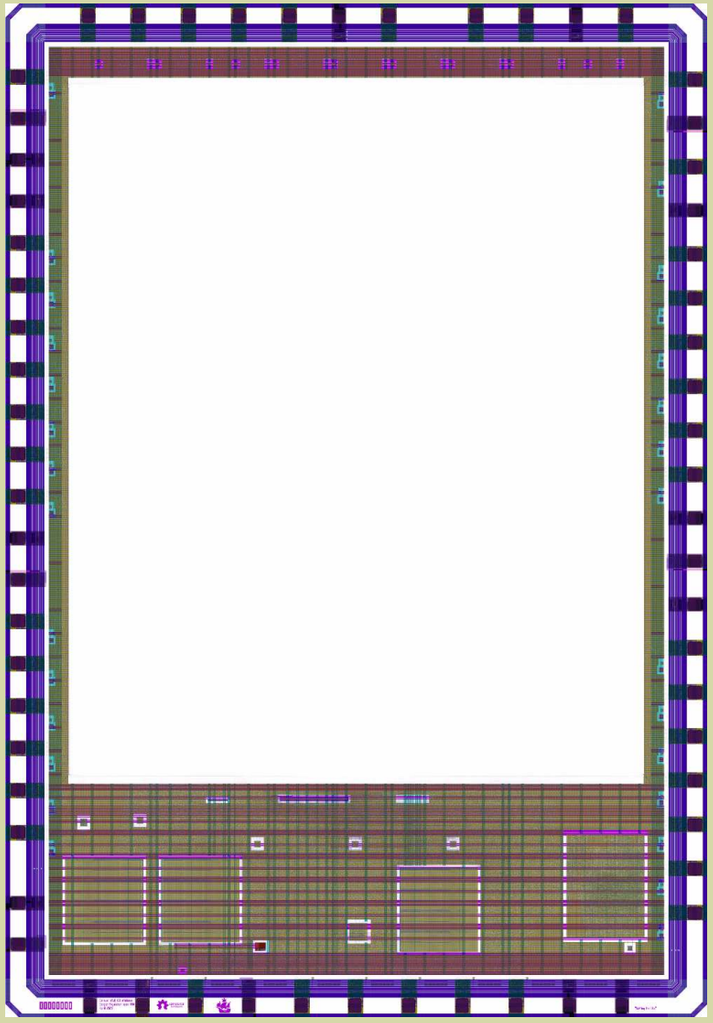
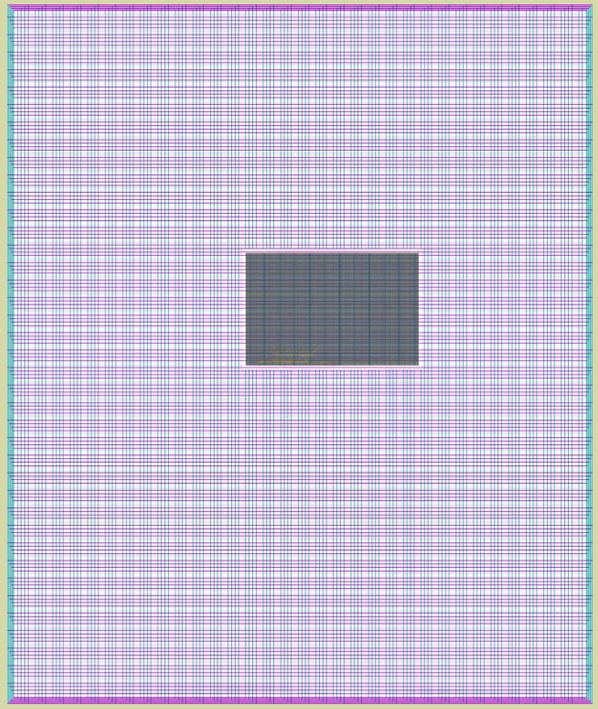
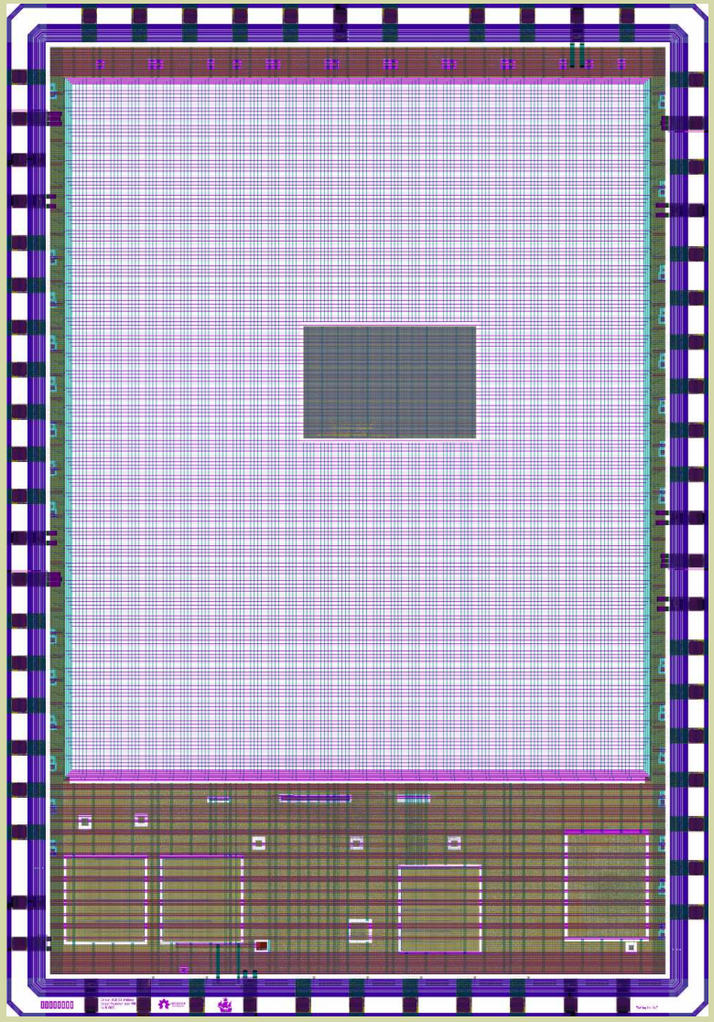
Harness + User Project = Completed chip







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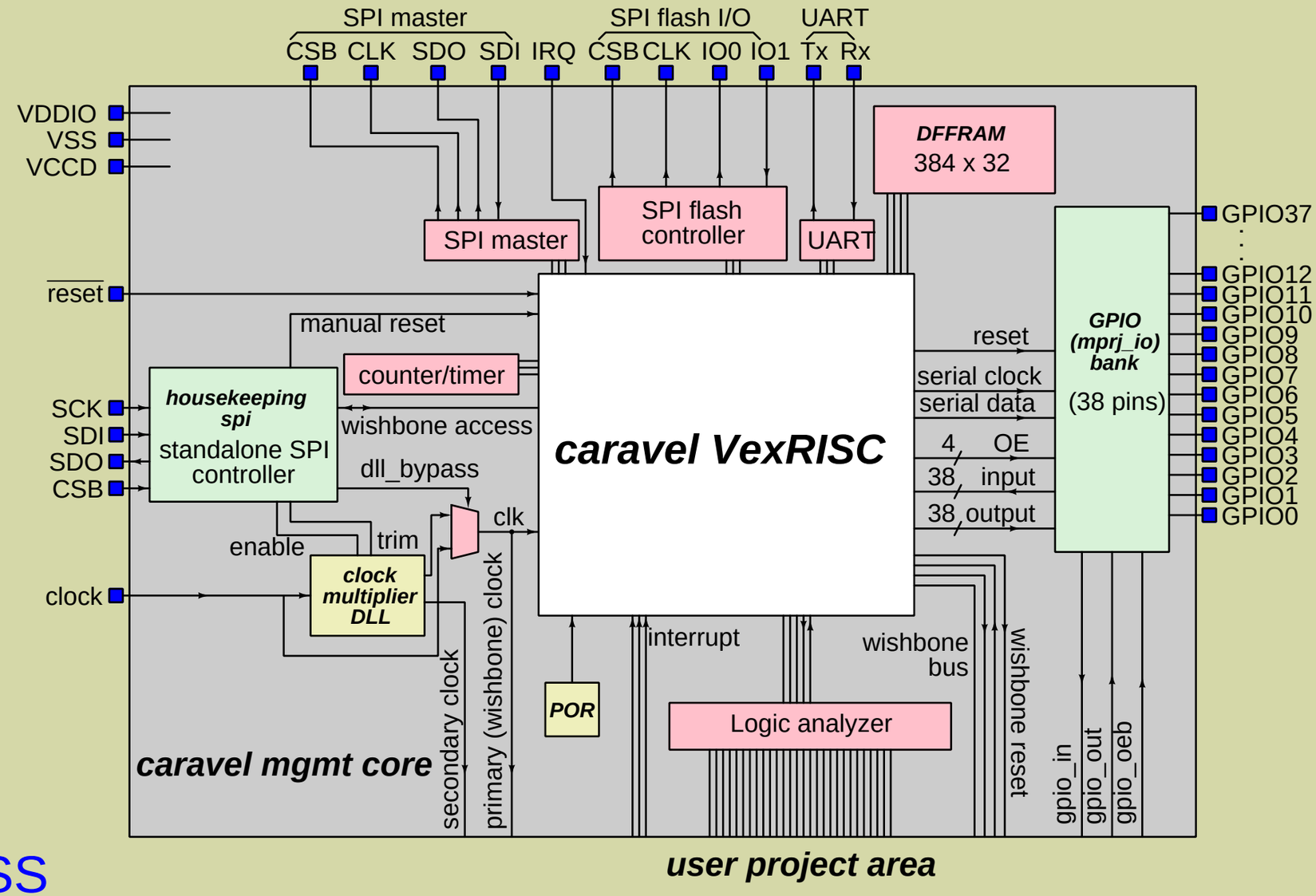
Caravel microcontroller (“management”) part:



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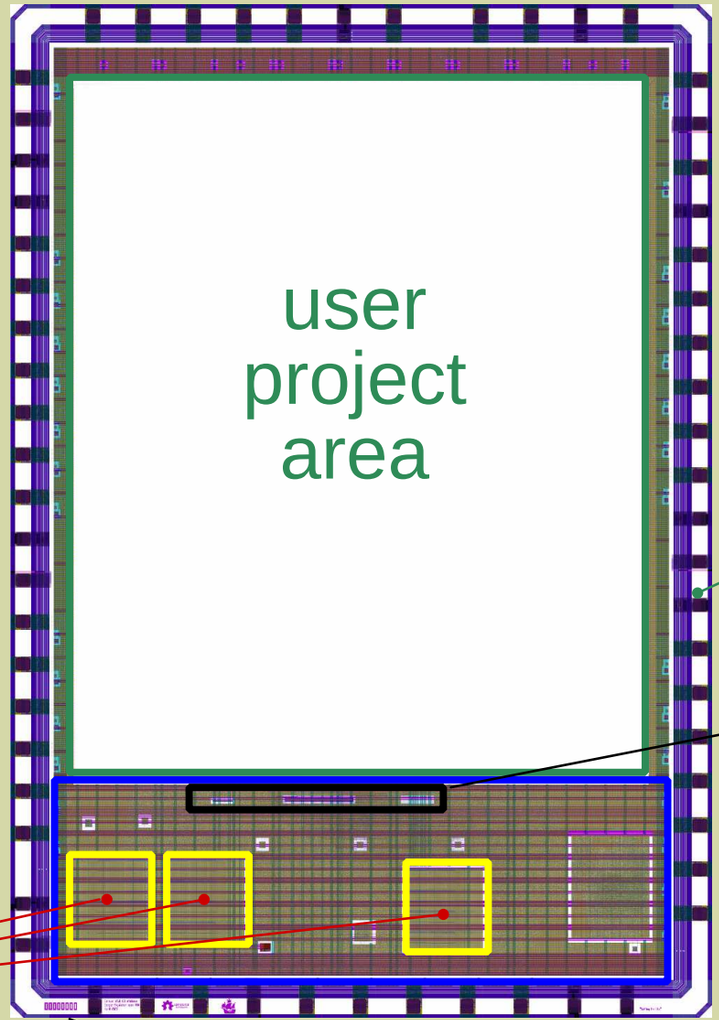

“Caravel” user project harness

3.6 × 5.2 mm

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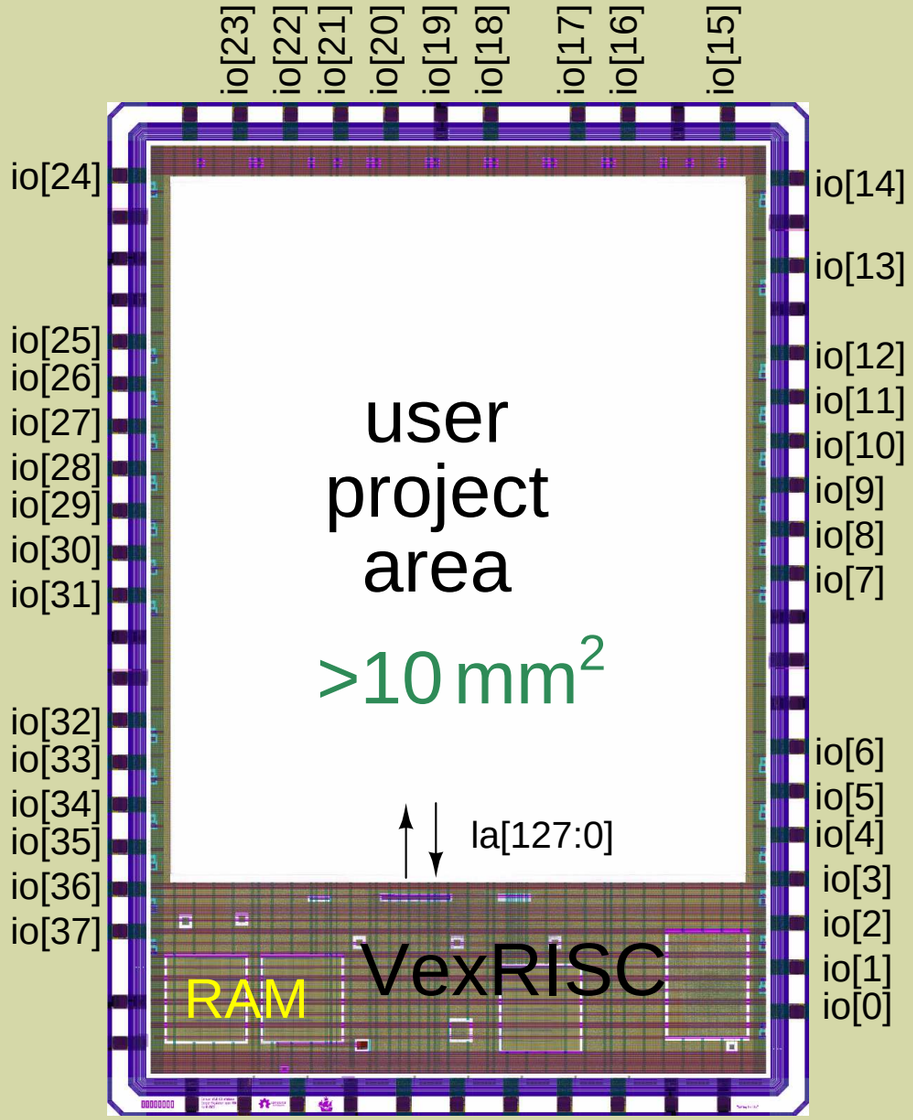

GPIO pins connect the user project to the outside world.

Internal “logic analyzer” connects the user project to the microcontroller.

38 pins GPIO

8 pins for microcontroller

14 power/ground pins

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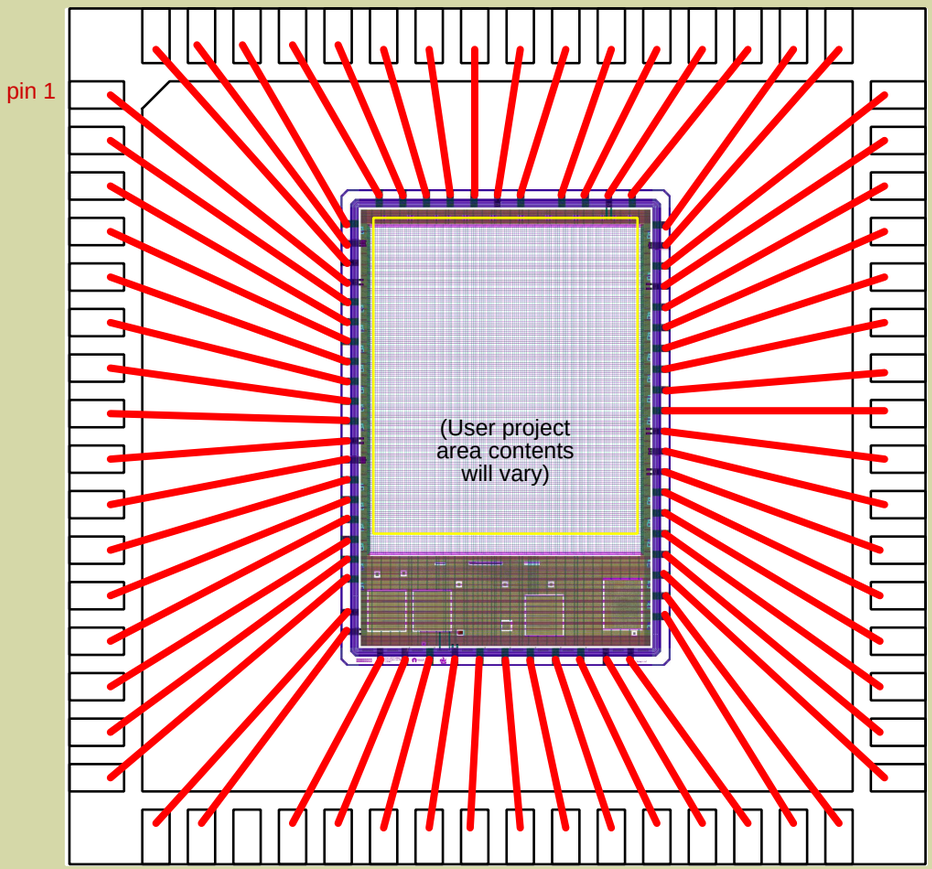
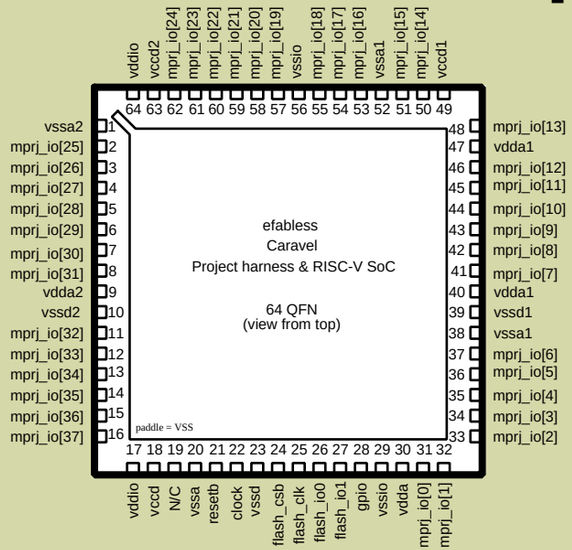
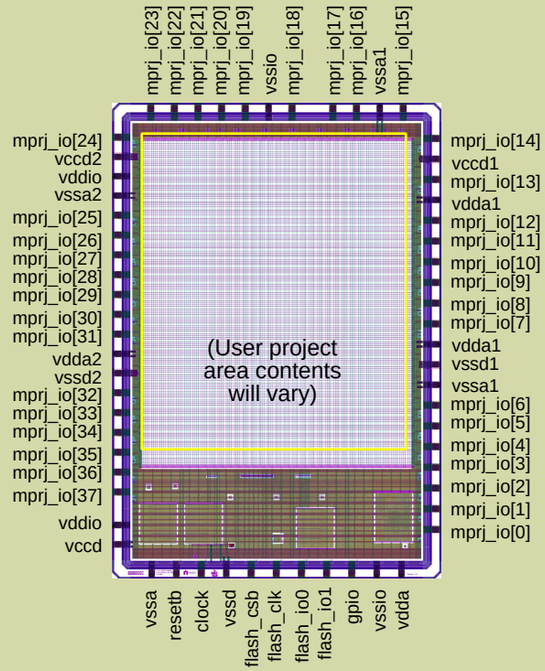
efabless "caravel" project harness 64-pin QFN package version
February 8, 2023 Revision 1

(Updated for Caravel version v3)







package size = 9 mm × 9 mm
paddle size = 7.63 mm
pin pitch = 0.5 mm

Caravel padframe dimensions = 3.588 mm × 5.188 mm

Caravel die dimensions = 3.60 mm × 5.20 mm

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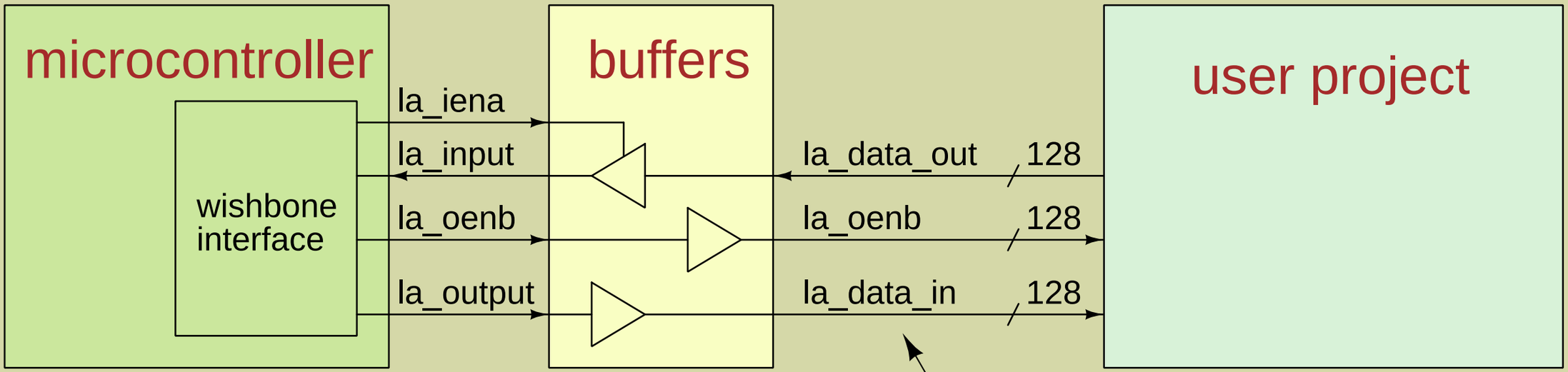
“Logic Analyzer”



In program:

reg_la0_data ... reg_la3_data
reg_la0_data_in ... reg_la3_data_in
reg_la0_oenb ... reg_la3_oenb
reg_la0_iena ... reg_la3_iena

(user_project_wrapper pins)

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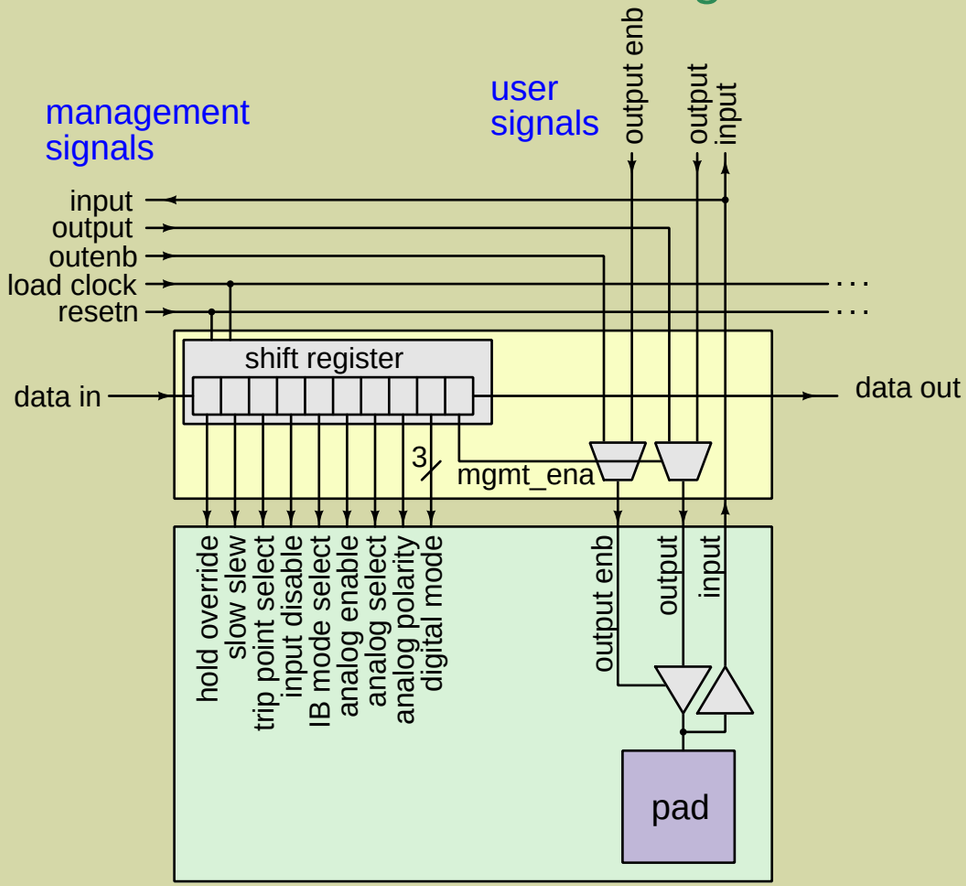
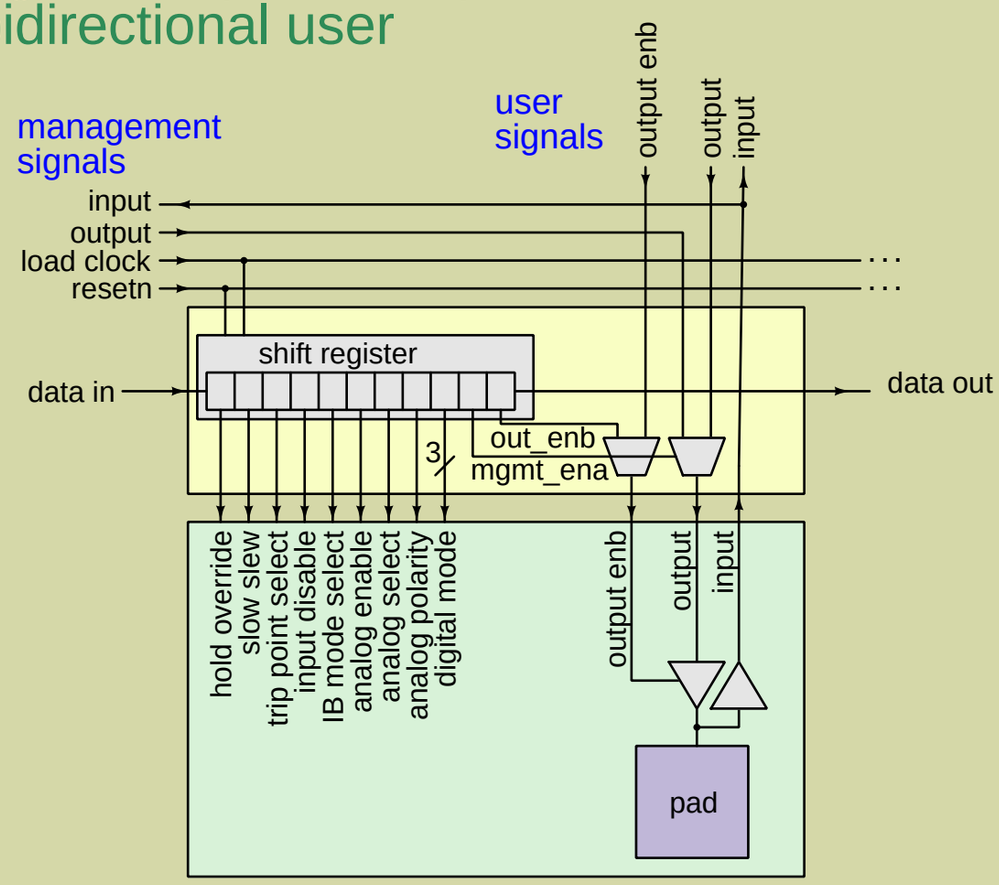
General-Purpose I/O (GPIO)

Full bidirectional user/managment



Managment input or output, Full bidirectional user



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Additional digital logic functions available to the user project:

- 3 user project interrupts to the microcontroller
- 32-bit up/down, one-shot/continuous counter/timer
- Wishbone interface between microcontroller and user project
- Additional programmable clock input to user project
- Pass-through programming of SPI flash

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Additional on-chip resources:

- Power-on-reset:
  - Power supply monitoring w/50ms startup delay
- Digital locked loop:
  - Programmable delay ring oscillator
  - Locks to external clock
  - 60 to 120 MHz system clock
  - Clock bypass mode

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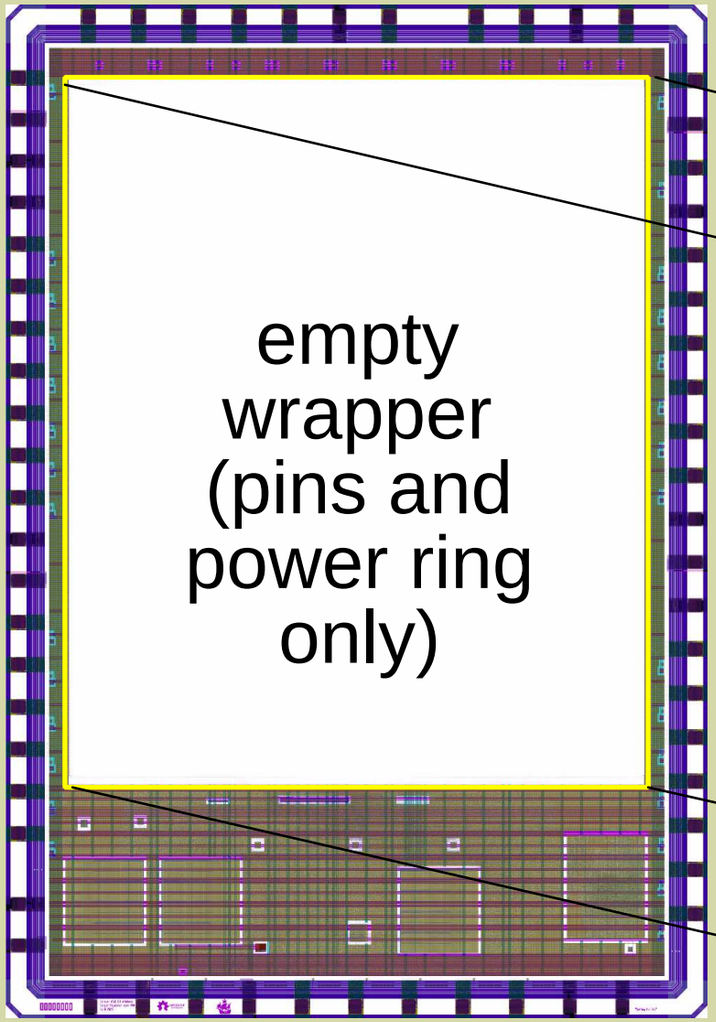
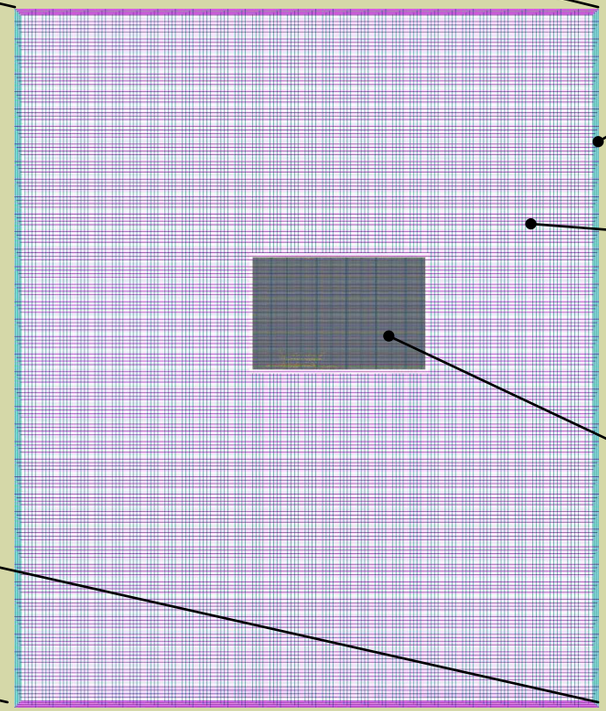
Building the User Project





populated
wrapper

Power bus rings pre-built in empty user area

Power grid added by place & route tools

Synthesized user project (up to size of project area)

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Building the User Project

Starting the user project (digital design flow):

- Clone or fork: https://github.com/efabless/caravel_user_project
- Add verilog source for project
- Follow instructions for synthesis, place, route, assembly, verification
- Simple “make” targets for generating layout using OpenLane
- Analog projects: clone or fork
  https://github.com/efabless/caravel_user_project_analog

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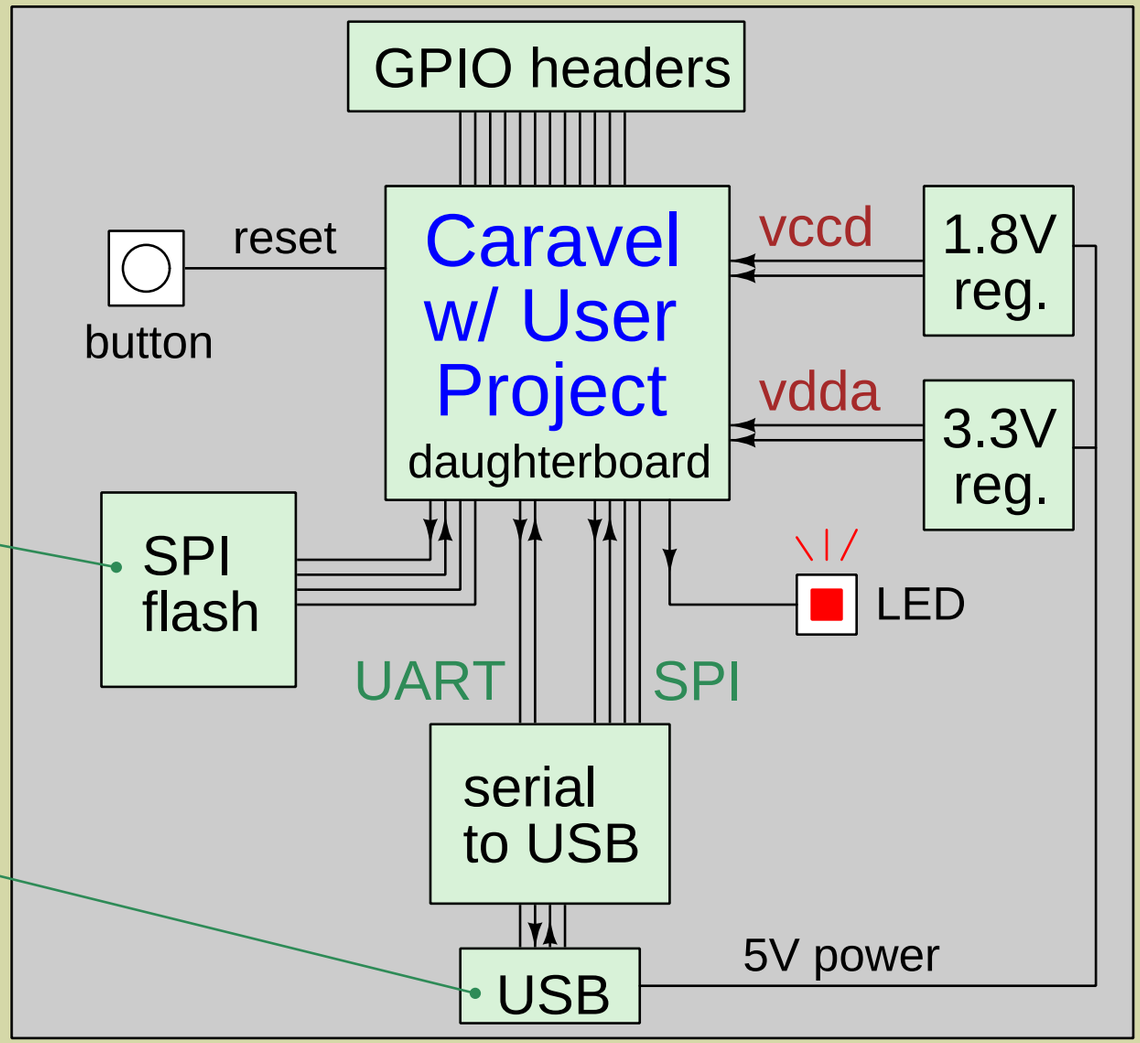
Development Board

Clone: https://github.com/efabless/caravel_board



Program to run on the RISC-V processor goes here

Communication with host computer via python scripts

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Typical project power-up sequence:

- Development board powers up microcontroller
- Power-on-reset circuit enables microcontroller
- Microcontroller runs program from SPI flash
  - Program (optionally) configures GPIO for user project
  - Program (optionally) resets user project
  - Program (optionally) controls/monitors user project

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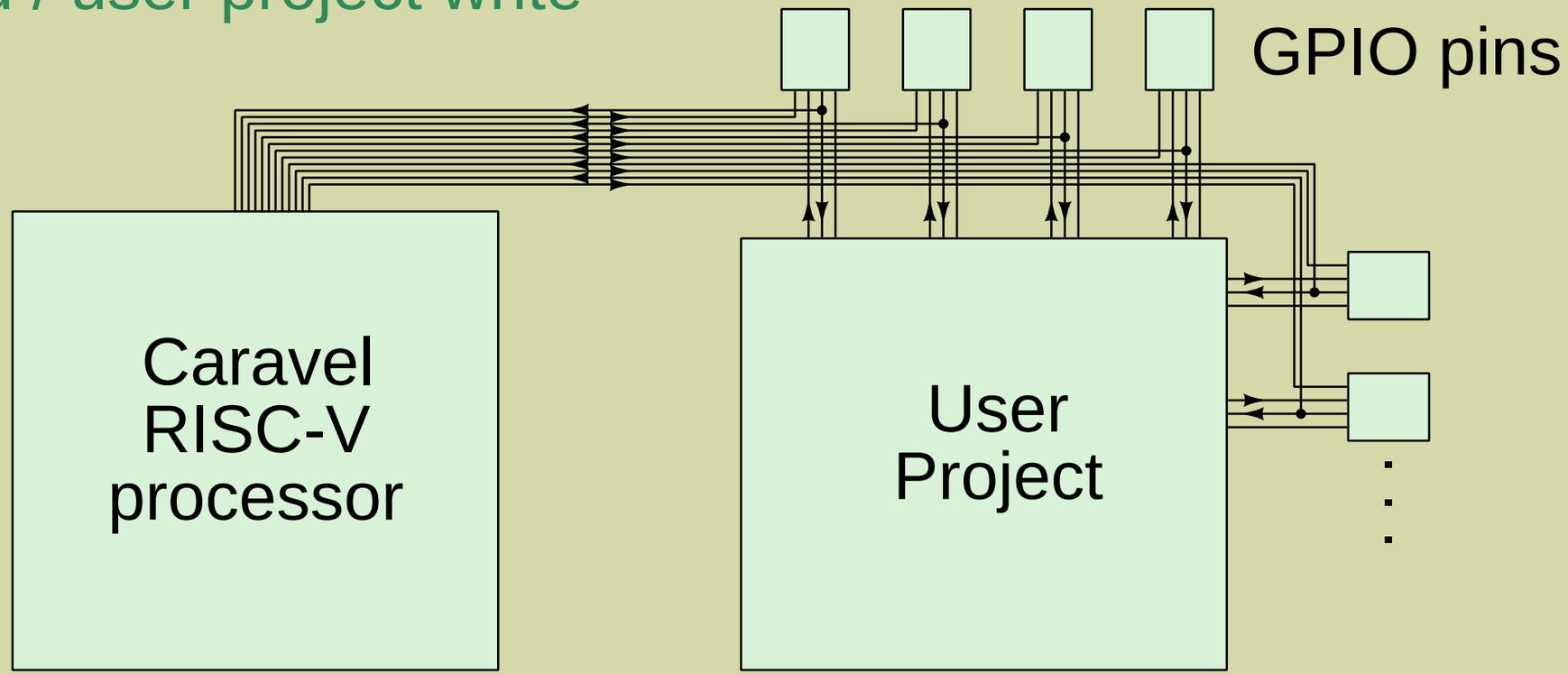
Processor driving user project through pins

Pads operate with
processor write / user project read, or
processor read / user project write



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Validating the User Project

Simulation

Using open-source simulator “iverilog”

Simulate RTL and gate level

Top level modules simulate entire board-level system

LVS

Using open-source tool “netgen”

Part of OpenLane “make” scripts—fully automated

Pre-check

Run as local script and by efabless for tape-in

Metadata checks

DRC checks

Layer density checks

XOR check

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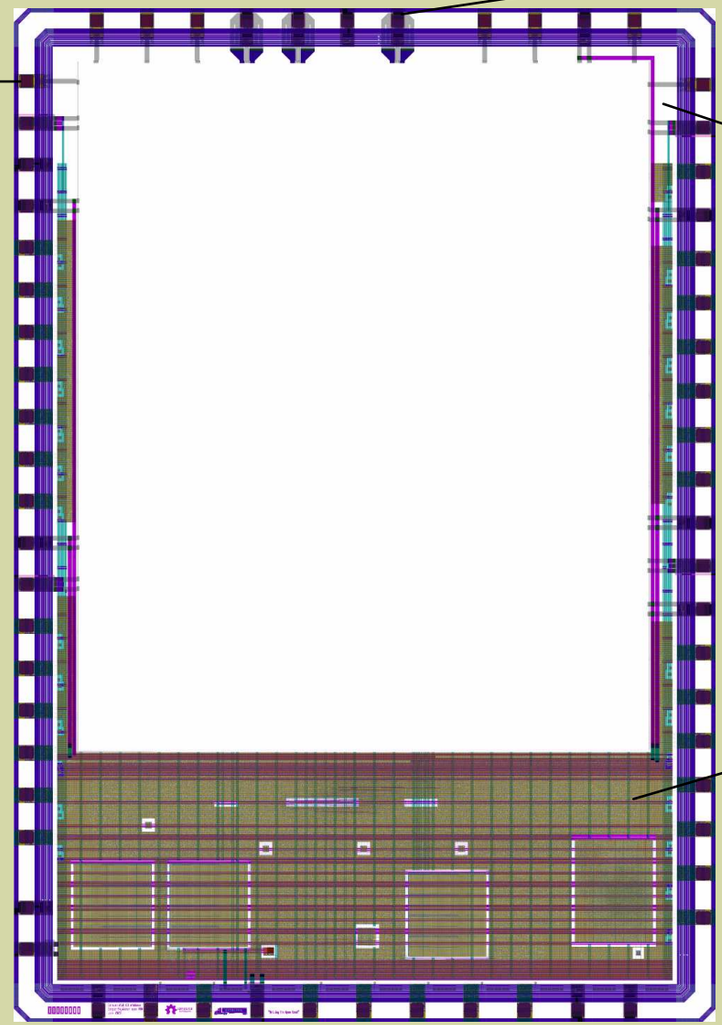
Alternatives to the Caravel harness design flow:

1. Caravan

Bare pads for analog signals (up to ~2GHz)

High current capacity pads

No digital under analog areas



Same RISC-V processor and other infrastructure

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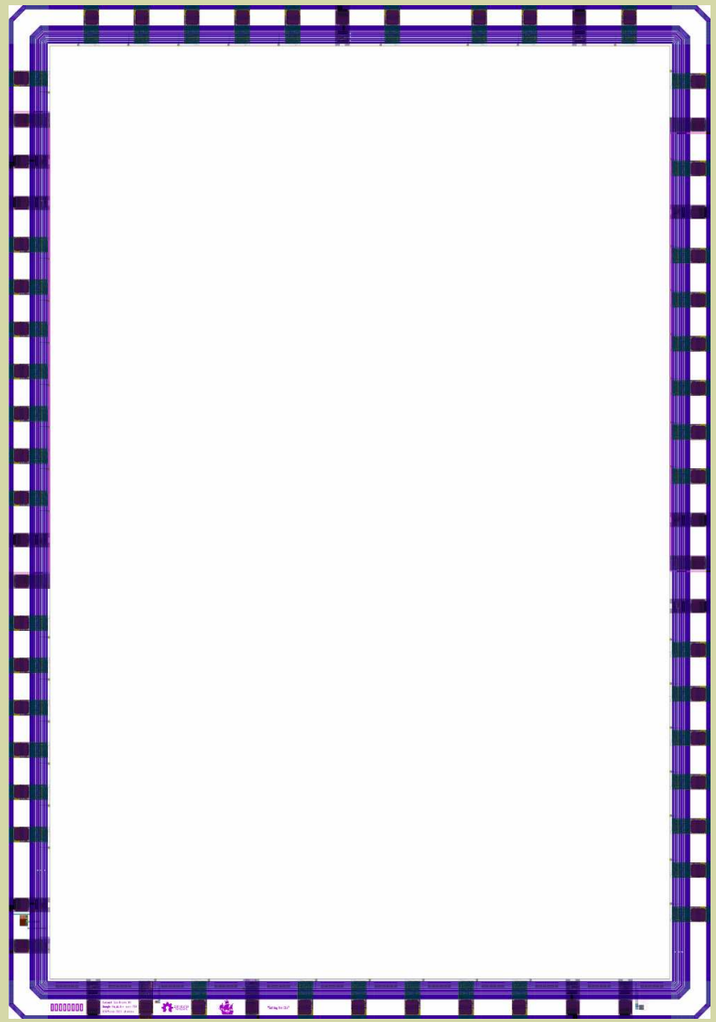
Alternatives to the Caravel harness design flow:

2. Openframe

Just the Caravel padframe, without the processor.



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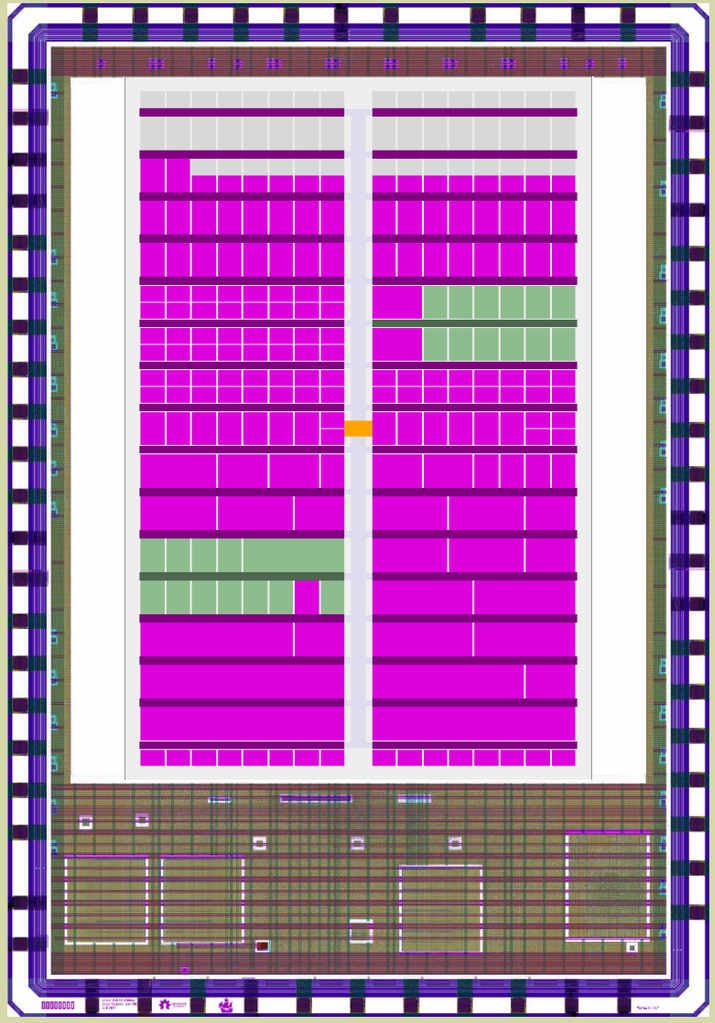
Alternatives to the Caravel harness design flow:

3. TinyTapeout

tinytapeout.com



Best pricing for simple circuits for learning at $150 per slot, $300 with development board.

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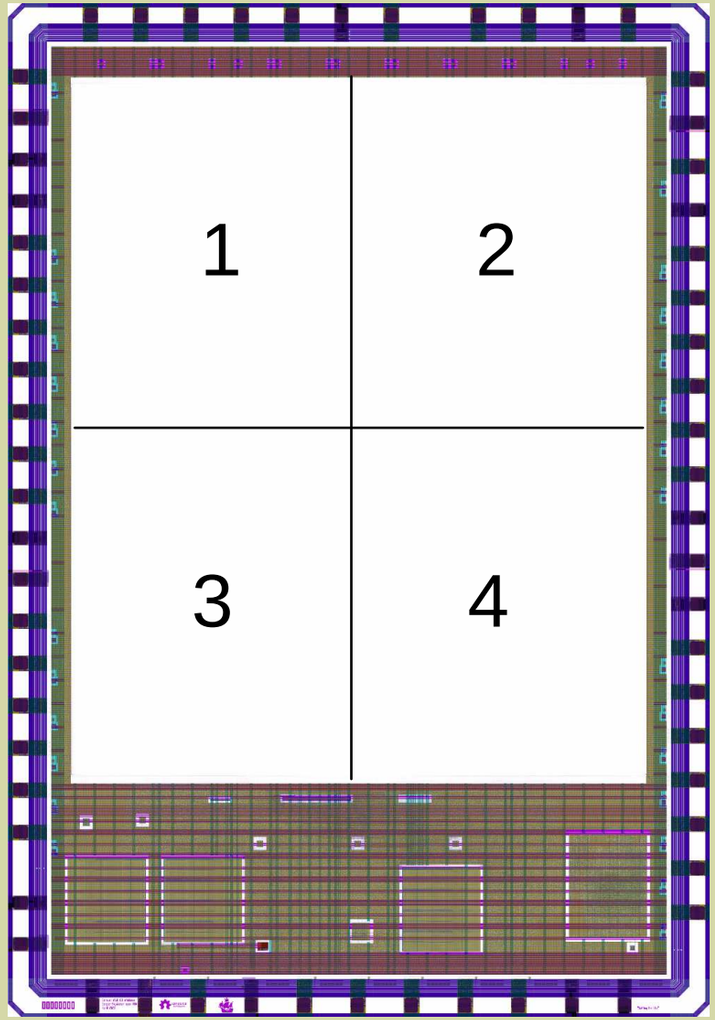
Alternatives to the Caravel harness design flow:

4. chipIgnite mini



Shared space,
lower cost.

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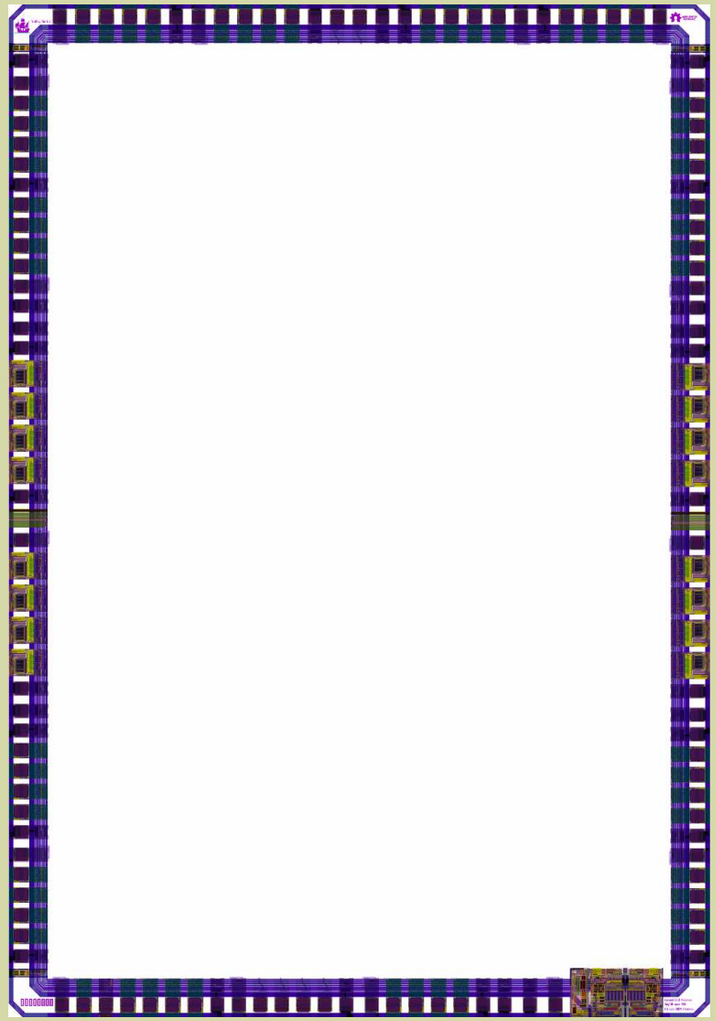
Alternatives to the Caravel harness design flow:

5. Panamax (coming next year!)

128 pins total

9 banks of 8 GPIO
(72 GPIO total)



overvoltage-tolerant pads

differential GPIO pad

analog pads

reference voltage generators

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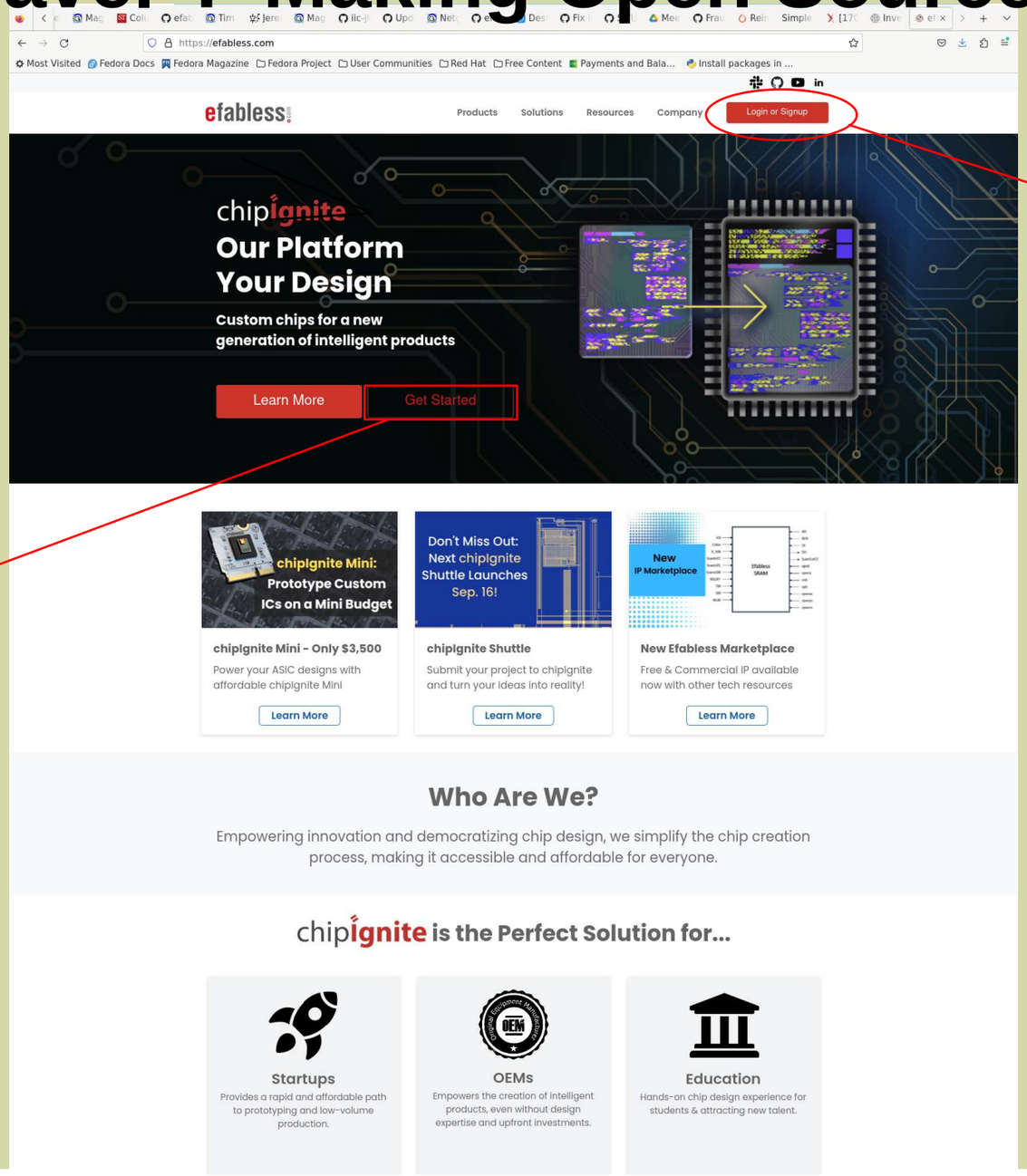
Efabless
front page



Register here

Instructions

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User dashboard

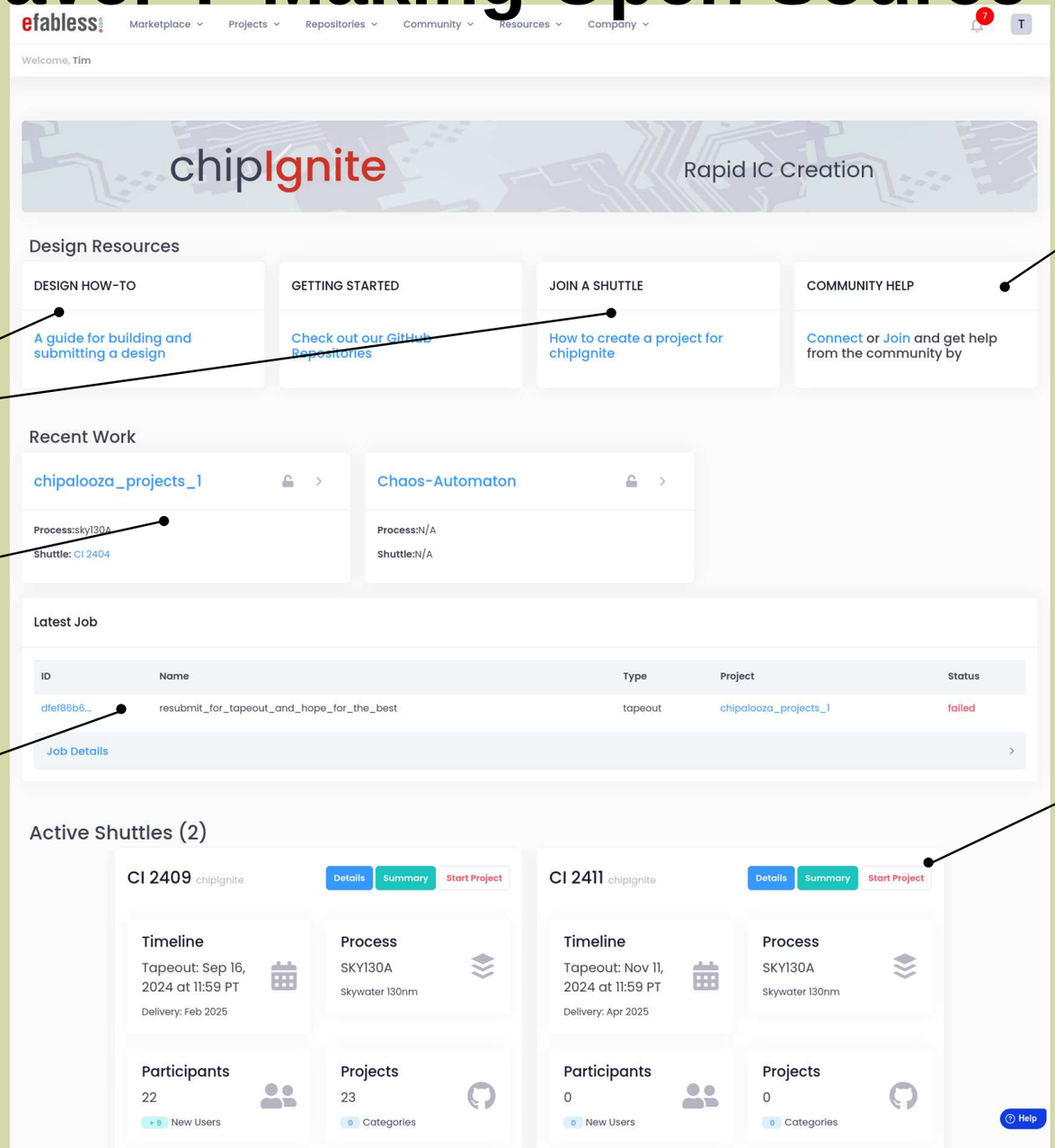
Instructional videos here

Your projects

Platform jobs (precheck, submit)

Links to Slack

Get on a shuttle!



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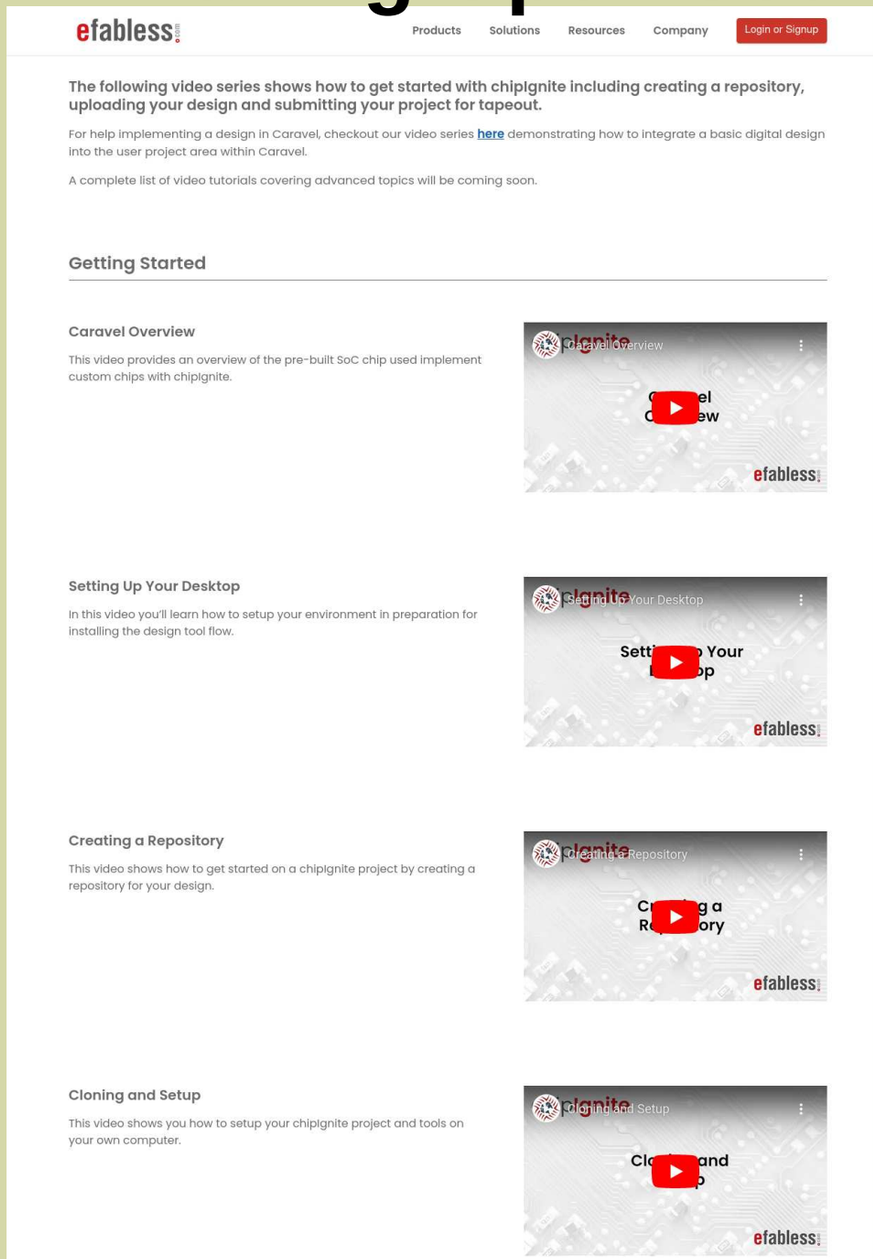
Instructional videos page

(from “Get Started” link)



Step-by-step instructions for each part of the design and submission process.

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Submitting the User Project

- User registers with efabless at efabless.com
- Follow instructional videos
- Best written instructions at
  https://github.com/efabless/caravel_user_project
- Designer creates project on Efabless platform
- Project is populated from designer's git repository
- Designer submits request to manufacture
- User project is assembled with the caravel chip
- Designer gets report from pre-checks (DRC/density/XOR)

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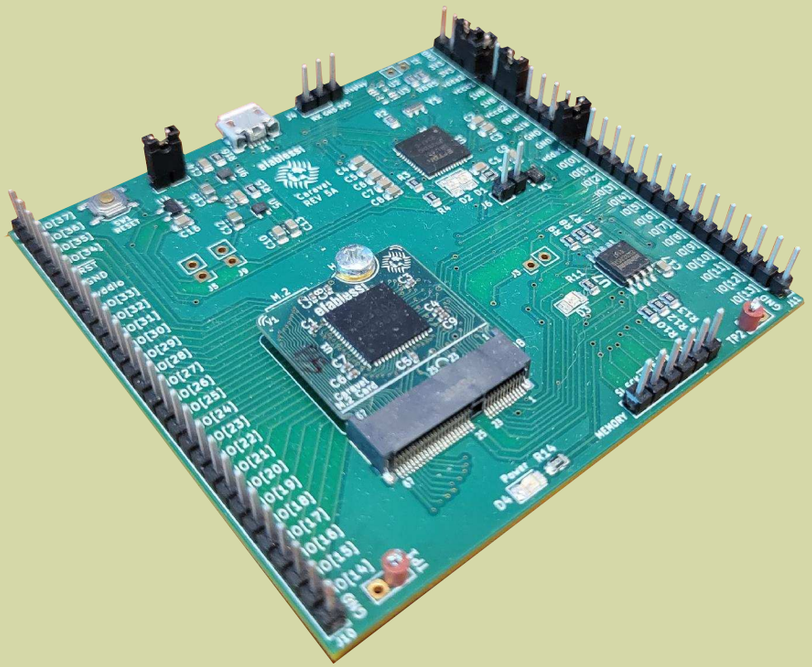
Chip's in the Mail!

- Designer receives assembled development board with their project on it.
- Board has a USB port for power and communications
- Python scripts available for programming the SPI flash
- Hex file(s) from simulation validation can be downloaded and run



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Showcase page:

Silicon Showcase

Bandgap Voltage Reference

John Kustin made this bandgap circuit as part of his graduate training. The experience is what made him decide to do a PhD in the field. It was taped out on chipIgnite and he brought it up and tested it. He used xschem for schematic and magic for layout. The bandgap achieves a TC of ~3.6 PPM/C.

Designer: John Kustin

GitHub | Layout

About the Author:
John Kustin entered the open-source silicon ecosystem during his Junior year at Stanford through Professor Priyanka Raina’s EE272B 10-week tapeout class. His open-source bandgap circuit in SkyWater 130nm won his department’s Student Design Project Award. After graduating with a BS in Electrical Engineering in June, 2022, he joined the University of Michigan to pursue a PhD in EE. John is interested in training the next generation of IC designers and democratizing IC design.

Riscduino

Riscduino is a single 32-bit RISC-V-based SoC design that is pin-compatible with the Arduino platform and targeted for the Efabless Shuttle program. This project uses only open-source toolsets for simulation, synthesis, and backend tools. The SoC flow follows the OpenLane methodology, and the SoC environment is compatible with the eFabless/Caravel methodology.

Designer: Dinesh Annayya

GitHub | Layout

About the Author
Dinesh Annaya is an ardent Open-Source EDA enthusiast and an expert user of OpenROAD™ and OpenLane. He developed a baseline RISCduino SoC, a single, 32 bit RISC-V based controller compatible with the Arduino platform . He has submitted over 15 designs on Open MPW shuttles on sky130- https://github.com/dineshannayya/riscduino. During the course of his design journey, he successively improved the design architecture for better performance, and enhanced functionality. His main motivation for the use of Open-Source EDA tools is to gauge the quality of results and potential for commercial use.

Turing-complete 8-bit MCU

A turing-complete 8-bit microprocessor based on a niche 70s architecture, successfully taped out on the first GF180 shuttle. It can easily run complex programs, such as rendering the Mandelbrot fractal, or powering a conference badge.

Designer: Luca "Tholin" H.

GitHub | Layout

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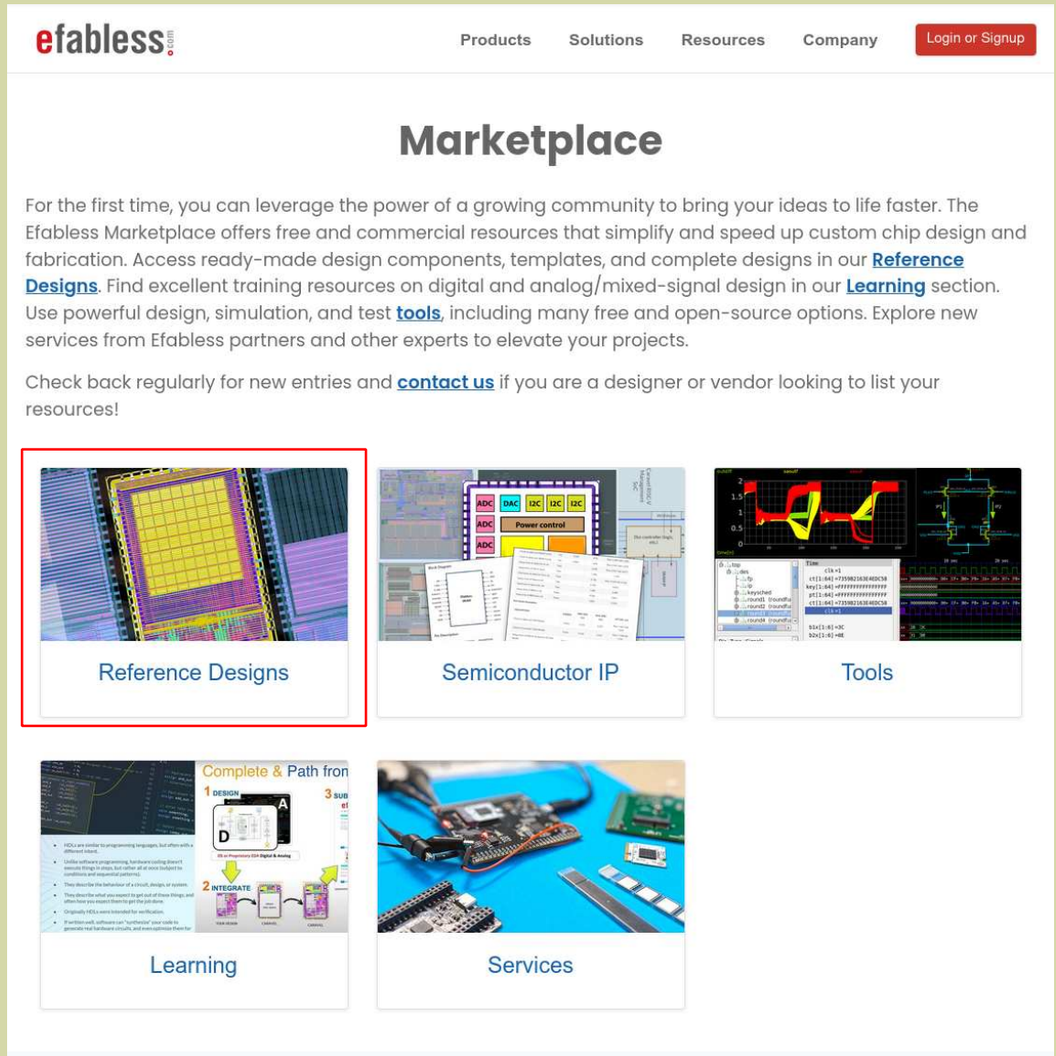
Marketplace (overhauled in 2024):



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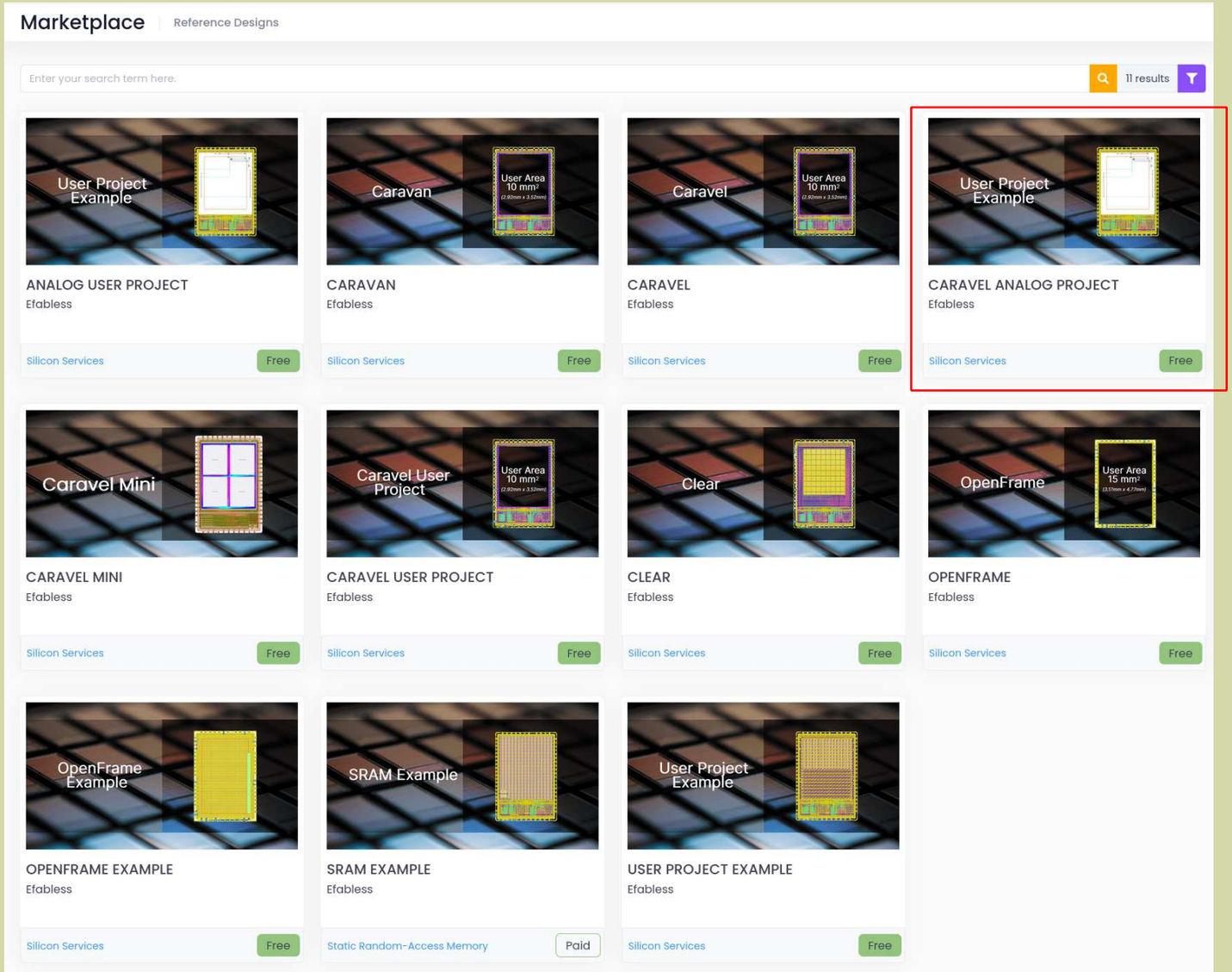
Marketplace→Reference Designs:



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Marketplace→Reference Designs→Caravel Analog Project:

Caravel Analog Project

Overview

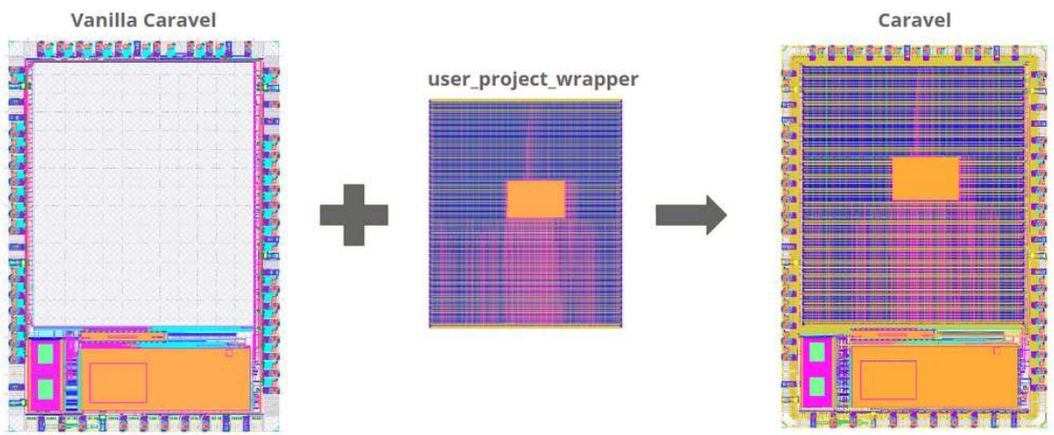
The Caravel Analog Project is a unique offering within the Caravel chip design framework that allows users to integrate their custom analog designs into a predefined space. This space, known as the user project area, is part of the overall Caravel chip and is specifically designated for user-defined logic. By utilizing the Caravel User Project, designers can incorporate their unique functionalities into a larger, professionally managed chip infrastructure, making it ideal for prototyping and small-scale production.

One of the key advantages of the Caravel Analog Project is its accessibility. It allows designers, regardless of their resources, to participate in silicon design and production. By providing a shared infrastructure and community support, Efabless lowers the barrier to entry, fostering innovation and collaboration in the field of chip design.

To ensure that all user designs are compliant with industry standards and compatible with the Caravel framework, Efabless has established a set of design rules. These rules are enforced through the `precheck` and `tapeout` flows, which are mandatory steps in the design process. The `precheck` flow validates the design against the specified rules, while the `tapeout` flow prepares the design for fabrication.

By integrating their custom designs into the Caravel User Project, users benefit from the robust features of the Caravel chip, including a RISC-V core, multiple I/O interfaces, and comprehensive debugging capabilities. This integration enables rapid development and testing of new ideas, significantly reducing time-to-market and development costs.

Analog designs can be integrated in either Caravel or Caravan, the only difference is that Caravan has bare pads, for experienced designers. Caravan should only be used if you are experienced, and the design is meant to be used in a controlled enviroment in a lab, it is only meant for prototyping. Otherwise, users designing analog projects are recommended to use Caravel.



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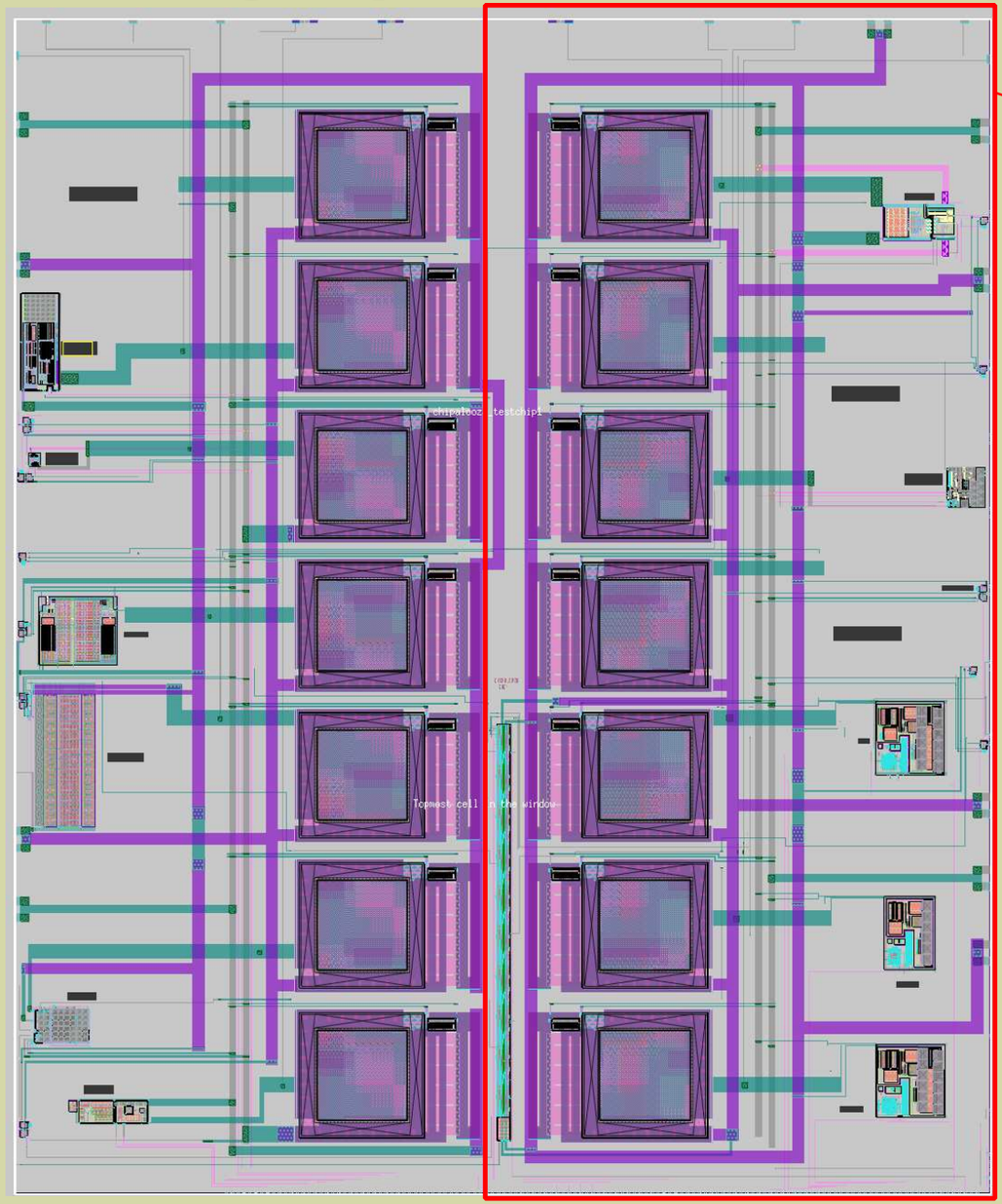
Analog multi-project integration

See:
github.com/
RTimothyEdwards/
chipalooza_projects_1



isosub around entire project area excluding deep-nwell regions

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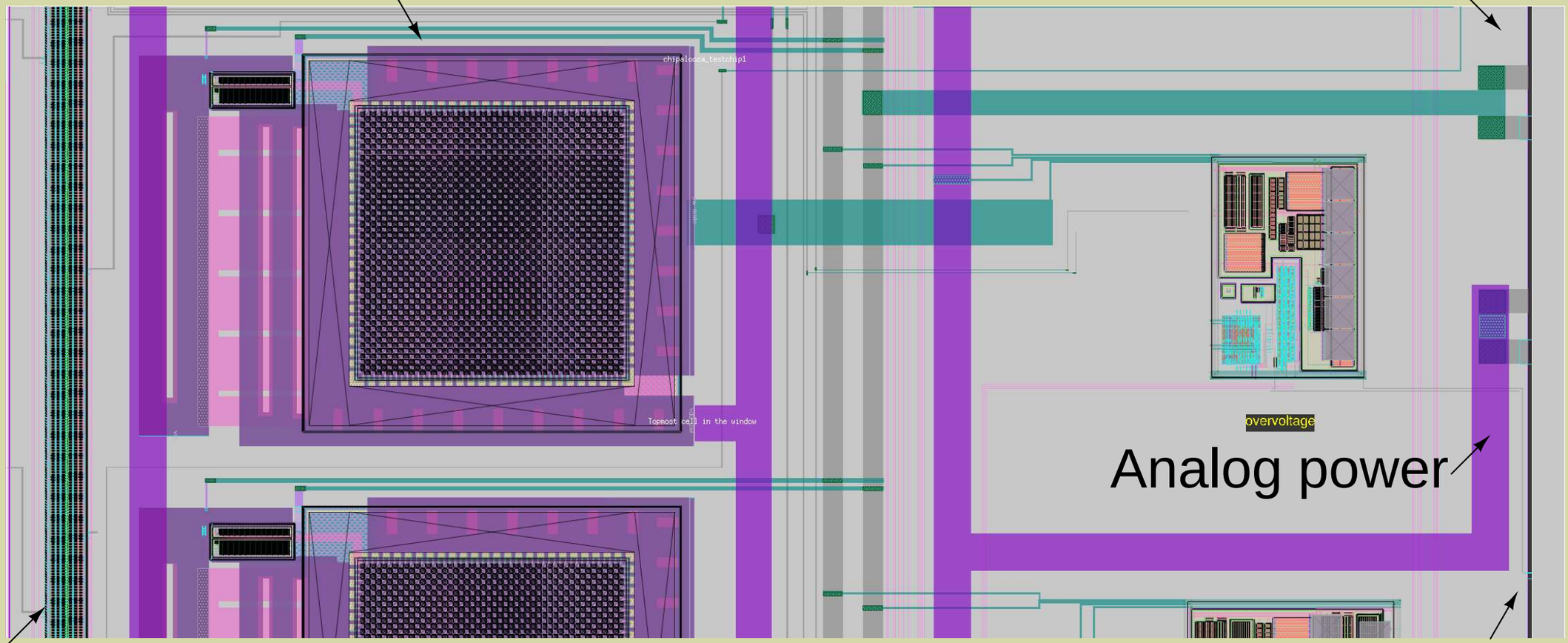
Analog multi-project integration

Power FET (Weston Braun)

Digital power



Analog power

Bias current generator

Analog signal I/O

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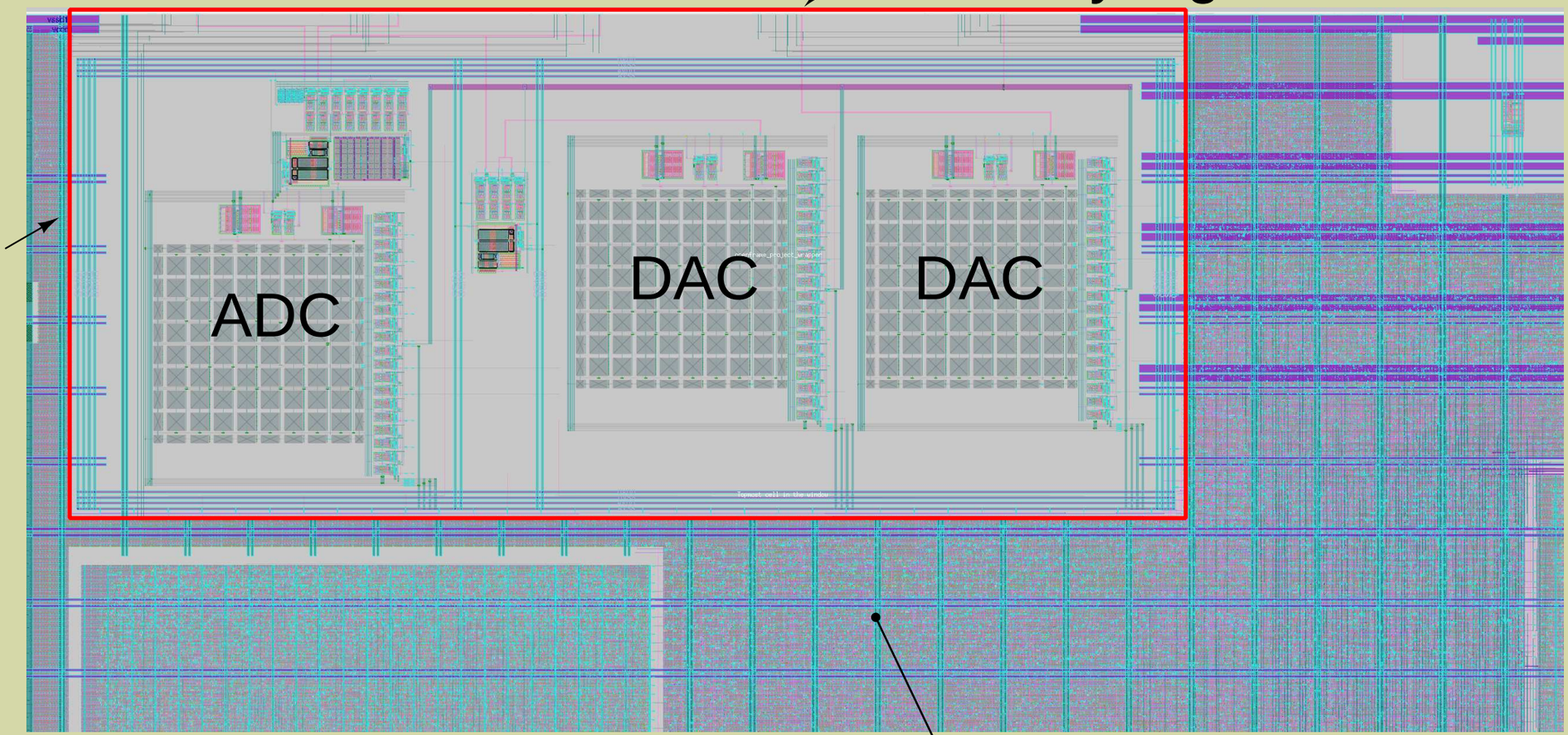
Integrate analog as macro in a digital synthesis environment

Openframe wrapper:

Analog signals abut frame,not routed by digital router



Analog macro

Digital core

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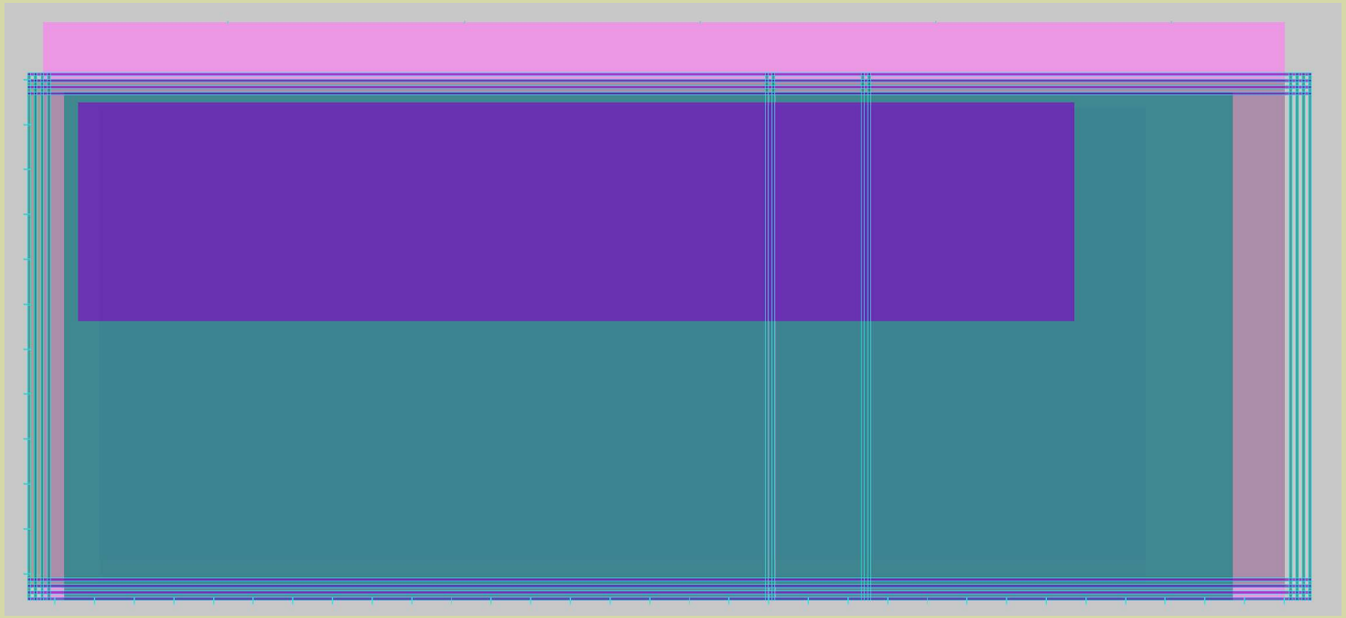
Analog multi-project integration



Analog macro is a LEF file as seen by the digital place & route tools (openlane)

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Thank you for listening!

Thank you for participating!

Keep it open source!