

Efabless “Caravel”: Making Open Source Chips Possible

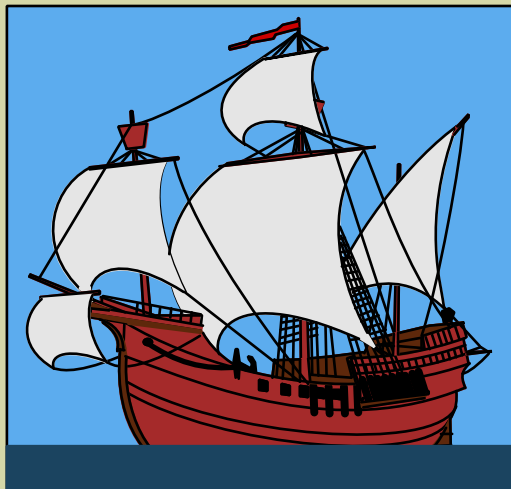
(Updated for 2024)



efabless
efabless.com



Tim Edwards
SVP Analog
Efabless



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Open source PDKs (Process Design Kits)



<https://github.com/google/skywater-pdk>

<https://github.com/google/globalfoundries-pdk>

<https://github.com/IHP-GmbH/IHP-Open-PDK>

130nm

180nm

130nm

Public forum:

open-source-silicon.slack.com

Join here:

<https://join.skywater.tools>

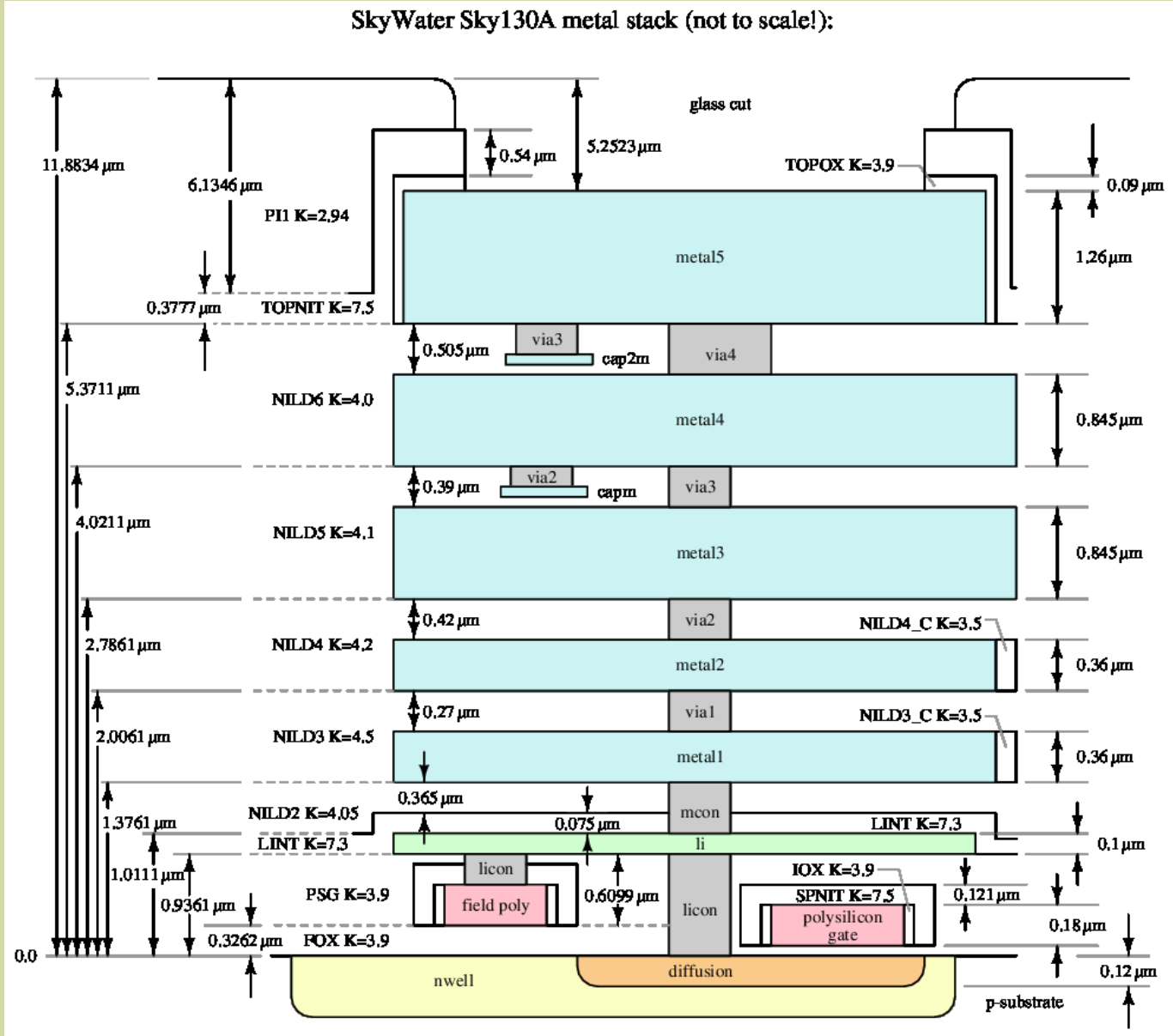


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<https://efabless.com>

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Sky130

130 nm, 6 metal stack process
 double-layer MiM cap
 high sheet rho poly resistors
 deep n-well

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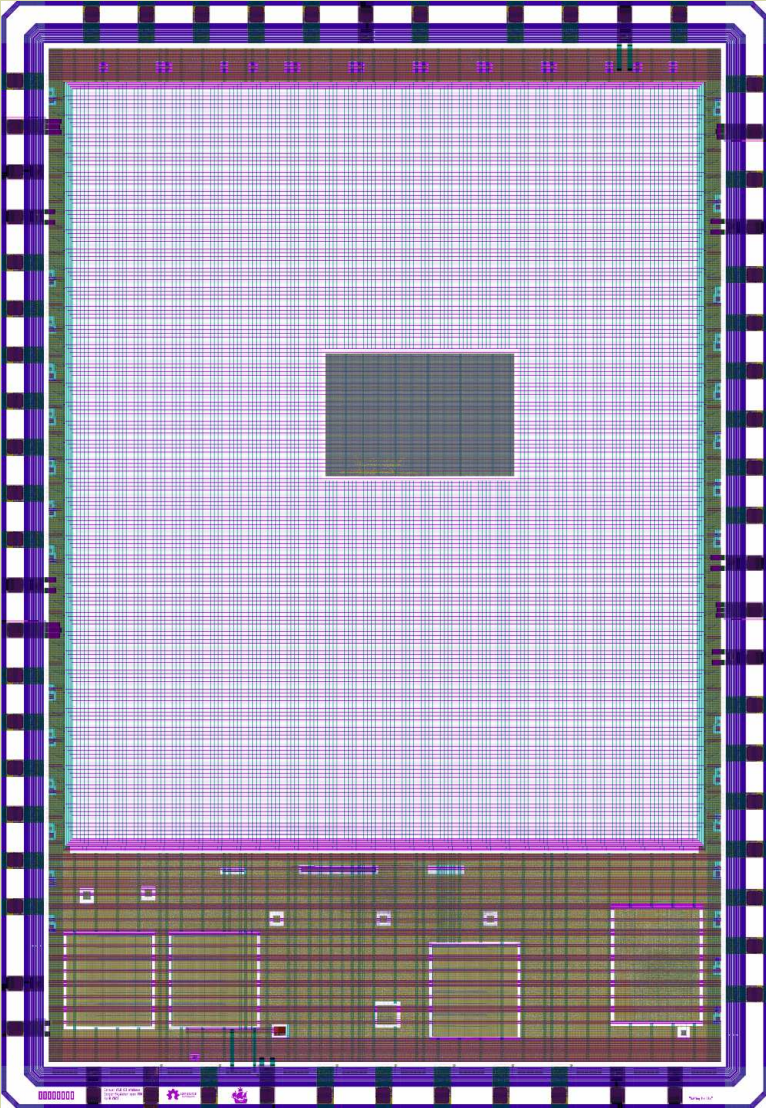
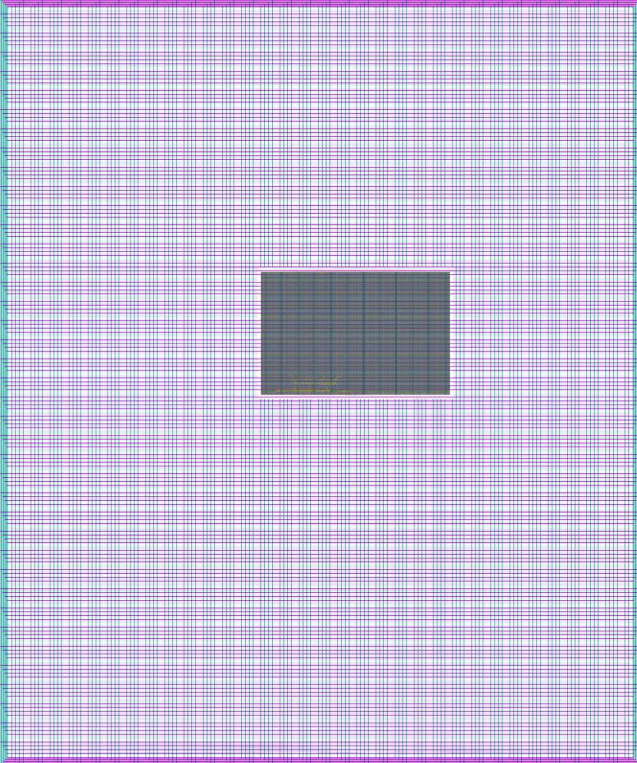
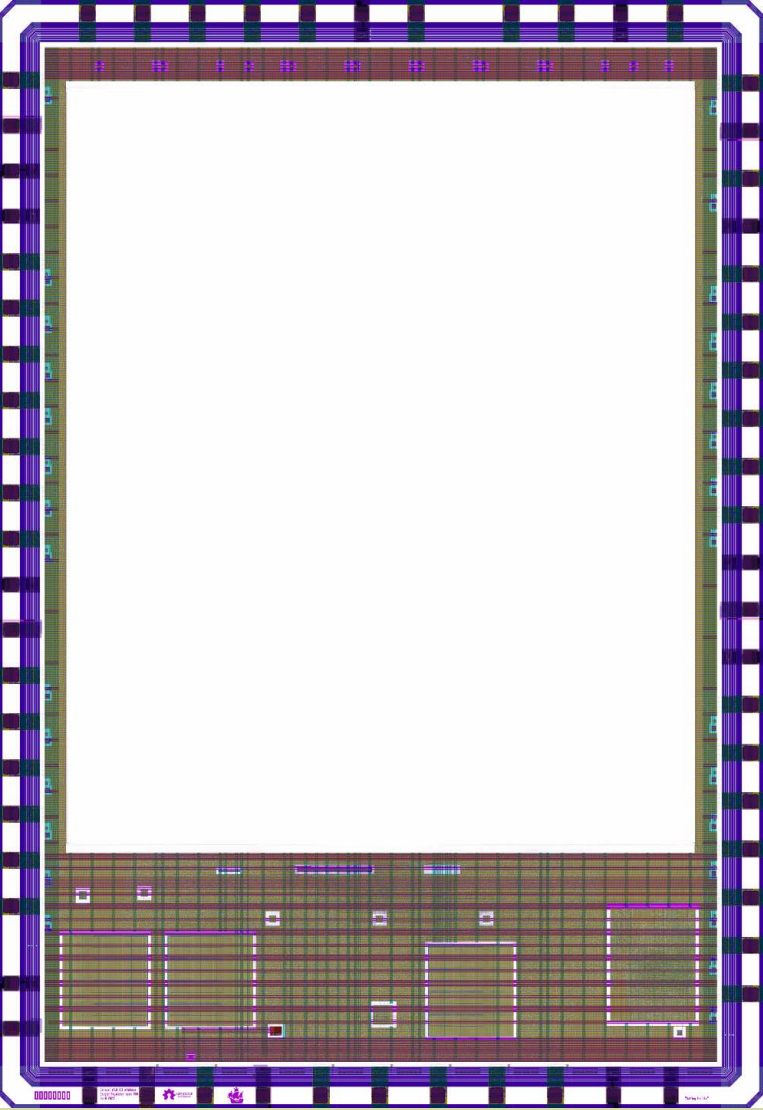
Harness

+

User Project

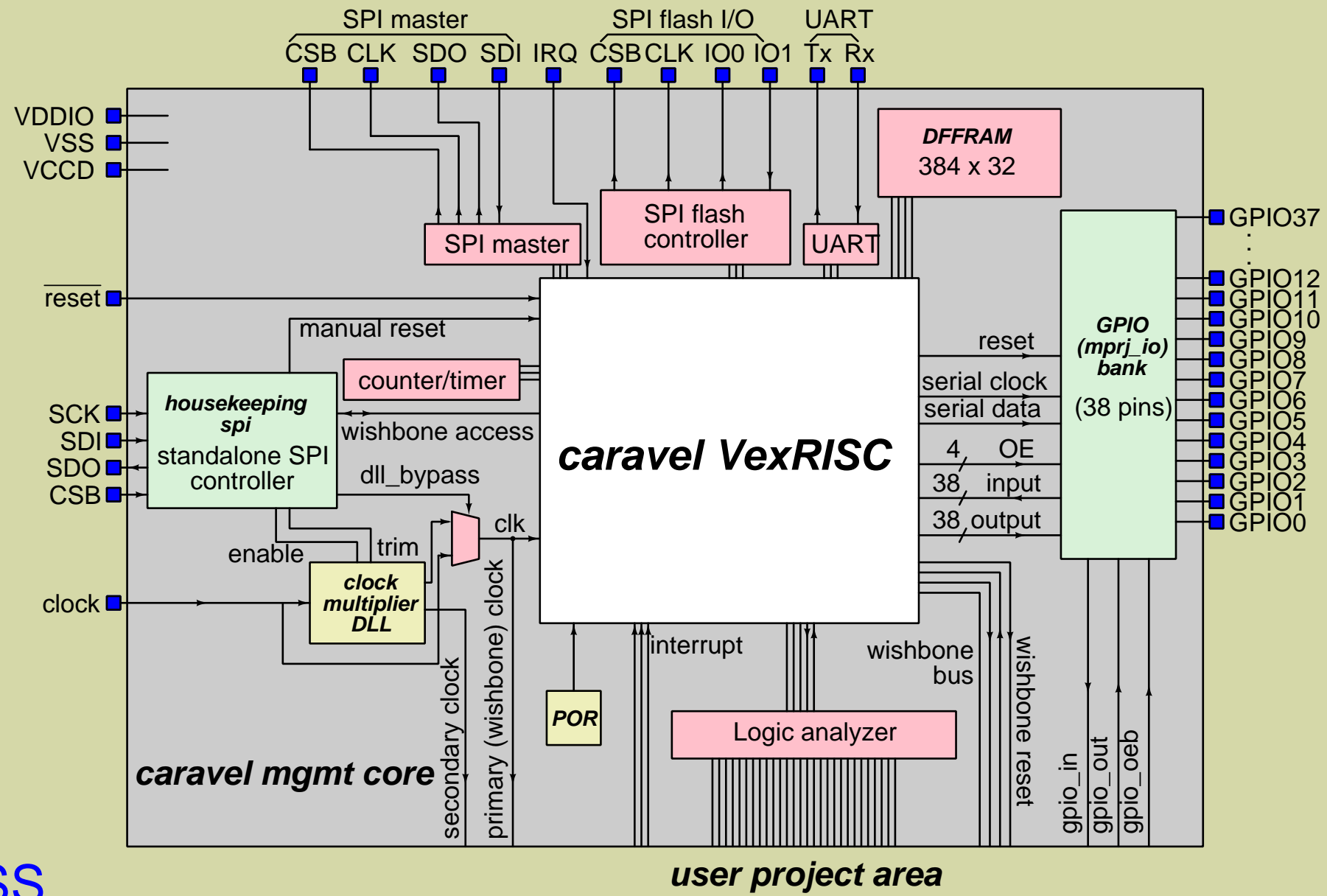
=

Completed chip

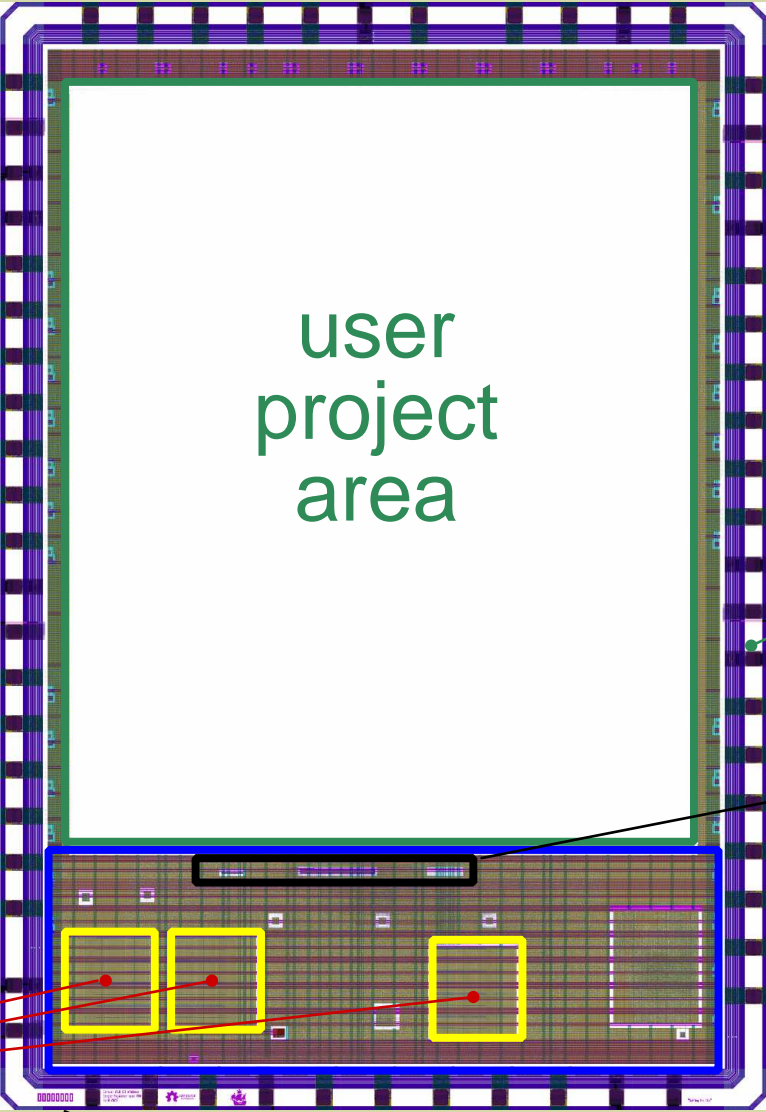


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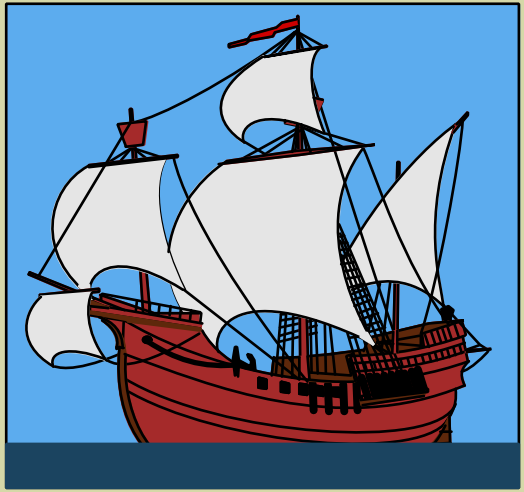
Caravel microcontroller ("management") part:



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“Caravel” user project harness
3.6 × 5.2 mm



storage areas
(DFFRAM)

fixed padframe

interface

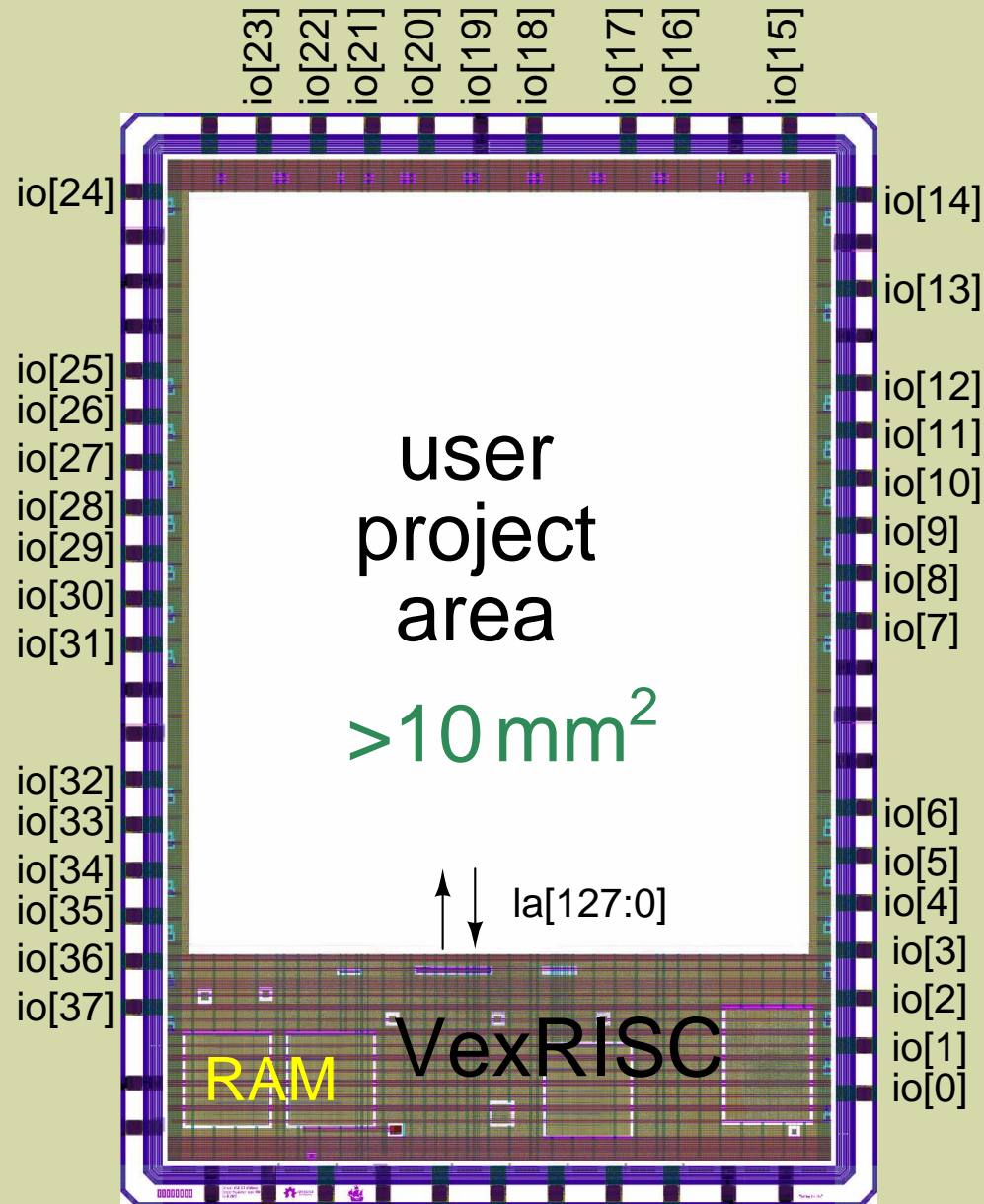
management area
(VexRISC)

user project ID marker

UNIC-CASS

August 21, 2024

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GPIO pins connect the user project to the outside world.

Internal “logic analyzer” connects the user project to the microcontroller.

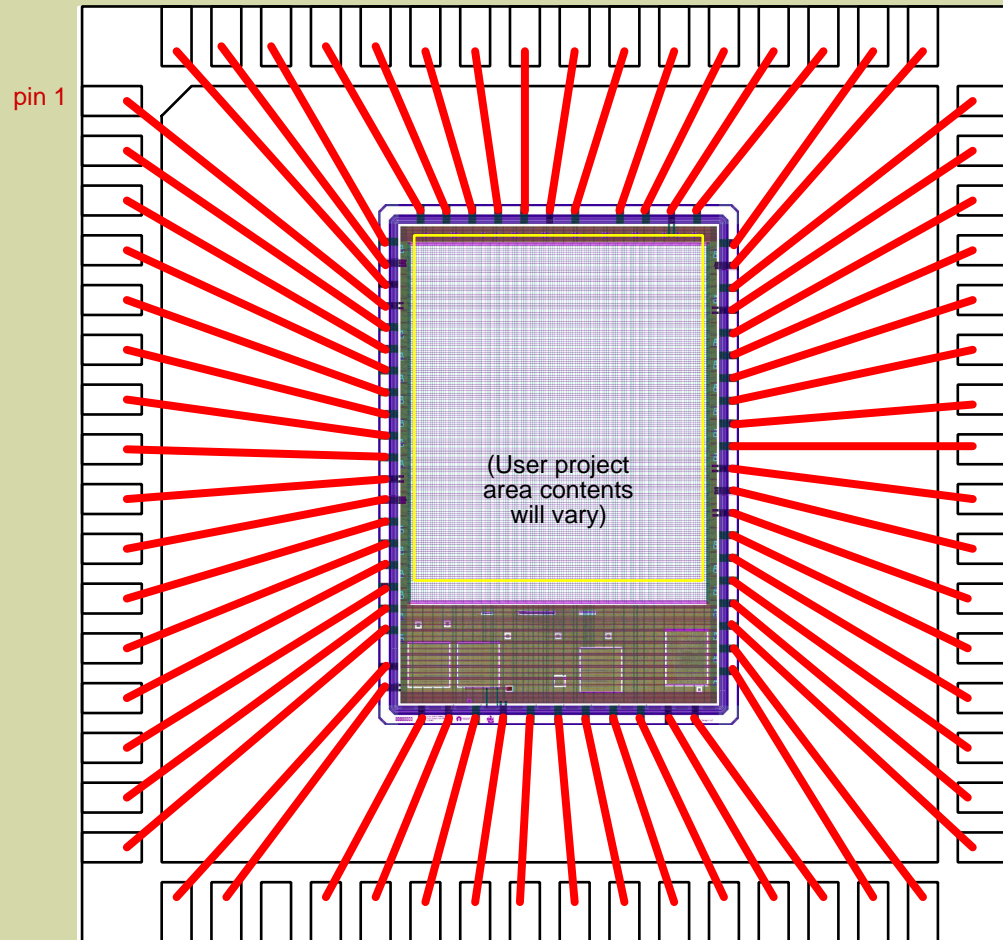
38 pins GPIO

8 pins for microcontroller

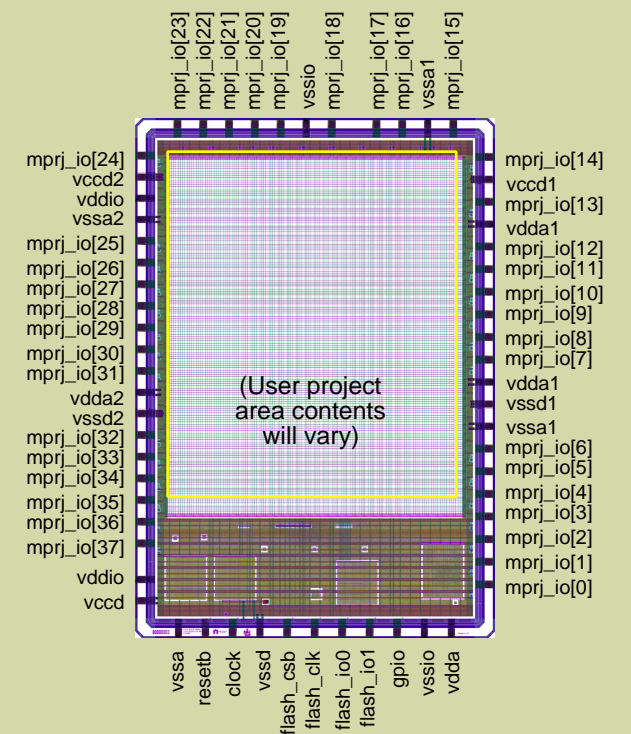
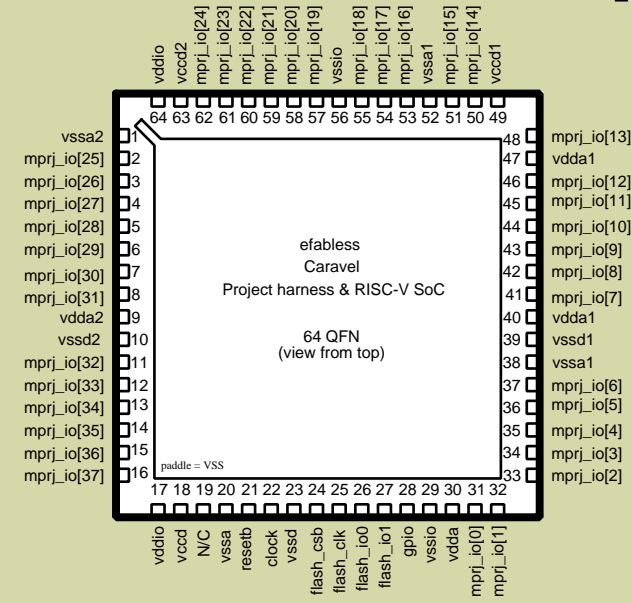
14 power/ground pins

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efabless "caravel" project harness 64-pin QFN package version
 February 8, 2023 Revision 1
 (Updated for Caravel version v3)

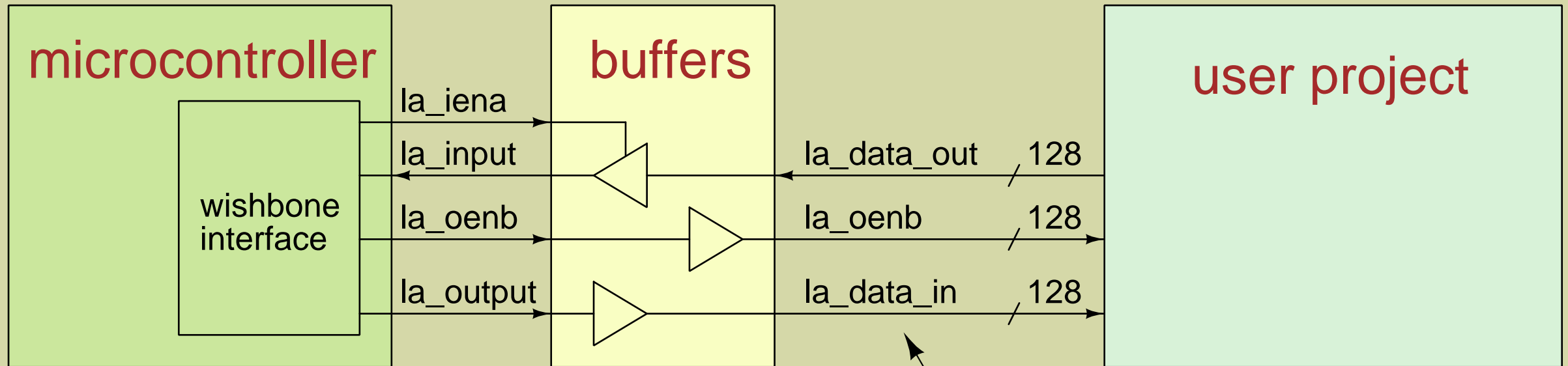


package size = 9 mm x 9 mm
 paddle size = 7.63 mm
 pin pitch = 0.5 mm
 Caravel padframe dimensions = 3.588 mm x 5.188 mm
 Caravel die dimensions = 3.60 mm x 5.20 mm



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“Logic Analyzer”



In program:

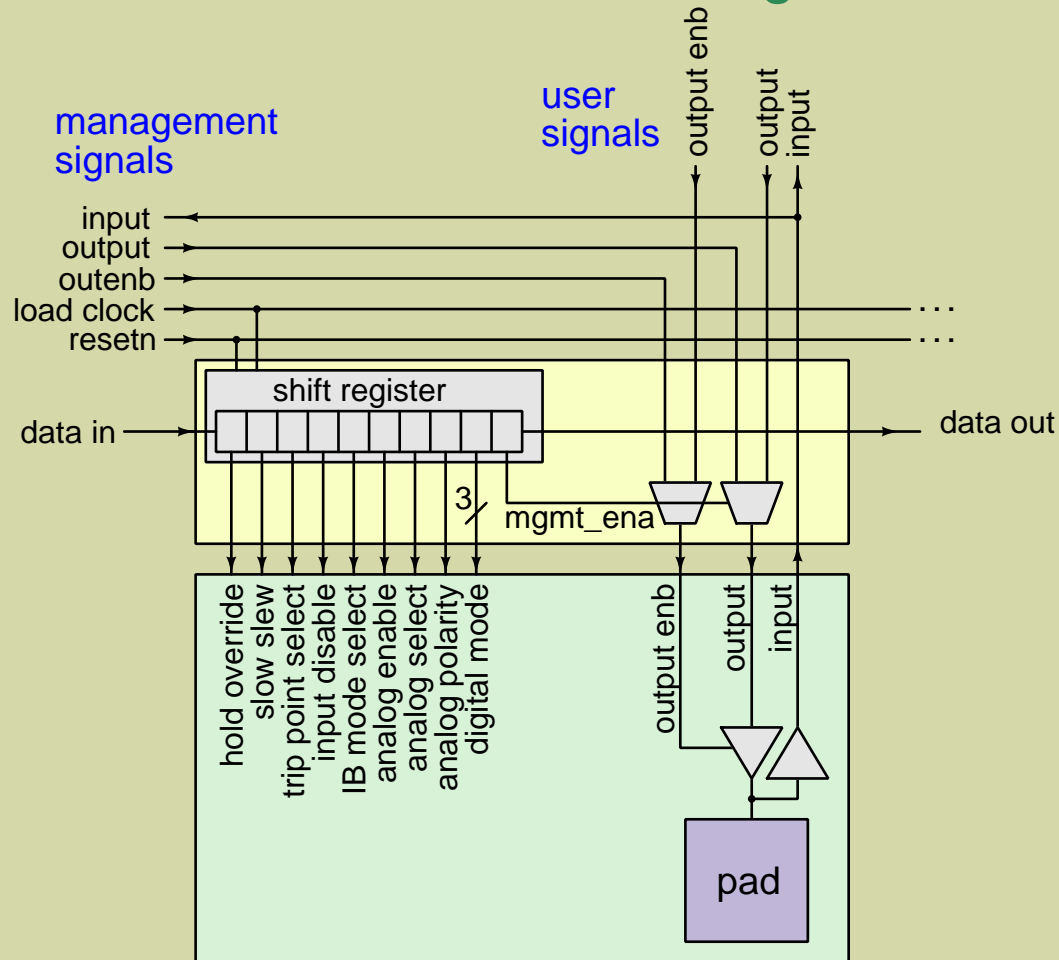
```
reg_la0_data ... reg_la3_data  
reg_la0_data_in ... reg_la3_data_in  
reg_la0_oenb ... reg_la3_oenb  
reg_la0_iena ... reg_la3_iena
```

(user_project_wrapper pins)

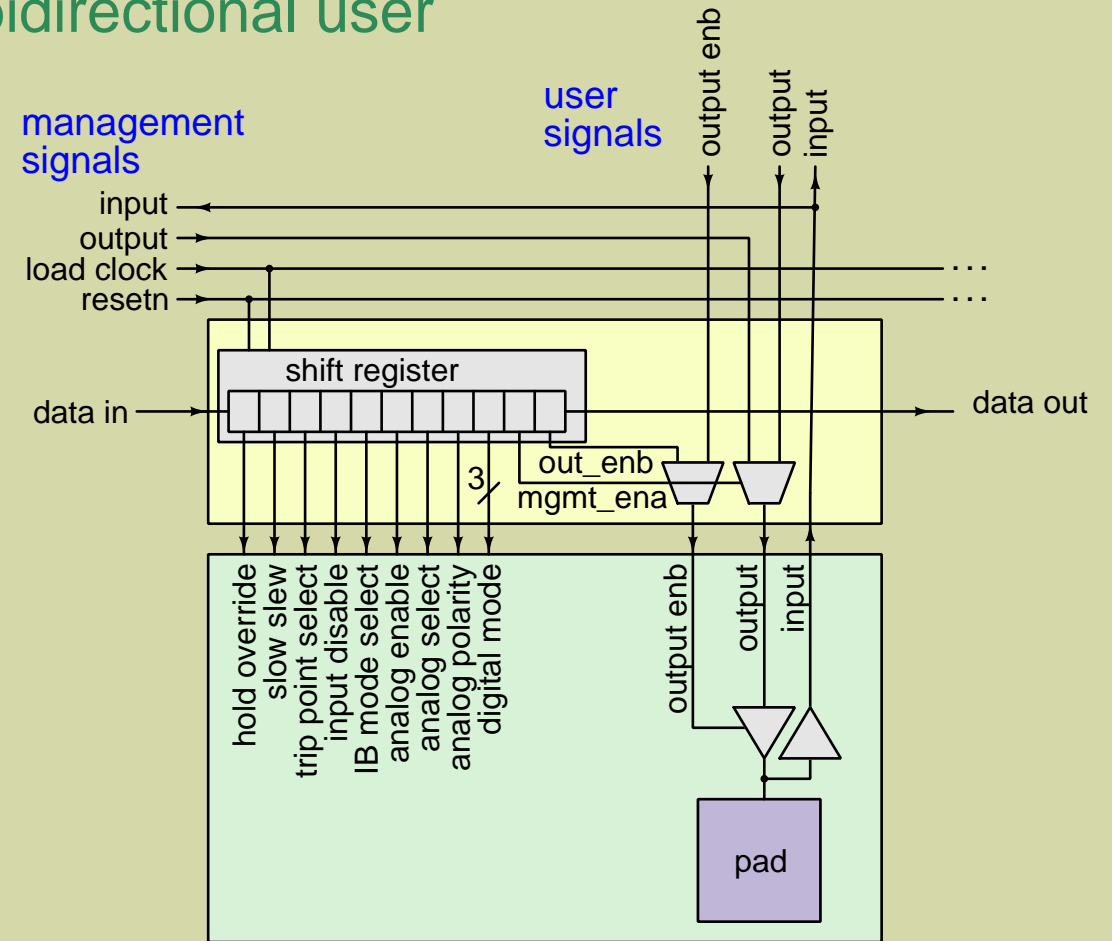
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General-Purpose I/O (GPIO)

Full bidirectional user/management



Management input or output, Full bidirectional user



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Additional digital logic functions available to the user project:

- 3 user project interrupts to the microcontroller
- 32-bit up/down, one-shot/continuous counter/timer
- Wishbone interface between microcontroller and user project
- Additional programmable clock input to user project
- Pass-through programming of SPI flash

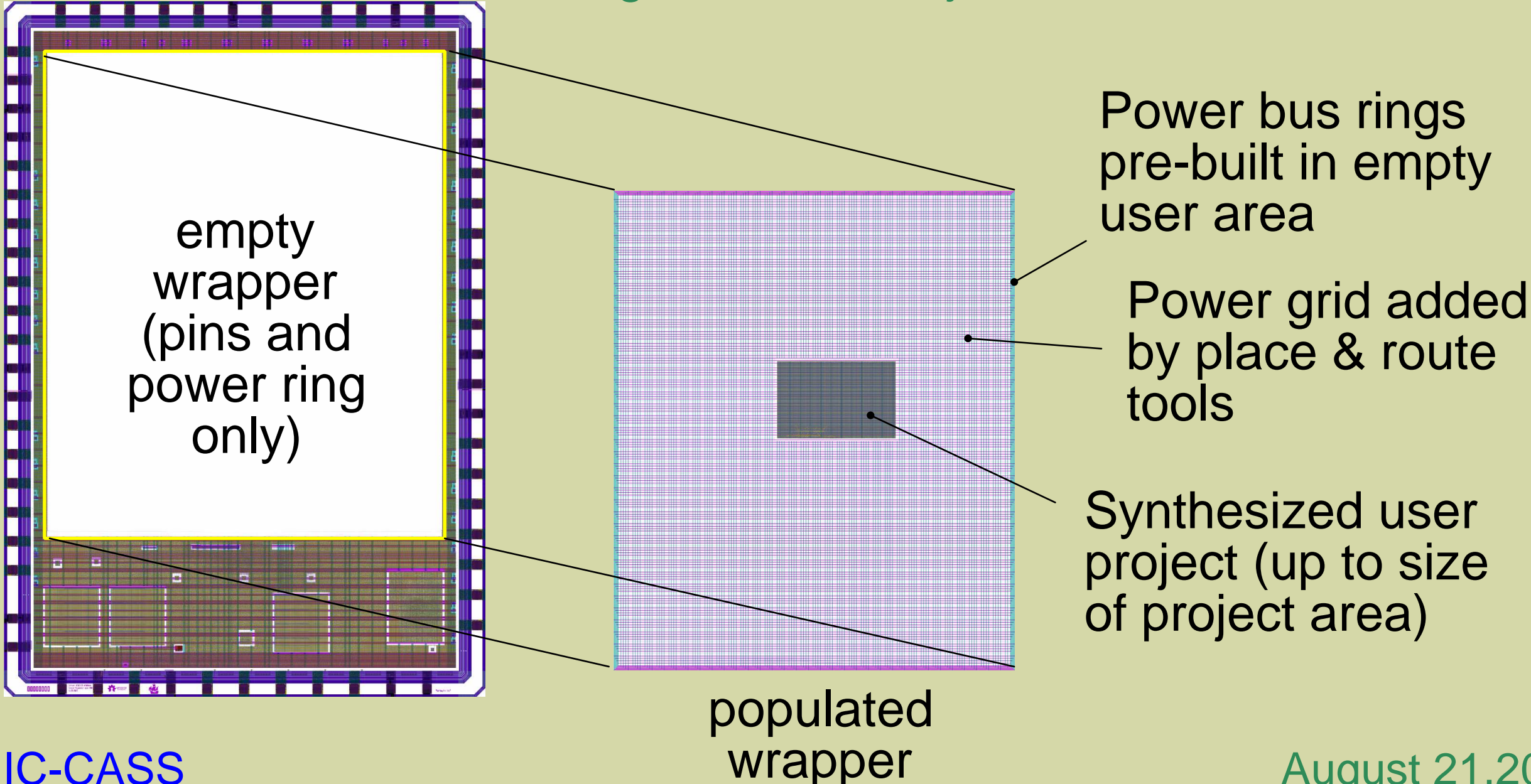
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Additional on-chip resources:

- Power-on-reset:
 - Power supply monitoring w/50ms startup delay
- Digital locked loop:
 - Programmable delay ring oscillator
 - Locks to external clock
 - 60 to 120 MHz system clock
 - Clock bypass mode

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Building the User Project



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Building the User Project

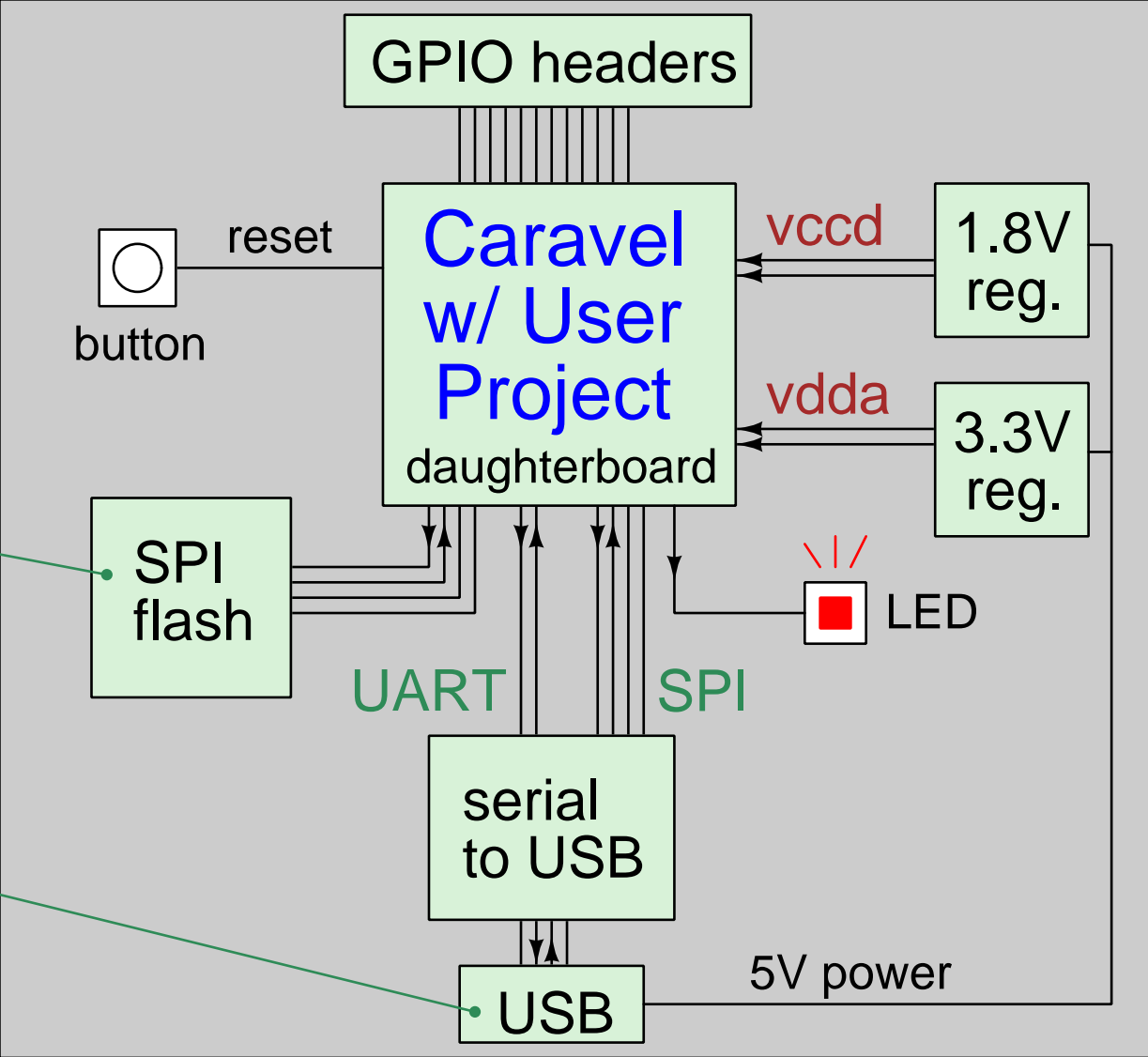
Starting the user project (digital design flow):

- Clone or fork: https://github.com/efabless/caravel_user_project
- Add verilog source for project
- Follow instructions for synthesis, place, route, assembly, verification
- Simple “make” targets for generating layout using **OpenLane**
- Analog projects: clone or fork
https://github.com/efabless/caravel_user_project_analog

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Development Board

Clone: https://github.com/efabless/caravel_board



Program to run on the RISC-V processor goes here

Communication with host computer via python scripts

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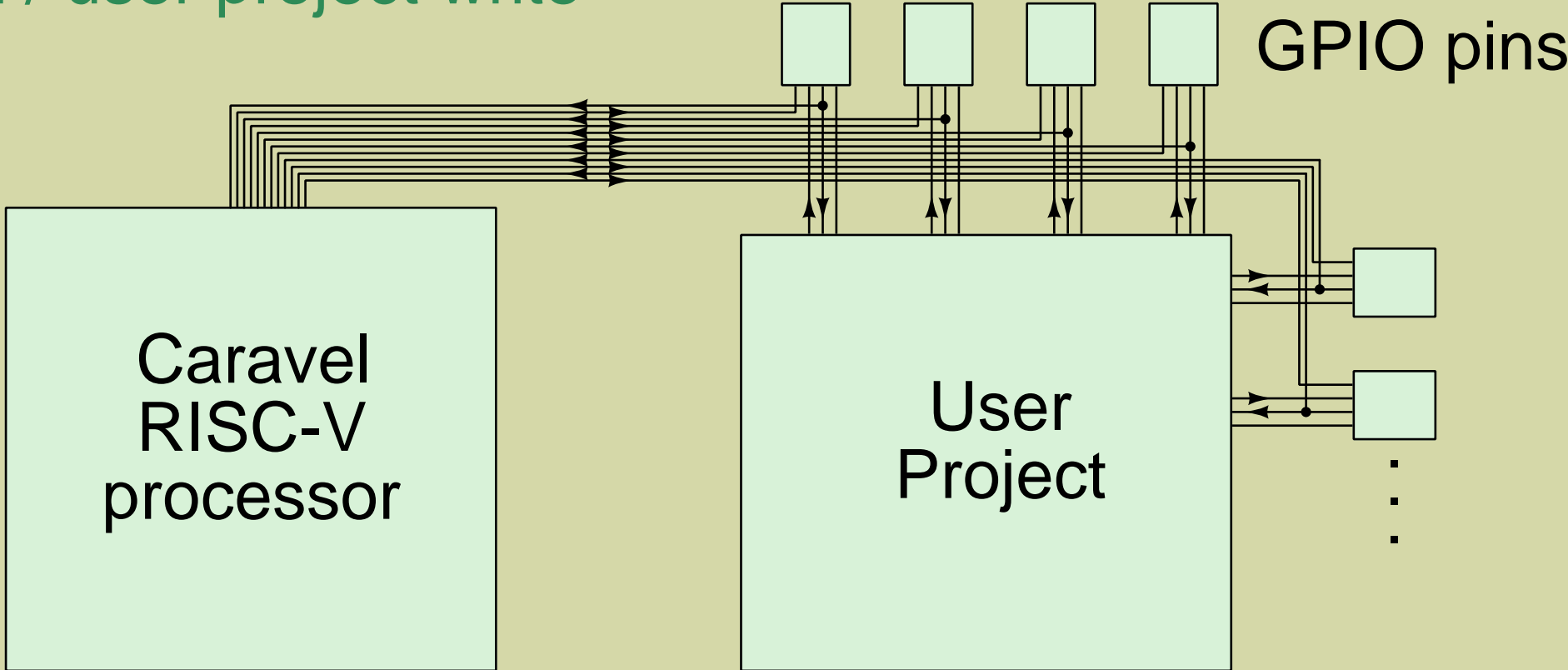
Typical project power-up sequence:

- Development board powers up microcontroller
- Power-on-reset circuit enables microcontroller
- Microcontroller runs program from SPI flash
 - Program (optionally) configures GPIO for user project
 - Program (optionally) resets user project
 - Program (optionally) controls/monitors user project

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Processor driving user project through pins

Pads operate with processor write / user project read, or processor read / user project write



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Validating the User Project

Simulation

Using open-source simulator “iverilog”

Simulate RTL and gate level

Top level modules simulate entire board-level system

LVS

Using open-source tool “netgen”

Part of OpenLane “make” scripts—fully automated

Pre-check

Run as local script and by efabless for tape-in

Metadata checks

DRC checks

Layer density checks

XOR check

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Alternatives to the Caravel harness design flow:

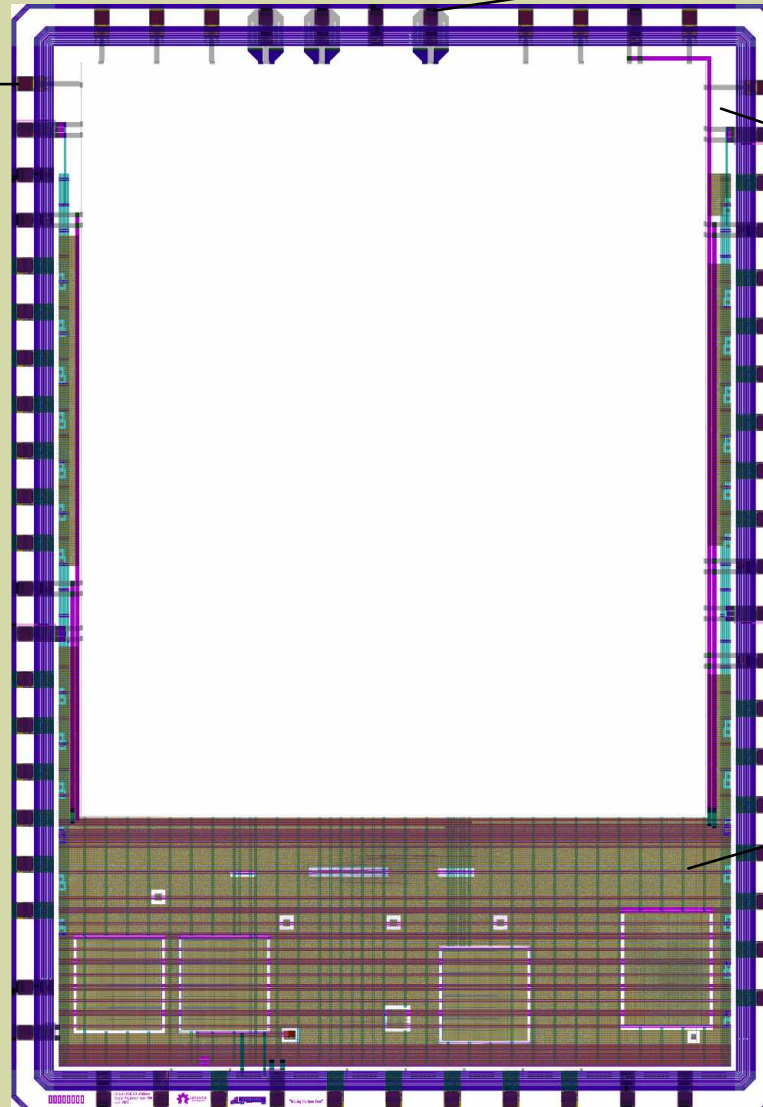
1. Caravan

Bare pads for analog signals (up to ~2GHz)

High current capacity pads

No digital under analog areas

Same RISC-V processor and other infrastructure

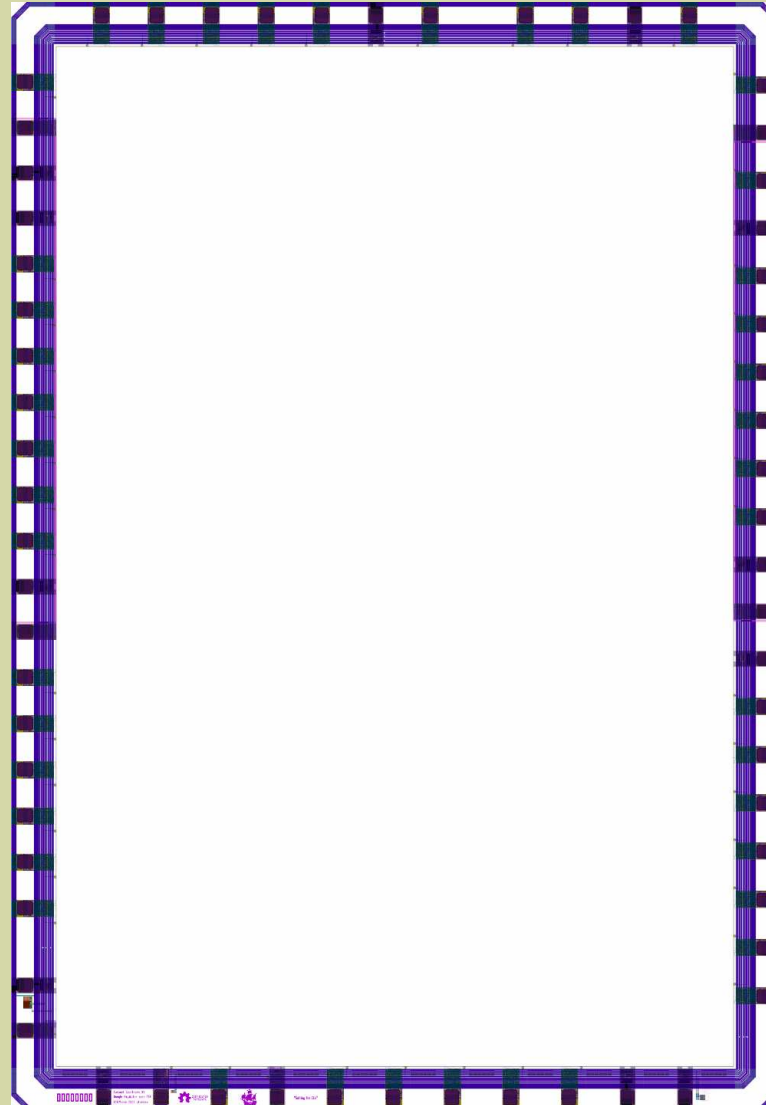


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Alternatives to the Caravel harness design flow:

2. Openframe

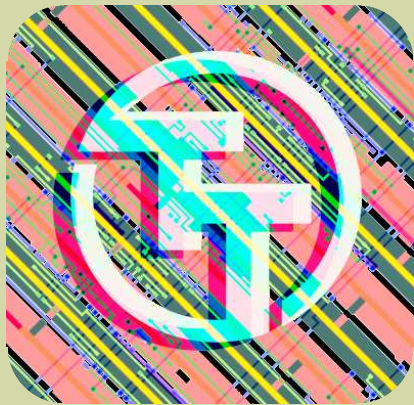
Just the Caravel
padframe, without
the processor.



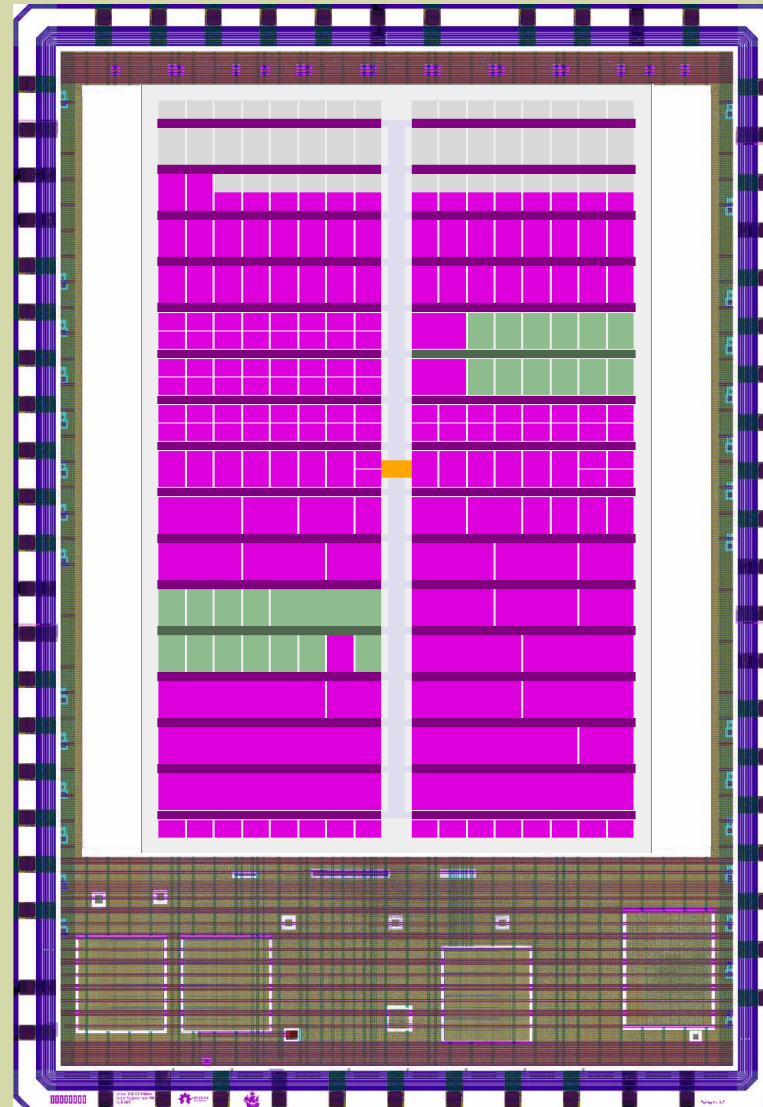
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Alternatives to the Caravel harness design flow:

3. TinyTapeout



tinytapeout.com

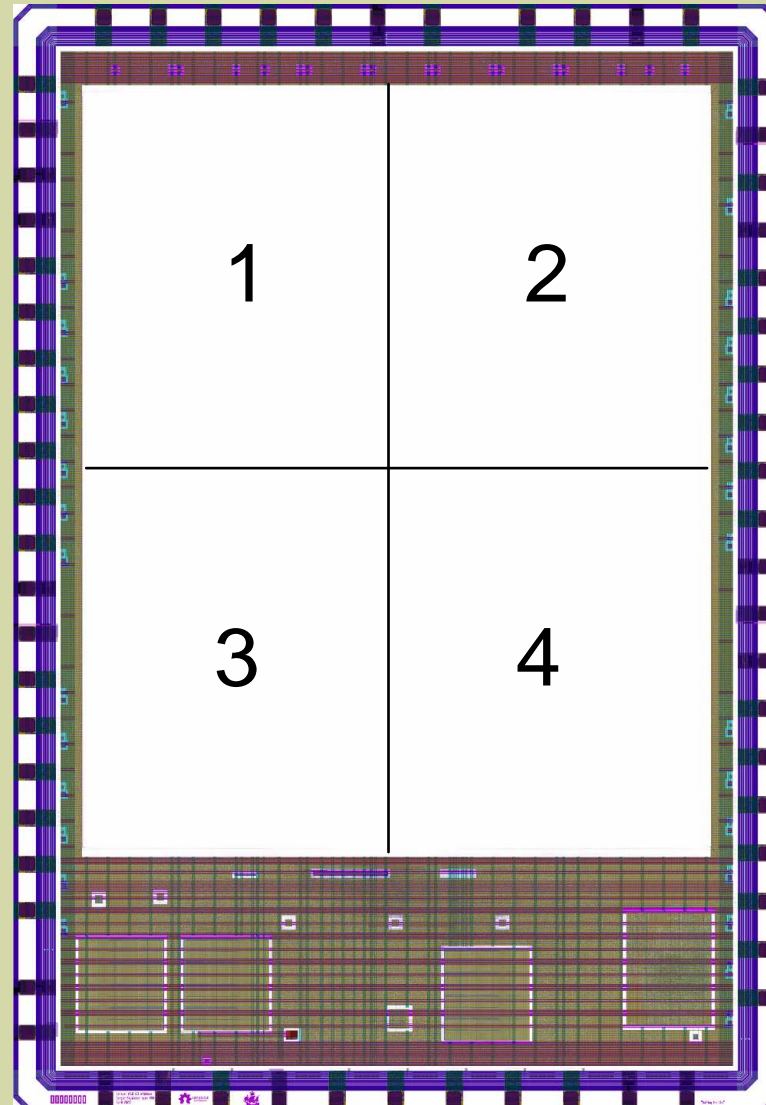


Best pricing for simple circuits for learning at \$150 per slot, \$300 with development board.

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Alternatives to the Caravel harness design flow:

4. chipIgnite mini



Shared space,
lower cost.

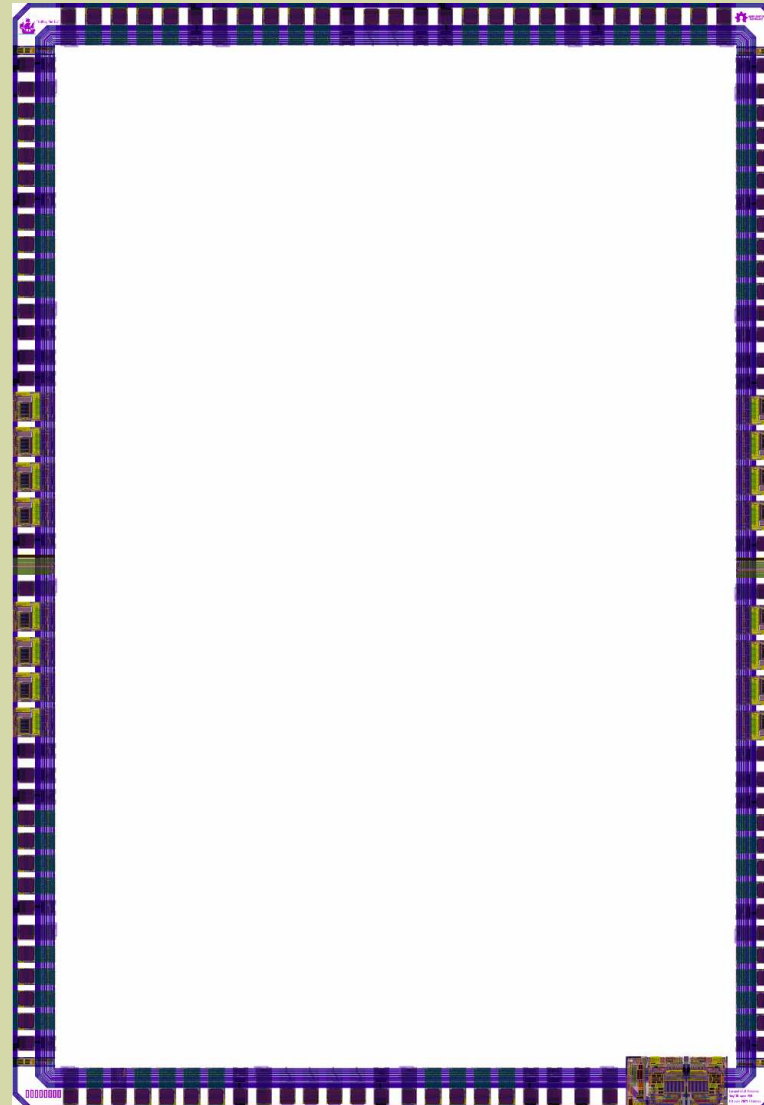
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Alternatives to the Caravel harness design flow:

5. Panamax (coming next year!)

128 pins total

9 banks of 8 GPIO
(72 GPIO total)



overvoltage-tolerant pads

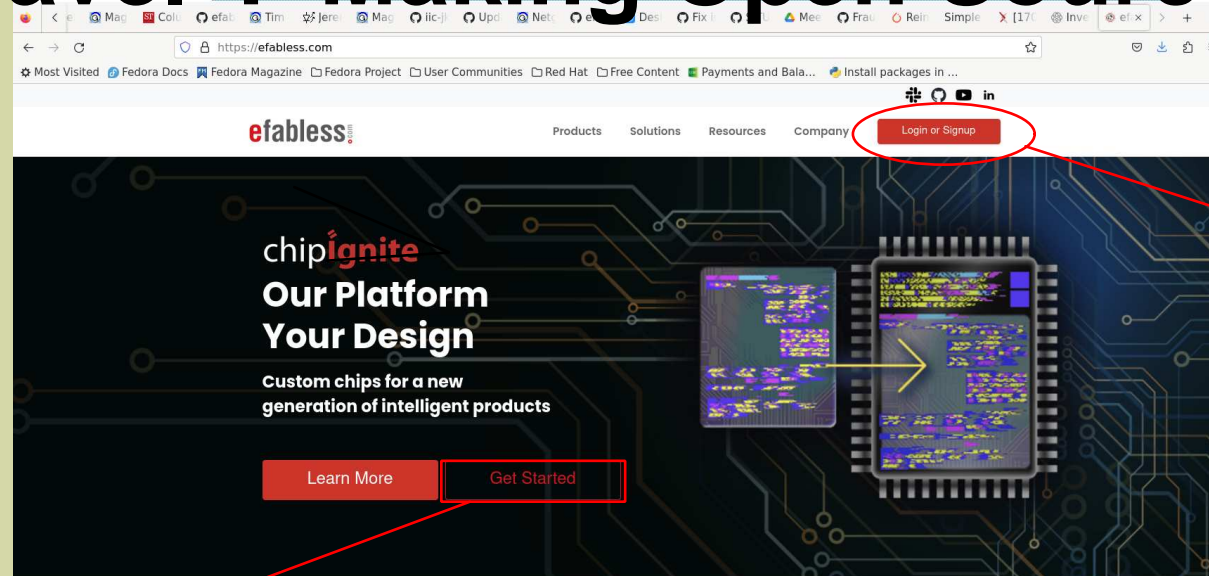
differential GPIO pad

analog pads

reference voltage generators


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Efabless front page




Register here

Instructions




chipignite Mini - Only \$3,500
Power your ASIC designs with affordable chipignite Mini

[Learn More](#)



chipignite Shuttle
Submit your project to chipignite and turn your ideas into reality!

[Learn More](#)



New Efabless Marketplace
Free & Commercial IP available now with other tech resources

[Learn More](#)

Who Are We?

Empowering innovation and democratizing chip design, we simplify the chip creation process, making it accessible and affordable for everyone.

chipignite is the Perfect Solution for...



Startups
Provides a rapid and affordable path to prototyping and low-volume production.



OEMs
Empowers the creation of intelligent products, even without design expertise and upfront investments.



Education
Hands-on chip design experience for students & attracting new talent.

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User dashboard

Instructional videos here

Your projects

Platform jobs (precheck, submit)

Links to Slack

Get on a shuttle!

Welcome, Tim

chipIgnite

Rapid IC Creation

Design Resources

- DESIGN HOW-TO: A guide for building and submitting a design
- GETTING STARTED: Check out our GitHub Repositories
- JOIN A SHUTTLE: How to create a project for chipIgnite
- COMMUNITY HELP: Connect or Join and get help from the community by

Recent Work

- chipalooza_projects_1 (Process: sky130A, Shuttle: CI 2404)
- Chaos-Automaton (Process: N/A, Shuttle: N/A)

Latest Job

ID	Name	Type	Project	Status
dfe86b6...	resubmit_for_tapeout_and_hope_for_the_best	tapeout	chipalooza_projects_1	failed

Active Shuttles (2)

- CI 2409** chipIgnite: Details Summary Start Project
Timeline: Tapeout: Sep 16, 2024 at 11:59 PT; Delivery: Feb 2025
Process: SKY130A Skywater 130nm
- CI 2411** chipIgnite: Details Summary Start Project
Timeline: Tapeout: Nov 11, 2024 at 11:59 PT; Delivery: Apr 2025
Process: SKY130A Skywater 130nm

Participants: 22 (New Users), 23 (Categories)

Projects: 0 (New Users), 0 (Categories)

Help

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Instructional
videos page

(from “Get Started”
link)

efabless

Products Solutions Resources Company Login or Signup

The following video series shows how to get started with chipignite including creating a repository, uploading your design and submitting your project for tapeout.

For help implementing a design in Caravel, checkout our video series [here](#) demonstrating how to integrate a basic digital design into the user project area within Caravel.

A complete list of video tutorials covering advanced topics will be coming soon.

Getting Started

Caravel Overview

This video provides an overview of the pre-built SoC chip used to implement custom chips with chipignite.

Setting Up Your Desktop

In this video you'll learn how to setup your environment in preparation for installing the design tool flow.

Creating a Repository

This video shows how to get started on a chipignite project by creating a repository for your design.

Cloning and Setup

This video shows you how to setup your chipignite project and tools on your own computer.

Step-by-step
instructions
for each part
of the design
and submission
process.

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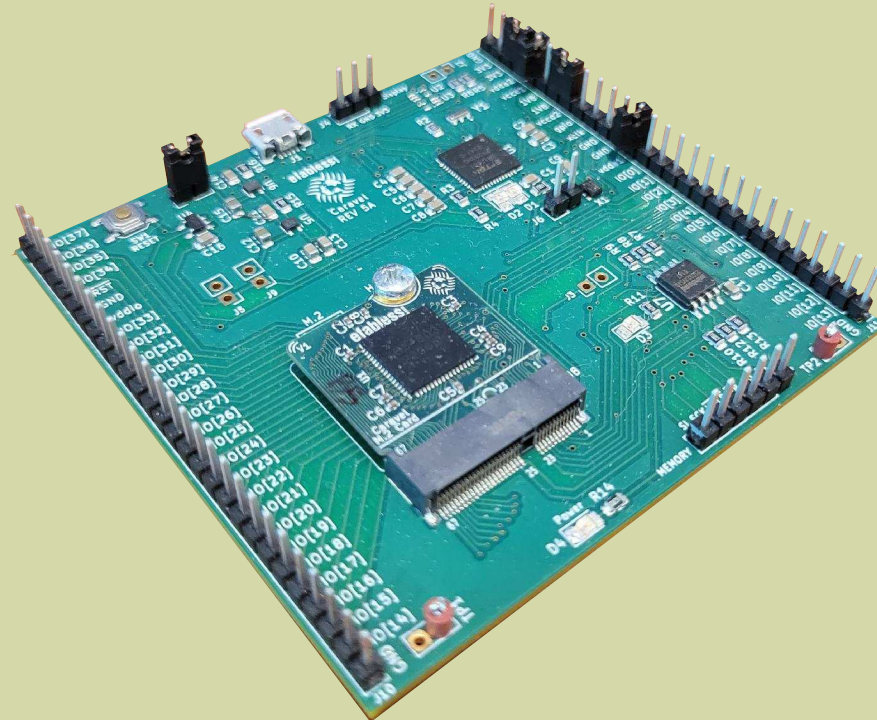
Submitting the User Project

- User registers with efabless at efabless.com
- Follow instructional videos
- Best written instructions at https://github.com/efabless/caravel_user_project
- Designer creates project on Efabless platform
- Project is populated from designer's git repository
- Designer submits request to manufacture
- User project is assembled with the caravel chip
- Designer gets report from pre-checks (DRC/density/XOR)

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Chip's in the Mail!

- Designer receives assembled development board with their project on it.
- Board has a USB port for power and communications
- Python scripts available for programming the SPI flash
- Hex file(s) from simulation validation can be downloaded and run



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Showcase page:

Silicon Showcase

Bandgap Voltage Reference

John Kustin made this bandgap circuit as part of his graduate training. The experience is what made him decide to do a PhD in the field. It was taped out on chipignite and he brought it up and tested it. He used xschem for schematic and magic for layout. The bandgap achieves a TC of -3.6 PPM/C.

Designer: John Kustin

[GitHub](#) | [Layout](#)



About the Author:

John Kustin entered the open-source silicon ecosystem during his Junior year at Stanford through Professor Priyanka Raina's EE272B 10-week tapeout class. His open-source bandgap circuit in SkyWater 130nm won his department's Student Design Project Award. After graduating with a BS in Electrical Engineering in June, 2022, he joined the University of Michigan to pursue a PhD in EE. John is interested in training the next generation of IC designers and democratizing IC design.

Riscduino

Riscduino is a single 32-bit RISC-V-based SoC design that is pin-compatible with the Arduino platform and targeted for the Efabless Shuttle program. This project uses only open-source toolsets for simulation, synthesis, and backend tools. The SoC flow follows the OpenLane methodology, and the SoC environment is compatible with the eFabless/Caravel methodology.

Designer: Dinesh Annaya

[GitHub](#) | [Layout](#)



About the Author

Dinesh Annaya is an ardent Open-Source EDA enthusiast and an expert user of OpenROAD™ and OpenLane. He developed a baseline RISCduino SoC, a single, 32 bit RISC-V based controller compatible with the Arduino platform. He has submitted over 15 designs on Open MPW shuttles on sky130- <https://github.com/dineshannaya/riscduino>. During the course of his design journey, he successively improved the design architecture for better performance, and enhanced functionality. His main motivation for the use of Open-Source EDA tools is to gauge the quality of results and potential for commercial use.

Turing-complete 8-bit MCU

A turing-complete 8-bit microprocessor based on a niche 70s architecture, successfully taped out on the first GF180 shuttle. It can easily run complex programs, such as rendering the Mandelbrot fractal, or powering a conference badge.

Designer: Luca "Tholin" H.

[GitHub](#) | [Layout](#)



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Marketplace (overhauled in 2024):

The screenshot shows the Efabless Marketplace website. At the top, there is a navigation bar with the Efabless logo, links for Products, Solutions, Resources, and Company, and a Login or Signup button. The main heading is "Marketplace". Below this, there is a paragraph of introductory text. Underneath the text are five category tiles, each with an image and a label: Reference Designs (highlighted with a red border), Semiconductor IP, Tools, Learning, and Services.

efabless Products Solutions Resources Company Login or Signup

Marketplace

For the first time, you can leverage the power of a growing community to bring your ideas to life faster. The Efabless Marketplace offers free and commercial resources that simplify and speed up custom chip design and fabrication. Access ready-made design components, templates, and complete designs in our [Reference Designs](#). Find excellent training resources on digital and analog/mixed-signal design in our [Learning](#) section. Use powerful design, simulation, and test [tools](#), including many free and open-source options. Explore new services from Efabless partners and other experts to elevate your projects.

Check back regularly for new entries and [contact us](#) if you are a designer or vendor looking to list your resources!

- Reference Designs**: Image showing a detailed chip layout with various colored blocks.
- Semiconductor IP**: Image showing a block diagram with components like ADC, DAC, I2C, and Power control.
- Tools**: Image showing a software interface with a waveform plot and a code editor.
- Learning**: Image showing a document titled "Complete & Path from" with a flowchart and text describing the design process.
- Services**: Image showing a physical circuit board with various components.

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Marketplace → Reference Designs:

The screenshot displays the Efabless Marketplace Reference Designs page. At the top, there is a search bar with the text "Enter your search term here." and a search icon. To the right of the search bar, it says "11 results" and a filter icon. Below the search bar, there is a grid of 12 reference design cards. Each card features a thumbnail image of a chip layout, a title, a subtitle, and a "Free" button. The cards are arranged in three rows and four columns. The first row contains: "ANALOG USER PROJECT" (Efabless, Silicon Services, Free), "CARAVAN" (Efabless, Silicon Services, Free), "CARAVEL" (Efabless, Silicon Services, Free), and "CARAVEL ANALOG PROJECT" (Efabless, Silicon Services, Free). The second row contains: "CARAVEL MINI" (Efabless, Silicon Services, Free), "CARAVEL USER PROJECT" (Efabless, Silicon Services, Free), "CLEAR" (Efabless, Silicon Services, Free), and "OPENFRAME" (Efabless, Silicon Services, Free). The third row contains: "OPENFRAME EXAMPLE" (Efabless, Silicon Services, Free), "SRAM EXAMPLE" (Efabless, Static Random-Access Memory, Paid), and "USER PROJECT EXAMPLE" (Efabless, Silicon Services, Free). The "CARAVEL ANALOG PROJECT" card in the first row is highlighted with a red border.

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Marketplace→Reference Designs→Caravel Analog Project:

Caravel Analog Project

Overview

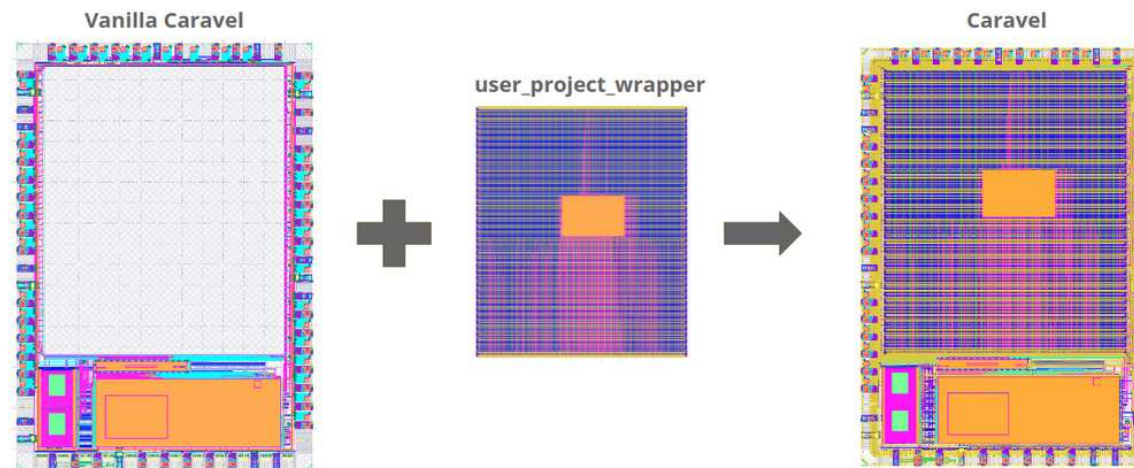
The Caravel Analog Project is a unique offering within the Caravel chip design framework that allows users to integrate their custom analog designs into a predefined space. This space, known as the user project area, is part of the overall Caravel chip and is specifically designated for user-defined logic. By utilizing the Caravel User Project, designers can incorporate their unique functionalities into a larger, professionally managed chip infrastructure, making it ideal for prototyping and small-scale production.

One of the key advantages of the Caravel Analog Project is its accessibility. It allows designers, regardless of their resources, to participate in silicon design and production. By providing a shared infrastructure and community support, Efabless lowers the barrier to entry, fostering innovation and collaboration in the field of chip design.

To ensure that all user designs are compliant with industry standards and compatible with the Caravel framework, Efabless has established a set of design rules. These rules are enforced through the `precheck` and `tapeout` flows, which are mandatory steps in the design process. The `precheck` flow validates the design against the specified rules, while the `tapeout` flow prepares the design for fabrication.

By integrating their custom designs into the Caravel User Project, users benefit from the robust features of the Caravel chip, including a RISC-V core, multiple I/O interfaces, and comprehensive debugging capabilities. This integration enables rapid development and testing of new ideas, significantly reducing time-to-market and development costs.

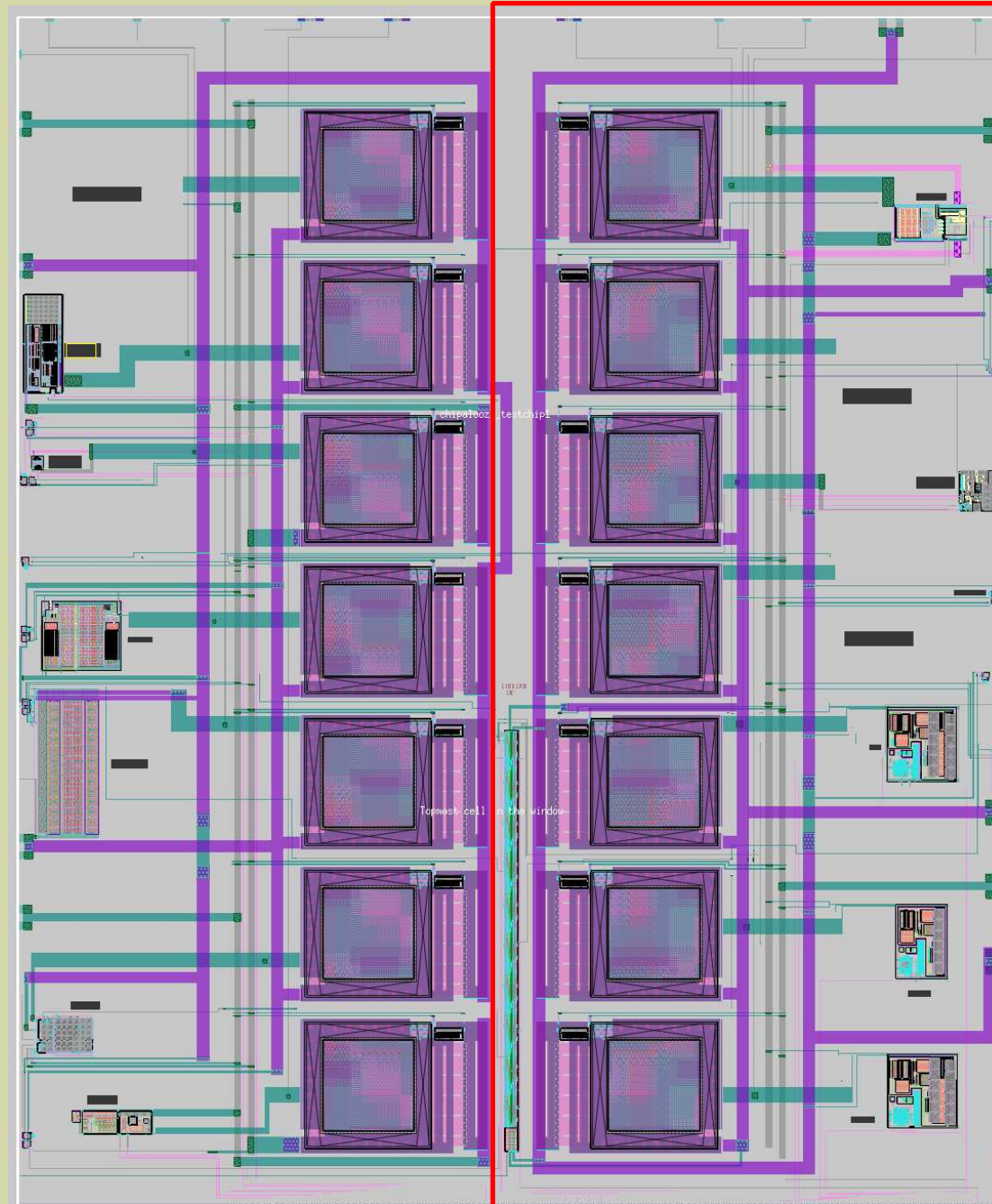
Analog designs can be integrated in either Caravel or Caravan, the only difference is that Caravan has bare pads, for experienced designers. Caravan should only be used if you are experienced, and the design is meant to be used in a controlled environment in a lab, it is only meant for prototyping. Otherwise, users designing analog projects are recommended to use Caravel.



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Analog multi-project integration

See:
[github.com/
RTimothyEdwards/
chipalooza_projects_1](https://github.com/RTimothyEdwards/chipalooza_projects_1)



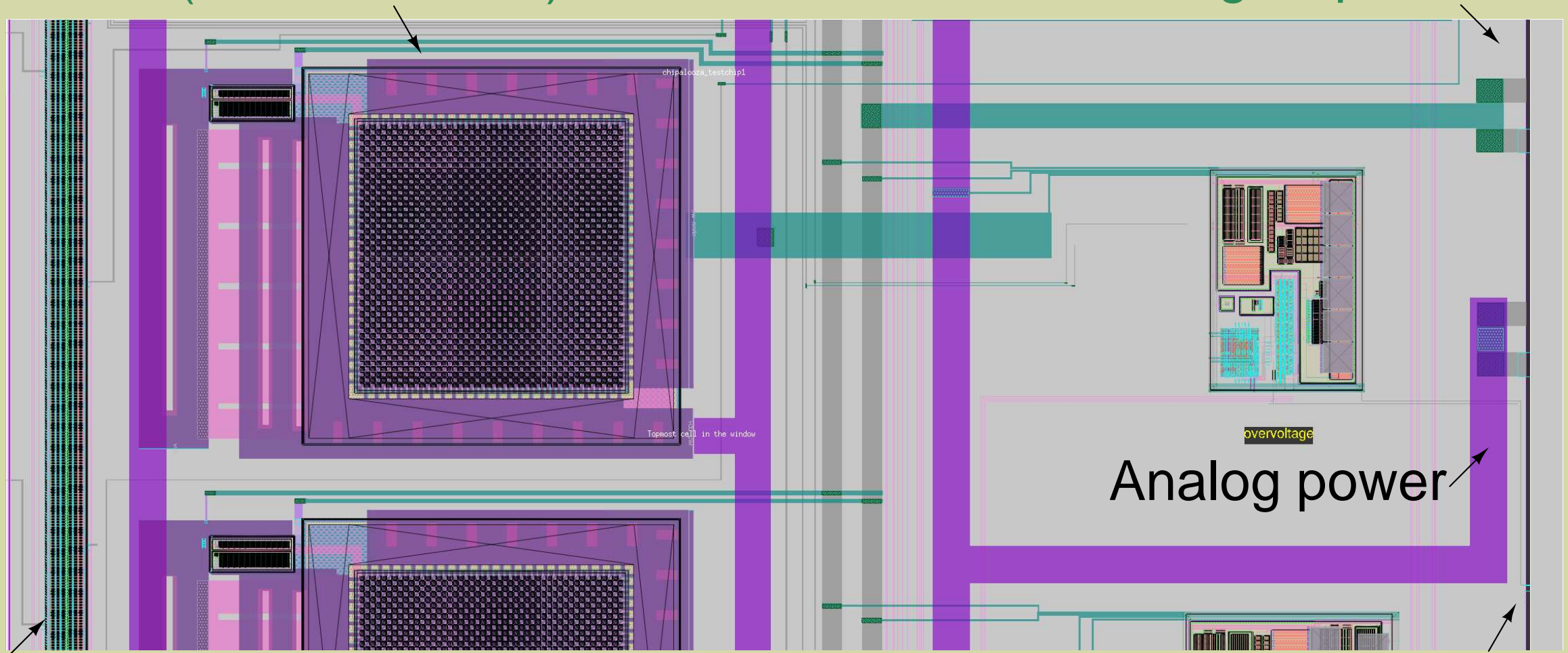
isosub
around
entire
project
area
excluding
deep-nwell
regions

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Analog multi-project integration

Power FET (Weston Braun)

Digital power



Bias current generator

Analog signal I/O

Analog power

overvoltage

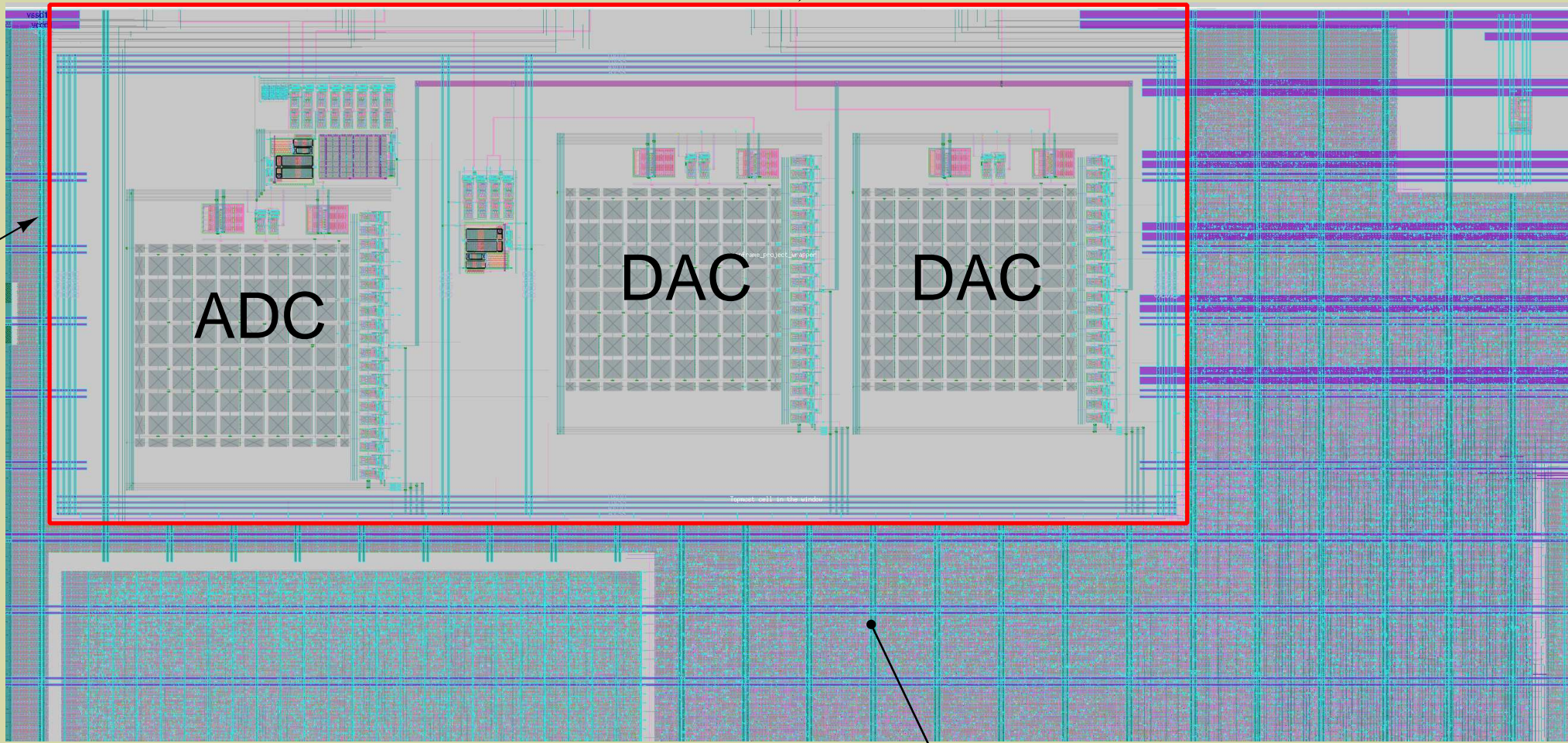
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Integrate analog as macro in a digital synthesis environment

Openframe wrapper:

Analog signals abut frame, not routed by digital router

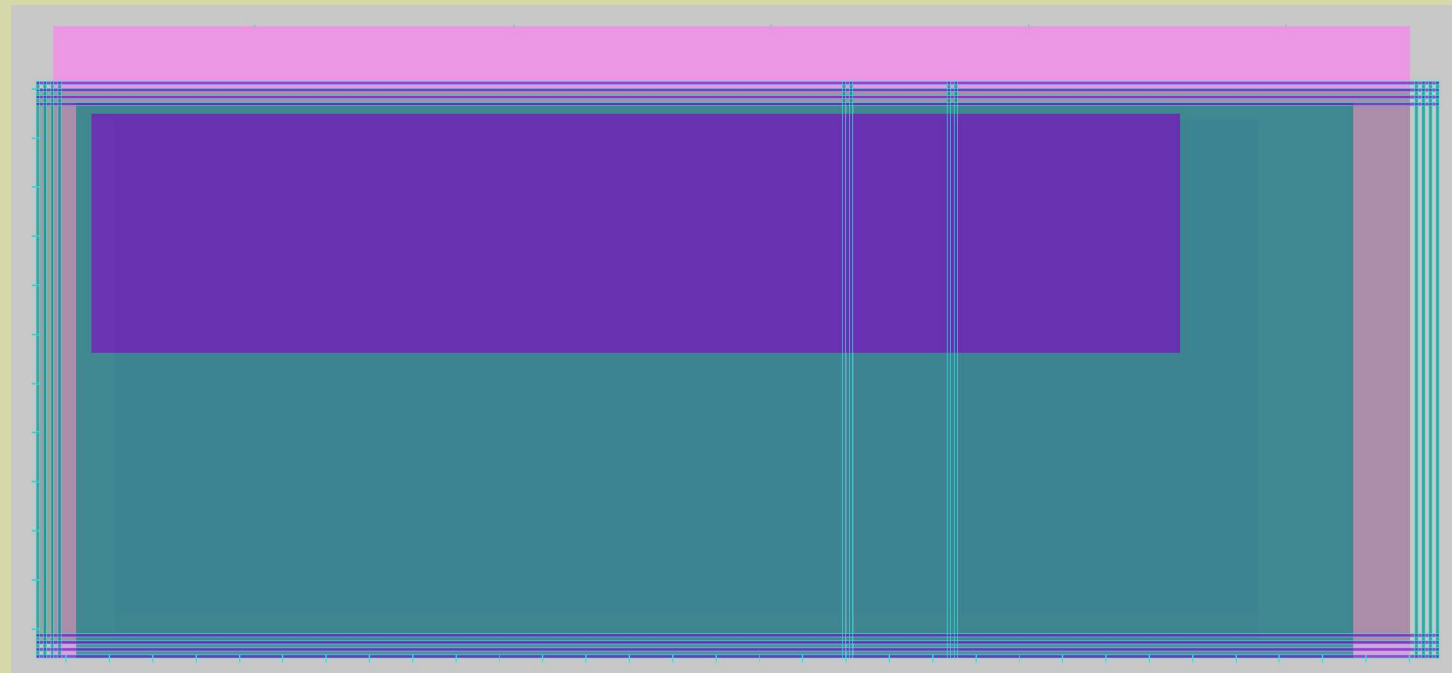
Analog macro



Digital core

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Analog multi-project integration



Analog macro is a LEF file as seen by the digital place & route tools (openlane)

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Thank you for listening!

Thank you for participating!

Keep it open source!