Vivek De

Intel Corportation, USA

vivek.de@intel.com

Biography

Vivek De is an Intel Fellow and Director of Circuit Technology Research in Intel Labs. He is responsible for providing strategic technical directions for long term research in future circuit technologies and leading energy efficiency research across the hardware stack. He has 295 publications in refereed international conferences and journals with a citation H-index of 79, and 227 patents issued with 32 more patents filed (pending). He received an Intel Achievement Award for his contributions to an integrated voltage regulator technology. He is the recipient of the 2019 IEEE Circuits and System Society (CASS) Charles A. Desoer Technical Achievement Award for “pioneering contributions to leading-edge performance and energy-efficient microprocessors & many-core system-on-chip (SoC) designs” and the 2020 IEEE Solid-State Circuits Society (SSCS) Industry Impact Award for “seminal impact and distinctive contributions to the field of solid-state circuits and the integrated circuits industry”. He received a Best Paper Award at the 1996 IEEE International ASIC Conference, and nominations for Best Paper Awards at the 2007 IEEE/ACM Design Automation Conference (DAC) and 2008 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). He also co-authored a paper nominated for the Best Student Paper Award at the 2017 IEEE International Electron Devices Meeting (IEDM). One of his publications was recognized in the 2013 IEEE/ACM Design Automation Conference (DAC) as one of the "Top 10 Cited Papers in 50 Years of DAC". Another one of his publications received the “Most Frequently Cited Paper Award” in the IEEE Symposium on VLSI Circuits at its 30th Anniversary in 2017. He received the 2017 Distinguished Alumnus Award from the Indian Institute of Technology (IIT) Madras. He received a B.Tech from IIT Madras, India, a MS from Duke University, Durham, North Carolina, and a PhD from Rensselaer Polytechnic Institute, Troy, New York, all in Electrical Engineering. He is a Fellow of the IEEE.

Lecture 1: Variation-Tolerant & Error-Resilient Many-Core SoCs with Fine-Grain Power Management

Many-core system-on-chip (SoC) architecture & design challenges & opportunities spanning edge devices to cloud computing systems in scaled CMOS process are presented. Key techniques for robust and variation-tolerant logic, embedded memory arrays and on-die interconnect fabrics are discussed. Fine-grain multi-voltage design and power management techniques, featuring integrated voltage regulators for wide dynamic voltage-frequency operating range and flexible platform power control across multi-threaded high-throughput near-threshold voltage (NTV) to single-threaded burst performance modes, are elucidated. Smart variation-aware workload mapping, runtime self-adaptation and error detection & recovery schemes to mitigate impacts of process-voltage-temperature (PVT) variations & aging, and achieve maximum performance under stringent thermal and energy constraints, are presented. Latest advances in design and process/package for realization of monolithic & heterogeneous 2D/3D-integrated compact, efficient, low supply noise, fine-grain, high-bandwidth & fast-response power converters & voltage regulators, essential for implementing intelligent system-

level power management and adaptation schemes across hardware and software, are also highlighted. Real SoC examples are used to demonstrate leading-edge practical systems.

Roberto Gómez-García

University of Alcalá, Spain

robert.gomez.garcia@ieee.org

Biography

Roberto Gómez-García (S'02-M'06-SM'11) was born in Madrid, Spain, in 1977. He received the degree in telecommunication engineering and the Ph.D. degree in electrical and electronic engineering from the Polytechnic University of Madrid, Madrid, in 2001 and 2006, respectively. Since 2006, he has been an Associate Professor with the Department of Signal Theory and Communications, University of Alcalá, Alcalá de Henares, Madrid. He has been, for several research stays, with the C2S2 Department, XLIM Research Institute, University of Limoges, Limoges, France, the Telecommunications Institute, University of Aveiro, Aveiro, Portugal, the U.S. Naval Research Laboratory, Microwave Technology Branch, Washington, DC, USA, and Purdue University, West Lafayette, IN, USA. His current research interests include the design of fixed/tunable high-frequency filters and multiplexers in planar, hybrid, and monolithic microwave-integrated circuit technologies, multifunction circuits and systems, and software-defined radio and radar architectures for telecommunications, remote sensing, and biomedical applications, in which he has authored/co-authored around 95 journal papers (75 in IEEE journals and 35 as first author) and 135 conference articles.

Dr. Gómez-García was the recipient of the “2016 IEEE Microwave Theory and Techniques Society (MTT-S) Outstanding Young Engineer Award” and is an “IEEE Circuits and Systems Society Distinguished Lecturer” for 2020-2021 He was an Adjunct Part-Time Professor during 2017-2019 at the University of Electronic Science and Technology of China, Chengdu, China, and Invited Visiting Professor during 2018/2019 at Gdansk University of Technology, Gdansk, Poland. He was an Associate Editor of the *IEEE Transactions on Microwave Theory and Techniques* from 2012 to 2016 and the *IEEE Transactions on Circuits and Systems-I: Regular Papers* from 2012 to 2015, a Senior Editor of the *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* from 2016 to 2017, and a Guest Editor of the 2013 and 2018 *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* “Special Issue on Advanced Circuits and Systems for CR/SDR Applications” and “Special Issue on Wireless Sensing Circuits and Systems for Healthcare and Biomedical Applications”, the *IET Microwaves, Antennas, and Propagation* 2013 “Special Issue on Advanced Tunable/Reconfigurable and Multi-Function RF/Microwave Filtering Devices”, and the *IEEE Microwave Magazine* 2014 “Special Issue on Recent Trends on RF/Microwave Tunable Filter Design" and 2019 “Special Issue on Wireless Sensors for Bio-Medical Applications”. He is currently an Associate Editor of the *IEEE Microwave and Wireless Components Letters, IEEE Journal of Electromagnetics, RF and Microwaves in Medicine and Biology*, the *IEEE Access*, the *IET Microwaves, Antennas, and Propagation*, and the *International Journal of Microwave and Wireless Technologies*. He is also a Reviewer for several IEEE, IET, EuMA, and Wiley journals. He serves as a member of the Technical Review Board for several IEEE and EuMA conferences. He is also a member of the IEEE MTT-S Filters (MTT-5), the IEEE MTT-S RF MEMS and Microwave Acoustics (MTT-6), the IEEE MTT-S Wireless Communications (MTT-23), the IEEE MTT-S Biological Effects and Medical Applications of RF and Microwave (MTT-28), and the IEEE CAS-S Analog Signal Processing Technical Committees.

Lecture 1: *"Reconfigure the World:* Adaptive-Transfer-Function and Multi-Band RF Filtering Devices for Emerging Wireless Systems*"*

Next-generation multi-purpose wireless-communications (e.g., 5G) and multi-mode remote-sensing systems demand highly-versatile RF front-ends capable of supporting them. As a result, a lot of interest has recently been detected in the development of advanced high-frequency electronics featuring increased levels of spectral adaptivity and multi-band operation. In particular, a considerable attention is being dedicated to the design of fully-reconfigurable single/multi-band RF bandpass filtering devices as key blocks to perform the adaptive-signal-band-selection process required by these systems. On the other hand, the ever-growing saturation of the radio-spectrum resource has led to critical electromagnetic-coexistence scenarios between the plurality of co-located RF systems that exploit it. In this case, the availability of fully-controllable multi-notch RF filters to suppress spectrally- and power-agile interferers is very desirable. The purpose of this seminar is to present an overview of recent contributions in the research field of RF filtering devices with highly-reconfigurable and multi-band transfer function. This includes both multi-passband and multi-bandstop components for multi-channel-selection and multi-interference-mitigation applications, respectively. Furthermore, their operational and design foundations, as well as a rich variety of experiment demonstrators in different bands and high-frequency technologies (e.g., planar, 3-D, lumped-element, acoustic-wave, and integrated ones), will be shown.

Lecture 2: *"Dīvide et īmpera?* Multi-Functional RF Filtering Components for Modern Wide-Band/Multi-Band Wireless RF Front-Ends*"*

Due to the necessity of lower-size/volume and optimized RF front ends for emerging wireless systems, the development of RF multi-functional components is acquiring a great interest. This means RF devices capable of carrying out multiple RF-processing actions in the same circuit. When compared to the classic RF chains based on the in-series cascade of independent mono-functional blocks (i.e., "*Dīvide et īmpera*" approach), benefits of the multi-functional philosophy are: (i) higher physical compactness, (ii) insertion-loss reduction due to the avoidance of inter-connecting RF interfaces between blocks, and (iii) enhanced performance with the multi-function co-design. Within this trend, special effort is being made to integrate the filtering functionality in other types of RF circuits, such as power dividers, amplifiers, or baluns. Thus, new families of multi-operation filtering devices are being conceived. The aim of this tutorial is to introduce main approaches to design multi-functional RF filtering circuits as an emerging research topic in the field of RF electronics. This includes the description of different types of multi-functional RF filtering components with static and adaptive behavior for ultra-wideband and multi-band applications. Their theoretical foundations and illustrative design examples are described. Besides, several experimental prototypes in different technologies and frequency bands are shown. Moreover, system-level implications derived from the use of multi-functional RF components in complete RF front-end chains are also discussed.

Georges G.E. Gielen

Ku Leuven, Belgium

gielen@kuleuven.be

Biography

Georges G.E. Gielen received the MSc and PhD degrees in Electrical Engineering from the Katholieke Universiteit Leuven (KU Leuven), Belgium, in 1986 and 1990, respectively. He is Full Professor in the MICAS research division at the Department of Electrical Engineering (ESAT). From August 2013 till July 2017 he was also appointed at KU Leuven as Vice-Rector for the Group of Sciences, Engineering and Technology, and he was also responsible for academic Human Resource Management. His research interests are in the design of analog and mixed-signal integrated circuits, and especially in analog and mixed-signal CAD tools and design automation. He is a frequently invited speaker/lecturer and coordinator/partner of several (industrial) research projects in this area, including several European projects. He has (co) authored 10 books and more than 600 papers in edited books, international journals and conference proceedings. He is Fellow of the IEEE since 2002, and received the IEEE CAS Mac Van Valkenburg career award in 2015. He is a 1997 Laureate of the Belgian Royal Academy of Sciences, Literature and Arts in the discipline of Engineering.

Lecture 1: Designing Analog Functions without Analog Circuits

The continuous progress of CMOS semiconductor technology fuels the technological revolution towards a smart world that immersively impacts our daily life, work and play. The Internet of Things, personalized healthcare monitoring, autonomous driving, industry 4.0, etc. are but a few examples. Sensors and sensor interfaces with intelligence in the edge play a key role in all of these. This presentation will focus on core challenges in the design of future electronic circuits for such applications, where cost, power and reliability are major issues besides raw performance. The key to achieve solutions with small area (cost) and low power is to design the analog functions in a highly digital manner. This will be illustrated with some practical design examples.

Lecture 2: Towards Unfailing Analog Circuits for Biomedical and Automotive Applications

Applications such as biomedical and automotive depend on extremely reliable electronics that are guaranteed to function correctly under all operating conditions and over the entire application lifetime. This seminar will focus on design techniques to make analog circuits smarter and unfailing. The approach taken heavily relies on digitally assisted architectures on the one hand, on detailed reliability modeling and real-time mitigation on the other hand, and on sophisticated test and DfT approaches for the detection of defective ICs before rollout. The lecture will explore the boundaries for the design of ultra-reliable analog circuits.

Minkyu Je

KAIST, South Korea

mkje@kaist.ac.kr

Biography

Minkyu Je received the M.S. and Ph.D. degrees, both in Electrical Engineering and Computer Science, from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1998 and 2003, respectively.

In 2003, he joined Samsung Electronics, Giheung, Korea, as a Senior Engineer and worked on multi-mode multi-band RF transceiver SoCs for GSM/GPRS/EDGE/WCDMA standards. From 2006 to 2013, he was with Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore. He worked as a Senior Research Engineer from 2006 to 2007, a Member of Technical Staff from 2008 to 2011, a Senior Scientist in 2012, and a Deputy Director in 2013. From 2011 to 2013, he led the Integrated Circuits and Systems Laboratory at IME as a Department Head. In IME, he led various projects developing low-power 3D accelerometer ASICs for high-end medical motion sensing applications, readout ASICs for nanowire biosensor arrays detecting DNA/RNA and protein biomarkers for point-of-care diagnostics, ultra-low-power sensor node SoCs for continuous real-time wireless health monitoring, and wireless implantable sensor ASICs for medical devices, as well as low-power radio SoCs and MEMS interface/control SoCs for consumer electronics and industrial applications. He was also a Program Director of NeuroDevices Program under A*STAR Science and Engineering Research Council (SERC) from 2011 to 2013, and an Adjunct Assistant Professor in the Department of Electrical and Computer Engineering at National University of Singapore (NUS) from 2010 to 2013. He was an Associate Professor in the Department of Information and Communication Engineering at Daegu Gyenogbuk Institute of Science and Technology (DGIST), Korea from 2014 to 2015. Since 2016, he has been an Associate Professor in the School of Electrical Engineering at Korea Advanced Institute of Science and Technology (KAIST), Korea.

His main research areas are advanced IC platform development including smart sensor interface ICs and ultra-low-power wireless communication ICs, as well as microsystem integration leveraging the advanced IC platform for emerging applications such as intelligent miniature biomedical devices, ubiquitous wireless sensor nodes, and future mobile devices. He is an author of 5 book chapters and has more than 290 peer-reviewed international conference and journal publications in the areas of sensor interface IC, wireless IC, biomedical microsystem, 3D IC, device modeling and nanoelectronics. He also has more than 50 patents issued or filed. He has served on the Technical Program Committee and Organizing Committee for various international conferences, symposiums and workshops including IEEE International Solid-State Circuits Conference (ISSCC), IEEE Asian Solid-State Circuits Conference (A-SSCC) and IEEE Symposium on VLSI Circuits (SOVC).

Lecture 1: Integrated Circuits and Microsystems for Emerging Biomedical Applications

Many factors, such as extended lifespan, prevailing obesity, and aging population are increasing the healthcare cost dramatically. Recent advances in semiconductor technologies, as well as innovations in IC design techniques, have led to microsystems with sensing and processing capabilities that can supplement, improve, or even entirely replace traditional diagnostic and therapeutic procedures. Integrated biomedical solutions based on IC technologies can offer remarkably effective ways of timely diagnosis, treatment, and management of diseases at a very low cost, never seen before.

In this talk, it will be presented how IC technologies and integrated microsystems enable emerging biomedical applications such as life-saving/changing miniature medical devices, surgical procedures with less invasiveness and morbidity, low-cost preventive healthcare solutions in daily life, effective chronic disease management, point-of-care diagnosis for early disease detection, high-throughput bio sequencing and screening for new discovery, and groundbreaking brain-machine interface from a deep understanding of human intelligence. It will also be shown that the vital role of the IC technology in biomedical microsystems is providing a seamless interface to various sensors and actuators, high-efficiency operation with various energy sources (especially, renewable ones), high-level integration and miniaturization, embedded intelligence, and connectivity.

Lecture 2: Integrated Circuits Interfacing with Neurons

Most of the neurological diseases are intractable ones and cause enormous economic and societal costs. It was recently found that the disorders in brain connectivity are the reasons for such conditions, calling for the methods to modulate the functional connectivity of the neuronal network effectively. On the other hand, there are intensive ongoing research efforts to demystify the structural and functional connectivity as well as the dynamics of neuron activity in the human brain, requiring the innovative tools that can enable such studies. In all these scenarios, the integrated circuits that can interface with neurons should play a key role.

In this talk, the requirements and recent advances in the development of neural interface circuits will be presented. As the key components of the bidirectional neural interface, the neural recording and stimulation circuits will be investigated. Also, the recent research works toward the development of concurrent bidirectional neural interface will be introduced together with the advanced circuit techniques invented for its realization. Such interface technology enables the modulation as well as the study of the human brain in a closed-loop manner eventually, which makes a vast difference from prior methods and approaches.

Kyuk-Jae Lee

Seoul National University, South Korea

hyukjae@snu.ac.kr

Biography

Hyuk-Jae Lee received the B.S. and M.S. degrees in Electronics Engineering from Seoul National University, Korea, in 1987 and 1989, respectively, and the Ph.D. degree in Electrical and Computer Engineering from Purdue University, West Lafayette, IN, in 1996. From 1998 to 2001, he worked at the Server and Workstation Chipset Division of Intel Corporation in Hillsboro, Oregon as a Senior Component Design Engineer. From 1996 to 1998, he was on the faculty of the Department of Computer Science of Louisiana Tech University at Ruston, Louisiana. In 2001, he joined the Department of Electrical and Computer Engineering at Seoul National University, Korea, where he is currently working as a Professor and the Department Chair. In 2002, Dr. Lee founded Mamurian Design, Inc., a fabless SoC design house for multimedia applications and served as an Acting CTO until 2012 to develop MPEG-4, H.264 and AMR multimedia processors. From 2013 to 2015, He served as the Director of System Semiconductor Program at the KEIT (Korea Evaluation Institute of Industrial Technology), in charge of managing the research fund from Korean Ministry of Industry, Trade, and Energy. From 2018, he has been serving as the Director of Strategic Industrial Collaboration Program between Seoul National University and Samsung Electronics Device Solution. He is currently a vice president of IEIE (Institute of Electronics and Information Engineers). His research interests are in the areas of computer architecture and SoC design for neural network processing and video applications. He has published more than 90 journal papers and 100 conference papers. He has been serving as an Associate Editor of IEEE Transactions on Circuits and Systems for Video Processing from 2015 and also as a CASS Distinguished Lecture from 2020. He was a guest editor of a special issue for Display Journal in 2015 and is currently a guest editor of a special issue of MDPI.

Lecture 1: Memory Access Optimization for Neural Network Processors

Recently, a number of neural network processors have been developed to efficiently process deep neural networks. Most these processors include a memory system with a large capacity of on-chip SRAMs as well as high-bandwidth off-chip DRAMs. In order to fully utilize the hardware resources of neural processors, efficient access of both on-chip SRAMs and off-chip DRAMs is essential. This tutorial presents traditional and state-of-art optimization techniques for memory access for neural network applications. State-of-art neural processors are introduced and common characteristics of the memory systems are explained. The optimization techniques for the data access of an on-chip SRAM are introduced. The scheduling, parallelization and data allocation of various deep learning algorithms are presented and the pros and cons of optimizations for a given memory system are explained. Additional data optimization for efficient access of an off-chip DRAM is explained in the next. To this end, the basic characteristics of a DRAM organization are introduced and then the data access scheduling for efficient DRAM access is explained. As the last subject of this tutorial, future memory systems are introduced.

Processing-in-Memory (PIM) and Approximate Memory (AM) architecture are briefly introduced and data optimizations for PIM and AM in deep neural processing are presented. A SCM (Storage Class Memory), a potential new memory hierarchy, is introduced and data access techniques for them are also presented.

Lecture 2: New Memory Architecture for Deep Learning Applications

Deep learning applications demand a large amount of data movement between processors and memory devices. To reduce the time and power consumption for data movement, extensive research has been carried out to develop new memory architecture suitable for deep learning. This talk introduces new trends of memory architecture for deep learning applications. Among them, Processing-near-Memory (PNM) and Approximate Memory (AM) architectures attract wide attention. PNM architecture is used to reduce data movement by placing computation near DRAM devices. On the other hand, AM architecture attempts to reduce the precision of deep learning data, and consequently, to reduce memory traffic. AM is especially suitable for deep learning applications of which accuracy may not be degraded significantly even with a loss of data precision. Recent developments in PNM and AM architectures are briefed and then data access optimizations for these memory architectures are explained. A proposal of a new memory architecture combining the two architectures is presented. The new memory architecture is simulated by modifying a GPU simulator and its effectiveness is presented with simulation results.

Gerald Sobelman

University of Minnesota

sobelman@umn.com

Biography

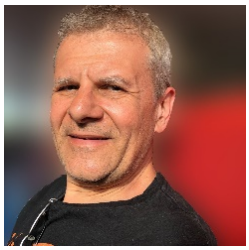
Gerald Sobelman is a Professor in the Department of Electrical and Computer Engineering at the University of Minnesota, and he has served as the Director of Graduate Studies for the Graduate Program in Computer Engineering at the University of Minnesota. He received a B.S. degree in physics from the University of California, Los Angeles, and M.S. and Ph.D. degrees in physics from Harvard University. He has been a postdoctoral researcher at The Rockefeller University, and he has held senior engineering positions at Sperry Corporation and Control Data Corporation.

Prof. Sobelman has previously served twice as a Distinguished Lecturer of the IEEE Circuits and Systems Society, during 2008–2009 and during 2013-2014. He has been a member of the technical program committees for several IEEE conferences. He was Chair of the Technical Committee on Circuits and Systems for Communications of the IEEE Circuits and Systems Society, and he has also served as an Associate Editor for IEEE Transactions on Circuits and Systems I and for IEEE Signal Processing Letters. In addition, he has chaired sessions at international conferences in the areas of communications and VLSI architectures.

Prof. Sobelman has presented short courses at a number of industrial and academic sites. He has authored or co-authored more than 150 technical papers and 1 book, and he holds 12 U.S. patents.

Lecture 1: Machine Learning and Optimization for Communications and Deep Networks

In recent years, many remarkable achievements have been made in the field of machine learning. While most of the initial successes were related to image, speech and language recognition, a recent important development has been the application of these techniques to other areas. In particular, communications systems can benefit from applying these techniques. For example, algorithms such as Monte Carlo Markov Chain and Monte Carlo Tree Search have been successfully used in the design of MIMO (i.e., multiple antenna) transceivers. In addition, highly quantized implementations, such as binarized networks, have led to implementations that are well-suited to power-limited mobile platforms. In addition, metaheuristic optimization techniques such the genetic algorithm and others have been used to automatically find highly efficient deep learning architectures, eliminating the need for lengthy and tedious manual experimentation. This lecture will describe these approaches and present some recent design examples. Relationships between the algorithms will be emphasized, and important computational issues will be highlighted. Finally, opportunities for future research in these areas will be suggested.



Mircea Stan

University of Virginia, USA

mircea@virginia.edu

Biography

Mircea R. Stan received the Ph.D. (1996) and the M.S. (1994) degrees from UMass Amherst and the Diploma (1984) from the Polytechnic Institute in Bucharest, Romania. Since 1996 he has been with the ECE Department at UVa, where he is now the Virginia Microelectronics Consortium (VMEC) Professor. Prof. Stan is teaching and doing research in the areas of high-performance low-power VLSI, temperature-aware circuits and architecture, embedded systems, spintronics, and nanoelectronics. He leads the High-Performance Low-Power (HPLP) lab, is an associate director of the Center for Automata Processing (CAP) and an assistant director of the Center for Research in Intelligent Storage and Processing-in-Memory (CRISP). He was a visiting faculty at UC Berkeley in 2004-2005, at IBM in 2000, and at Intel in 2002 and 1999. He has received the 2018 Influential ISCA Paper Award (for the 2003 paper “Temperature-aware microarchitecture”), the NSF CAREER award in 1997 and was co-author on best paper awards at ASILOMAR19, LASCAS19, SELSE17, ISQED09, GLSVLSI06, ISCA03 and SHAMAN02 and on IEEE Micro Top Picks in 2008 and 2003. He gave keynotes at DCAS18, SOCC16, CogArch16, WoNDP15, iNIS15 and CNNA14. He was the chair of the VSA-TC of IEEE CAS in 2005-2007, general chair for ISLPED06 and GLSVLSI04, TPC chair for SOCC18, ISVLSI17, NanoNets07 and ISLPED05, and on technical committees for numerous conferences. He is Associate Editor-in-Chief (AEIC) for the IEEE TVLSI, Senior Editor (SE) for the IEEE TNano, Associate Editor (AE) for IEEE Design & Test, and was an AE for the IEEE TNano in 2012-2014, IEEE TCAS I in 2004-2008 and for the IEEE TVLSI in 2001-2003. Prof. Stan is a fellow of the IEEE, a member of ACM and AAAS, and of Eta Kappa Nu, Phi Kappa Phi and Sigma Xi. His h-index is 52 and his i10-index is 135.

Lecture 1: Processing in Memory (PIM) – Power and Thermal Challenges and Opportunities

Memory technology is a defining component of modern computing and has a strong impact on performance, power and cost of computing systems. However, the advances in memory performance have not been able to keep up with the performance advances for CPU’s, thus leading to what is known as “the memory wall.” Depending on the application, the memory wall manifests itself both in terms of memory latency, as well as memory bandwidth. An interesting solution to the memory wall problem is to bring memory closer to the processor, or vice-versa, to move some processing capability in the memory itself – this leads to variations of what is known as Near-Memory Processing, Processing in Memory (PiM), etc. This seminar will first introduce a PIM taxonomy along several dimensions of the PiM design space; it will then follow with a history of PIM, then go over several recent PIM examples. The seminar will then go in depth into the Thermal/Power delivery challenges for PIM that are a result of the increased switching activities inherent to the moving of processing into the memory fabric, and exacerbated by the evolution towards 3D integration due to the slow-down of traditional Moore’s law methods. The seminar will conclude with some novel solutions that alleviate the Thermal/Power challenges for PiM.

Lecture 2: Smart Dust with Asynchronous Stream Processing (ASP)

Asynchronous circuits have many advantages over their synchronous counterparts in terms of robustness to parameter variations, wide supply voltage ranges, and potentially low power by not needing a clock, yet their promise has not been translated yet into commercial success due to several issues related to design methodologies and the need for handshake signals. Stochastic computing is another processing paradigm that has shown promises of low power and extremely compact circuits but has yet to become a commercial success mainly because of the need for a fast clock to generate the random streams. The recently proposed Asynchronous Stream Processing combines the best features of asynchronous circuits (lack of clock, robustness) with the best features of stochastic computing (processing on streams) to enable extremely compact and low power sensing “motes” that can finally fulfill the promise of smart dust, another concept that was ahead of its time and yet to achieve widespread deployment. This seminar will go into the details of an Asynchronous Stream Processing (ASP) mote. The ASP mote includes input sensors, asynchronous sigma-delta modulators that convert the sensor data into streams, asynchronous stream processing units to process the streams, analog memories to store data, energy sources, and pulse-based ultra-wide band (UWB) units to transmit the processed data. Among the unique characteristics of the ASP mote are: exact stream adders based on Sigma-Delta modulation, and the direct transmission of conditioned Sigma-Delta streams as pulses for UWB.

Zhihua Wang

Tsinghua University, China

zhihua@tsinghua.edu.cn

Biography

Zhihua Wang (M'99-SM'04-F'17) received the B.S., M.S., and Ph.D. degrees in Electronic Engineering in 1983, 1985 and 1990, respectively, from Tsinghua University, Beijing, China, where he has served as full professor and Deputy Director of the Institute of Microelectronics since 1997 and 2000. He was a visiting scholar at CMU (1992-1993) and KU Leuven (1993-1994), and was a visiting professor at HKUST (2014.9-2015.3). His current research mainly focuses on CMOS RFIC and biomedical applications, involving RFID, PLL, low-power wireless transceivers, and smart clinic equipment combined with leading edge RFIC and digital signal processing techniques. He has co-authored 13 books/chapters, over 209 (537) papers in international journals (conferences), over 249 (29) papers in Chinese journals (conferences) and holds 122 Chinese and 9 US patents.

Prof. Wang has served as the chairman of IEEE SSCS Beijing Chapter (1999-2009), an AdCom Member of the IEEE SSCS (2016-2019), a technology program committee member of the IEEE ISSCC (2005-2011), a steering committee member of the IEEE A-SSCC (2005-), the technical program chair for A-SSCC 2013, a guest editor for IEEE JSSC Special Issues (2006.12, 2009.12 and 2014.11), IEEE SSCS Distinguished Lecturer(2018-2019), Associate Editors in Chief, IEEE Open Journal of Circuits and Systems (2019~), associate editor of IEEE Trans on CAS-I(2016-2020), IEEE Trans on CAS-II(2010-2013) and IEEE Trans on BioCAS(2008-2015), TPC Member of IEEE International Solid State Circuit Conference (ISSCC, 2005-2011), IEEE CASS Technical Committee member for Biomedical and Life Science Circuits and Systems (2016~2019), Steering Committee Member of IEEE Asian Solid-State Circuits Conference(A-SSCC, 2004-2025) and other administrative/expert committee positions in China's national science and technology projects.

Lecture 1: Binaural Hearing Aid and Artificial Intelligence in Fitting and Signal Processing

Nowadays, the hearing aid technology is facing a new horizon based on advanced digital signal processing, wireless communication and artificial intelligence. In this lecture, new methodology with a systematic solution covering both the auditory periphery and the cognitive system is given. The up to date and rapidly evolves technologies for the binaural hearing aid system are well addressed. The multi-channel wide dynamic range compression, active noise reduction, self-adaptable directivity, acoustic scene analysis, and the wireless linking with other audio or communication systems are presented. The key technologies including the ultra-low power chip design, the advanced digital signal processing (DSP), and the wireless system integration and connectivity are discussed. The micromechanics and high-performance electro-acoustics, the miniaturized antenna, the user interface, and the fitting system development are also the important aspects for the hearing aid technologies are shown in this lecture. A smart binaural hearing aid technology, which simultaneously processes the acoustic signals from the four

microphones in both ears are indicated which utilizing the computing power from the smart phone to finish the advanced binaural DSP algorithms.

Lecture 2: Challenges and the Design of RF a Transceiver for Medical Applications

The demand of medical electronic devices, to make the medical devices smaller and smarter, is one of the driving forces of integrated circuits and systems. The implantable medical devices (IMD's), which are fully or partially implanted in the human bodies through surgeries, have a series of strict technical requirements including the choice of frequency and bandwidth, low power consumption, data rate, signal modulation method, disturbing and interference etc. This lecture focuses on a recently proposed technique in the art of radio transceiver design to reduce power consumption and area occupation. A set of miniature IMD's have been implemented using this ultra-low power transceiver which can be integrated in different application specific systems-on-a-chip (SoC's).