IEEE JOURNAL ON

EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS

Call for Papers

Revolution of AI and Machine Learning with Processing-in-Memory (PIM): from Systems, Architectures, to Circuits

Guest editors:

- Tony Tae-Hyoung Kim, Nanyang Technological University, Singapore (Corresponding Guest Editor)
- Bongjin Kim, University of California, Santa Barbara, CA, USA
- Joo-Young Kim: KAIST, South Korea
- Jaydeep Kulkarni, University of Texas at Austin, TX, USA

Scope and Purpose

Artificial intelligence (AI) and machine learning (ML) technology are revolutionizing many fields of study as well as a wide range of industry sectors such as information technology, mobile communication, automotive, and manufacturing. As more industries are adopting the technology, we are facing an ever-increasing demand for a new type of hardware that enables faster and more energy-efficient processing for AI workloads.

Traditional von-Neumann compute-centric computers such as CPU and GPU, which fetch data from the memory devices to on-chip processing cores, have been improving their computing performances rapidly with the scaling of process technology. However, in the era of AI and ML, as most workloads involve simple but data-intensive processing between large-scale model parameters and activations, data transfer between the storage and compute device becomes the bottleneck of the system (i.e., von-Neumann bottleneck). Memory-centric computing takes an opposite approach to solve this data movement problem. Instead of fetching data from the storage to compute, data stays in the memory while the processing units are merged into it so that computations can be done in the same location without moving any data. Processing-In-Memory (PIM) has attracted research community's attention because it can improve the energy efficiency dramatically in the memory-centric computing by minimizing the data movement. While the benefits of PIM are well accepted in the era of AL and ML, the limitations and the challenges in implementing PIM have not been investigated thoroughly. Many special issues of IEEE transactions have focused on 'AI and ML algorithms', 'AI and ML system architectures', and 'AI and ML hardware accelerators'. However, none of them has covered PIM comprehensively. PIM can be designed with various memory types such as dynamic-random-access-memory (DRAM), static-random-access-memory (SRAM), and various non-volatile memory (NVM) devices. The pros and cons of each memory type for PIM operation vary significantly. They also affect the architecture and the circuit implementation.

Topics of interest

This special issue of IEEE JETCAS will explore academic and industrial research on topics related to processing-in-memory circuits and architectures. Topics include, but are not limited to:

- Processing-in-memory circuits and systems for machine learning and AI applications
- Processing-in-memory circuits and systems for other applications including graph processing, data analytics, and genomics
- Energy-efficient processing-in-memory design for edge computing
- Processing-in-memory modeling and data management
- Solving memory bottlenecks for emerging data-centric systems
- Modeling of emerging memory devices for processing-in-memory
- Processing-in-memory architectures for general-purpose processing and/or neural networks
- Processing-in-memory architectures and applications
- Interaction of processing-in-memory modules with CPU architecture
- Multi-level memory hierarchy architectures for processing-in-memory
- System-level design and benchmarking of processing-in-memory in AI and machine learning
- Conventional and emerging memory technologies for processing-in-memory
- Heterogeneous integration of processing-in-memory
- Processing-in-memory prototypes for AI, machine learning, and neural networks
- Processing-in-memory computing for edge/IoT/embedded systems

Submission procedure

Prospective authors are invited to submit their papers following the instructions provided on the JETCAS website: https://mc.manuscriptcentral.com/jetcas. The submitted manuscripts should not have been previously published nor should they be currently under consideration for publication elsewhere.

Important dates

- Manuscript submissions due 2021-12-07
- First round of reviews completed 2022-01-31
- Revised manuscripts due 2022-03-15
- Second round of reviews completed 2022-04-15
- Final manuscripts due 2022-05-10
- Publication date 2022-06-30

Request for information

- Tony Tae-Hyoung Kim (thkim@ntu.edu.sg)