Design of Over GIGA bit Wireless LSI systems

Yoshikazu Miyanaga

Hokkaido University
Laboratory of Information Communication Networks
Graduate School of Information Science and Technology

Sapporo 060-0814, Japan
Contents

- Research Background
  - OFDM, MIMO
- Proposed MIMO-OFDM System
  - 600Mbps, 80 MHz Band by 2x2 MIMO-OFDM
  - 2.6Mbps, 160 MHz Band by 4x4 MIMO-OFDM
- VLSI Design of Proposed Transceiver
  - Super Low-Power LSI Design
Background on Methods

Communication Methods

- Current Main Stream: **54MBPS** (IEEE 802.11a, .11g)
  → It is not enough when wireless USB and multi-media communication are considered.

- Establish of **IEEE 802.11n** Standardization
  → Over **100 different methods** have been nominated at the end of 2005. In late 2009, its standardization will be completed.
  → The 600MBSP throughput of IEEE 802.11n is most suitable candidate as final one but it is not enough.
  → The new standardization, i.e., IEEE 802.11ac, has started since 2008 Autumn.
  → IEEE 802.11ac is now trying to develop a system over 1 Gbps wireless throughput with beyond 80MHz.
Current Trend of MIMO-OFDM Systems

IEEE802.11 Standards

Development by Hokkaido Univ. (Baseband)

Hokkaido Univ. 4x4 MIMO-OFDM (2008) 1.5 Gbps

IEEE802.11a (2002) 54Mbps

IEEE802.11n Draft (2007) 300Mbps

IEEE802.11n Optional (2008?) 600Mbps

IEEE802.11 VHT Study Group

Hokkaido Univ. 2x2 MIMO-OFDM (2006) 600 Mbps

Hokkaido Univ. SISO-OFDM (2005) 300 Mbps

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Background on Systems

- Digital Baseband (BB) + Radio Frequency (RF)
  - MIMO indicates many antennas.
    - A system will be large.
    - Its decoder must be quite complicated.
  - A package of a low power consumption system including BB and RF can be designed, cannot it?
  - A real MIMO-BB chip has been developed but what kind performance can be realized?
    - Is it possible to realize 4x4, 6x6 ····· larger MIMO system in LSI?
Basic OFDM System

- **Input Data**
  - Mapping
  - S/P
  - IFFT
  - Guard Interval
  - P/S
  - D/A
  - Channel

- **Output Data**
  - Demapping
  - P/S
  - Equalizer
  - FFT
  - Delete GI
  - S/P
  - A/D
Basic OFDM System

Coder: cov, blk

De-Coder: Viterbi, LDPC

Input Data

Mapping

S/P

IFFT

Guard Interval

P/S

D/A

channel

Low Power Design

512 – 1024 p FFT within several nano second

512 – 1024 p FFT within several nano second

Output Data

Demapping

P/S

Equalizer

FFT

Delete GI

S/P

A/D

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MIMO System

Transmitter

Receiver

TX

RX

Encoder → Mapper → IFFT
Encoder → Mapper → IFFT

IFFT

MIMO Detector

FFT

FFT

De-Mapper → Decoder
De-Mapper → Decoder
MIMO Decoding Circuit

- The instance when the receiver gets the training symbols
  - The estimation of channel and the inverse matrix calculation should be completed.

- The instance when the receiver gets data symbols
  - MIMO decoding should be done.

\[
\begin{align*}
A, B & \quad \text{(from 1st and 2nd training symbols)}
\end{align*}
\]

\[
\begin{align*}
H & \quad \text{Channel Estimation}
G & = H^{-1}
\end{align*}
\]

\[
\begin{align*}
\text{Inverse Matrix} & \quad \text{Memory}
\end{align*}
\]

\[
\begin{align*}
\text{MIMO Detector} & \quad y \\
\bar{s} & \quad \text{from FFT}
\end{align*}
\]
MIMO Decoding Circuit

- Super high speed & Ultra low power ....

\[ \begin{align*}
A & \rightarrow y \\
B & \rightarrow y \\
\text{Channel Estimation} & \\
\text{Inverse Matrix} & \quad G = H^{-1} \\
\text{Low Power Design} & \\
\text{Memory} & \\
\text{MIMO Detector} & \rightarrow \bar{s} \\
\text{Matrix Inversion within several nano seconds} &
\end{align*} \]
Overview

- One Chip/Package Wireless System
  - A total system including interface, BB, RF and antennas.
  - The Next Generation LAN/PAN: Super Speed Hot Spot, Wireless Home Theater, Next Generation High Speed LAN etc

- Realization of both high speed and Low power
  - High Speed Wireless → 2.6 GBPS Throughput
    - High Performance MIMO System → In Door Wireless
  - Very Low Power BB-LSI → 1W System
    - Dynamic Architecture → Optimum Low Power Consumption
    - Soft Wireless → High Throughput and Low Power Consumption
Wireless Communication Chip

OFDM: Modulation/De-Modulation
IEQ: Intelligent Equalizer
Con: System Controller
MAC: Media Access Controller
MIMO: Multi I/O Module
RF: Radio Frequency Analog Circuits
Conventional Wireless Communication Chip

- Conventional
  - 11a 54MBPS
  - 11n 300MBPS
  - 100-900mW power consumption

- Conventional
  - BLAST
  - 4x4 Streams
  - Distance: Several meters
  - 2x3MIMO System

General Networks

Conventional Wireless Communication Chip

- Con
- MAC
- OFDM
- MIMO

Antenna

RF
Proposed Wireless Communication Chip

① SISO 300MBPS by parallel/pipeline processing
② Low Power Consumption of 300mW by Dynamic Architecture
③ BER Improvement by Noise Reduction
④ Cognitive OFDM System

① 4x4 MIMO-OFDM
② 700mW Power Consumption
③ 2.6GBPS Throughput
MIMO, OFDM ....

BASIC TECHNOLOGIES
Basic OFDM System
OFDM

- **OFDM**
  - Orthogonal Frequency Division Multiplexing
  - One of Digital Modulation Technique in which many orthogonal carrier are multiplexed.

- **OFDM is important, isn’t it?**
  - Several key systems, e.g., surface digital TV of Japan and EU, High Speed ADSL MODEM, Wireless LAN etc employs OFDM.
  - OFDM can be fabricated into LSI.
Digital Modulation

\[ s(t) = A \cdot \cos(2\pi \cdot f_c \cdot t + \theta_k) \]

- **ASK**: Amplitude Shift Keying
- **PSK**: Phase Shift Keying
- **FSK**: Frequency Shift Keying

1 bit/1 symbol

Modulation Technique
AS K and PS K Modulation in OFDM

- Multi-Valued Modulation Technique
  - 1 symbol represents several bits at one time.

Binary PSK (BPSK)

Quadrature PSK (QPSK)
Representation of Digital Modulation

The signal $s(t)$ in communication can be represented as

$$s(t) = \text{Re}[ (a_k + jb_k) e^{j2\pi f_c t} ]$$

where

- $e^{j2\pi f_c t}$ : carrier component
- $a_k + jb_k$ : digital modulation component : signal

All digital signals are represented as complex values:

$$(a_k + jb_k) e^{j2\pi f_c t}$$
QAM (Quadrature Amplitude Modulation)

- The digital components $a_k + jb_k$ in case of QPSK can be represented in the complex domain.

\[
\begin{align*}
\frac{-\sqrt{2}}{2} + j\frac{\sqrt{2}}{2} \\
\frac{\sqrt{2}}{2} + j\frac{\sqrt{2}}{2} \\
\frac{-\sqrt{2}}{2} - j\frac{\sqrt{2}}{2} \\
\frac{\sqrt{2}}{2} - j\frac{\sqrt{2}}{2}
\end{align*}
\]
16QAM and 64QAM

16QAM

64QAM
Data Mapping on Spectrum Domain

- Data are assigned onto spectrum domain. Accordingly, each complex signal can be mapped to each frequency.
  - High efficiency can be kept within a communication bandwidth.
Basic OFDM System
Basic OFDM System
Gard-Interval

The $n$-th Symbol

Same data are copied.
Same signals are coming to a receiver with different time delays.
GI and Multi-Path

A receiver can get an original symbol but a phase rotation happens by multi-paths.
Influence to Symbols

Phase Rotation on Complex Domain
Basic OFDM System
2 × 2 MIMO System

Transmitter

Encoder → Mapper → IFFT

Encoder → Mapper → IFFT

Receiver

FFT → MIMO Detector

FFT → MIMO Detector

De-Mapper → Decoder

De-Mapper → Decoder

RX
MIMO Decoder

- Linear Decoding
  - ZF
  - MMSE
- Sequential Decoding
  - V-BLAST (ZF Criterion)
  - V-BLAST (MMSE Criterion)

Cost

Performance
Zero-Forcing (1)

MIMO Channel Model

\[
y = Hs + n
\]

Received Signal  Transmitted Signal  Noise

Channel Matrix

The inverse matrix of an estimated channel matrix is applied and then the original transmitted signal is estimated.

\[
\bar{s} = H^{-1}y
\]
Zero-Forcing (2)

Calculation of Inverse Matrix

- In case of 2x2 matrix, its processing can be implemented as inverse matrix equation explicitly.

\[ H = \begin{bmatrix} a & b \\ c & d \end{bmatrix} \]

\[ H^{-1} = \frac{1}{ad - bc} \begin{bmatrix} d & -b \\ -c & a \end{bmatrix} \]
MIMO Decoding Circuit

- In case of the receive of training symbol:
  - Blocks of channel estimation and inverse matrix calculation are activate.
- In case of the receive of data symbol:
  - A block of MIMO decoding is activate.

\[
\begin{align*}
G & = H^{-1} \\
\bar{S} & \text{ from FFT, A, B (from 1st and 2nd training symbols), Channel Estimation, Inverse Matrix, Memory, MIMO Detector}
\end{align*}
\]
Contributes in this Study

- New MIMO-OFDM Systems by Our Project
  - IEEE802.11 a/g (54 Mbps)
  - Wideband SISO-OFDM (300 Mbps)
  - 2x2 MIMO-OFDM (600 Mbps)
  - 4x4 MIMO-OFDM (2.6 Gbps)
  - New OFDM Format at 80-160 MHz Bandwidth
  - VLSI Design of OFDM Transceivers
## Proposed 2x2 MIMO-OFDM Format

### Transmit mode

<table>
<thead>
<tr>
<th>Mode</th>
<th>Coding Rate</th>
<th>Modulation</th>
<th>Data Rate (Mbps) SISO-OFDM</th>
<th>Data Rate (Mbps) MIMO-OFDM</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1/2</td>
<td>QPSK</td>
<td>66.6</td>
<td>133.3</td>
</tr>
<tr>
<td>2</td>
<td>1/2</td>
<td>16QAM</td>
<td>133.3</td>
<td>266.6</td>
</tr>
<tr>
<td>3</td>
<td>1/2</td>
<td>64QAM</td>
<td>200</td>
<td>400</td>
</tr>
<tr>
<td>4</td>
<td>3/4</td>
<td>64QAM</td>
<td>300</td>
<td>600</td>
</tr>
</tbody>
</table>

### Frame Format

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>FFT/IFFT Window Length</td>
<td>6.4 us (512 samples)</td>
</tr>
<tr>
<td>Guard Interval Length</td>
<td>0.8 us (64 samples)</td>
</tr>
<tr>
<td>Number of Subcarriers</td>
<td>512</td>
</tr>
<tr>
<td>Number of Data Subcarriers</td>
<td>480</td>
</tr>
<tr>
<td>Frequency Spacing</td>
<td>0.1563 MHz</td>
</tr>
</tbody>
</table>
Transmit Performance

- Packet Size: 1000-byte Packet Length
- Modulation: 64-QAM
- Channel Model: 150-ns Delay Spread
  - TGn Channel Model D
- Evaluation
  - 4x4 IEEE802.11n (600 Mbps, 5/6-Coding Rate)
  - 4x2 Proposed-MIMO (600 Mbps, 3/4-Coding Rate)
  - 2x2 Proposed-MIMO (600 Mbps, 3/4-Coding Rate)
BER Performance

![Graph showing Bit Error Rate (BER) performance for different antenna configurations.]

- **4x4 IEEE802.11n**
- **4x2 STARC-MIMO**
- **2x2 STARC-MIMO**

The graph illustrates the bit error rate (BER) performance over the average carrier-to-noise ratio (CNR) per receiver antenna (in dB). The performance is compared for 4x4 IEEE802.11n, 4x2 STARC-MIMO, and 2x2 STARC-MIMO configurations.

A significant difference is noted at an average CNR of 7 dB, where the 4x2 STARC-MIMO configuration shows a notable improvement over the 2x2 STARC-MIMO configuration.
SISO-OFDM System

- Specification
  - 512-point FFT/IFFT
  - IIR Filter Type Flame Syncronization
  - Convolutional Coding
  - Soft Viterbi Decoding (Constraint Length 7  Rate 1/2)
  - QPSK, 16QAM, 64QAM Mod/De-Modulation

**Diagram:**
- BB Receiver 12bit
- BB Transmitter 12bit
- MAC Receiver 3bit
- MAC Transmitter 3bit
- Error Correction Output 3bit
- Metric 16bit × 6
# SISO-OFDM (ASPLA 90nm)

<table>
<thead>
<tr>
<th>Component</th>
<th>mm²</th>
<th>Game #</th>
<th>Power Con Tra (mW)</th>
<th>Power Con Rec (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Control</td>
<td>5006</td>
<td>1668</td>
<td>0.11</td>
<td>0.11</td>
</tr>
<tr>
<td>Coding/Mapping</td>
<td>10143</td>
<td>3381</td>
<td>0.29</td>
<td>0.10</td>
</tr>
<tr>
<td>Flame Synchronization</td>
<td>80573</td>
<td>26858</td>
<td>1.44</td>
<td>5.26</td>
</tr>
<tr>
<td>FFT/IFFT, Channel Eq.</td>
<td>838144</td>
<td>279381</td>
<td>39.30</td>
<td>39.92</td>
</tr>
<tr>
<td>GI・Preamble Signal Pro.</td>
<td>13854</td>
<td>4618</td>
<td>0.34</td>
<td>0.13</td>
</tr>
<tr>
<td>Modulation/Sync. SRAM</td>
<td>285576</td>
<td>95192</td>
<td>10.06</td>
<td>9.64</td>
</tr>
<tr>
<td>Demodulation·GI SRAM</td>
<td>285576</td>
<td>95192</td>
<td>9.12</td>
<td>9.36</td>
</tr>
<tr>
<td>Soft Viterbi</td>
<td>224894</td>
<td>74964</td>
<td>2.67</td>
<td>16.54</td>
</tr>
<tr>
<td>Viterbi Decoding</td>
<td>2545635</td>
<td>848545</td>
<td>12.64</td>
<td>178.28</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>4,289,401</strong></td>
<td><strong>1,429,799</strong></td>
<td><strong>75.97</strong></td>
<td><strong>259.34</strong></td>
</tr>
</tbody>
</table>
FPGA Board for Evaluation

- Gigabit Ethernet PHY
  - Gigabit Ethernet MAC
  - STARC MAC
- Altera
  - STARC PHY
- Output

Xilinx
2x2 MIMO-OFDM

- SDM-MIMO Decoding
  - Transmission Rate
    - 600Mbps
  - Transmission Distance
    - It is shorter than our proposed 4x2 MIMO-OFDM
- System Overview
  - 2 Parallel SISO-OFDM
  - MIMO Decoding
MIMO System

Transmitter

TX

Receiver

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PPDU Format

- The format is based on 02.11n and STARC MIMO-OFDM PPDU.
  - Number of training symbol is set to 2.

![Diagram showing PPDU format with SC-STF, SC-AGC, SC-LTF, SC-SIG, DATA sections. St.1 and St.2 are highlighted with I and -I for SC-LTF, and I and I for SC-SIG, DATA. SNR Estimation and Channel Estimation are marked.]
## Simulation Results

<table>
<thead>
<tr>
<th></th>
<th>SISO</th>
<th>MIMO</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mapping</strong></td>
<td>64QAM</td>
<td></td>
</tr>
<tr>
<td><strong>Coding</strong></td>
<td>Convolutional Coding (R=1/2)</td>
<td>Viterbi Decoding</td>
</tr>
<tr>
<td><strong>Bandwidth</strong></td>
<td>80M Hz</td>
<td></td>
</tr>
<tr>
<td><strong>FFT #</strong></td>
<td>512 (data:480, pilot:20)</td>
<td></td>
</tr>
<tr>
<td><strong>OFDM Symbol #</strong></td>
<td>8</td>
<td></td>
</tr>
<tr>
<td><strong>TX Rate</strong></td>
<td>200M bps</td>
<td>400M bps</td>
</tr>
<tr>
<td><strong>Antenna #</strong></td>
<td>1 x 1</td>
<td>2 x 2, 4 x 2</td>
</tr>
<tr>
<td><strong>Channel Model</strong></td>
<td>HYPERLAN2/Model A AWG</td>
<td>TGn Sync Channel/Model D AWG</td>
</tr>
<tr>
<td><strong>Channel Est.</strong></td>
<td>Legacy</td>
<td>Orthogonal Coded Pilot</td>
</tr>
<tr>
<td><strong>MIMODecoding</strong></td>
<td>2x2 ZERO–FORCING 2x2 BLAST (MMSE) 4x2 G–LST (MMSE)</td>
<td></td>
</tr>
</tbody>
</table>
Results
Circuit Structure of 2x2 MIMO-OFDM Transceiver

- Full-Pipelined Processing
- Duplicated Processing Blocks Supporting for Two Data Streams

(A) Encoding & Mapping
(E) Pre-Transform Memory
(B) Frame Sync.
(C) FFT/IFFT
(F) Post-Transform Memory
(D) GI/PLCP Insertion
(G) MIMO Detection
(H) De-Mapping
(I) Viterbi Decoding

ZF, MMSE, V-BLAST, ...
Dynamic Architecture of Low Power

Realization of High Throughput and Low Power
Timing of MIMO Decoding

High Latency Type (It can be designed by General Purpose Processor)

- Merit ... Circuit Scale is small.
- Demerit ... Long processing time is required.

Low Latency Type (Pipeline and Parallel Processing are used)

- Demerit ... Circuit Scale is large and it is complicated.
- Merit ... Small Circuit size is obtained.

Latency (In case of GI time, it is 0)
Channel Estimation & Inverse Matrix

- 1 OFDM symbol sampling time
  - 512(FFT)+64(GI)=576
- Processing time of Channel Est and Inv Matrix
  - 480(Data Subcarriers) + 11 (Pipeline Latency) = 491

\[
\delta = H_{11} H_{22} - H_{12} H_{21}
\]

\[
\delta \delta^* = \frac{1}{\delta \delta^*}
\]

Processing can be done in 1 symbol.
VLSI Implementation of OFDM Transceivers

- Circuit Design
  - Fixed-Point Simulation: Matlab
  - RTL Design: Verilog
- CMOS Implementation
  - ASPLA 90nm
    - SISO-OFDM Transceiver
    - 2x2 MIMO-OFDM Transceiver
## Circuit Performance

### 2x2 MIMO-OFDM Decoder

<table>
<thead>
<tr>
<th>Detection Algorithm</th>
<th>Zero Forcing</th>
<th>MMSE-BLAST</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Subcarriers</td>
<td>480</td>
<td></td>
</tr>
<tr>
<td>No. of Pipeline Stages</td>
<td>11</td>
<td>14</td>
</tr>
<tr>
<td>Pipeline Latency (μs)</td>
<td>0.18</td>
<td>0.21</td>
</tr>
<tr>
<td>No. of Complex Multipliers</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>No. of Real Multipliers</td>
<td>11</td>
<td>27</td>
</tr>
<tr>
<td>Clock Frequency (MHz)</td>
<td></td>
<td>80</td>
</tr>
<tr>
<td>NAND Gate Count</td>
<td>371,537</td>
<td>1,160,092</td>
</tr>
<tr>
<td>Function</td>
<td>Area (mm²)</td>
<td>Gate #</td>
</tr>
<tr>
<td>--------------------------------</td>
<td>------------</td>
<td>--------</td>
</tr>
<tr>
<td>System Control</td>
<td>118353</td>
<td>39451</td>
</tr>
<tr>
<td>Coding/Mapping</td>
<td>20286</td>
<td>6762</td>
</tr>
<tr>
<td>Flame Syncronization</td>
<td>81967</td>
<td>27322</td>
</tr>
<tr>
<td>FFT/IFFT</td>
<td>1166008</td>
<td>388669</td>
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<td>MIMO Decoding</td>
<td>1114612</td>
<td>371537</td>
</tr>
<tr>
<td>GI・PLCP Addition</td>
<td>50928</td>
<td>16976</td>
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<tr>
<td>Modulation/Syncro SRAM</td>
<td>573584</td>
<td>191195</td>
</tr>
<tr>
<td>De-Mod/GI Addition SRAM</td>
<td>573584</td>
<td>191195</td>
</tr>
<tr>
<td>Soft Decision</td>
<td>437280</td>
<td>145760</td>
</tr>
<tr>
<td>Viterbi De-Modulation</td>
<td>5073270</td>
<td>1691090</td>
</tr>
<tr>
<td>合計</td>
<td><strong>9,209,872</strong></td>
<td><strong>3,069,957</strong></td>
</tr>
</tbody>
</table>
## Implementation Results

<table>
<thead>
<tr>
<th></th>
<th>Circuit Area (mm²)</th>
<th>No. of Logic Gates</th>
<th>Power TX (mW)</th>
<th>Power RX (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SISO-OFDM</td>
<td>4.30</td>
<td>1.43 M</td>
<td>76.0</td>
<td>259.3</td>
</tr>
<tr>
<td>2x2 MIMO-OFDM</td>
<td>9.21</td>
<td>3.07 M</td>
<td>139.8</td>
<td>535.0</td>
</tr>
</tbody>
</table>
Proposed MIMO-OFDM PPDU Format

IEEE802.11a Compatible Preamble & SIGNAL
T GnSync Compatible

20MHz

8.0μs 8.0μs 4.0μs 4.0μs 2.0μs 2.0μs 28.8μs 7.2μs 7.2μs 7.2μs

Tx1

L-STF L-LTF L-SIG HT-SIG
L-STF L-LTF L-SIG HT-SIG
L-STF L-LTF L-SIG HT-SIG
L-STF L-LTF L-SIG HT-SIG

SC-STF SC-AGC SC-LTF SC-LTF SC-LTF SC-LTF SC-LTF SC-SIG DATA

7.2μs

80MHz

DATA

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Real-time MIMO Detection

- MIMO-OFDM systems must compute inverse matrices of the channels for all the subcarriers.

<table>
<thead>
<tr>
<th>Proposed</th>
<th>Algorithm</th>
<th>Complexity</th>
</tr>
</thead>
<tbody>
<tr>
<td>SISO 4x2 MIMO</td>
<td>V-BLAST</td>
<td>$2^3=8$</td>
</tr>
<tr>
<td>4x2 MIMO</td>
<td>V-BLAST &amp; STBC</td>
<td>$4^2=16$</td>
</tr>
<tr>
<td>IEEE802.11n 4x4 MIMO</td>
<td>V-BLAST</td>
<td>$4^3=64$</td>
</tr>
</tbody>
</table>

(Use of QR decomposition)

- Processing time of MIMO detection influences response time in PHY and MAC layer.

Low-Latency and High-Throughput Architecture
Overview of $4 \times 2$ V-LSTBC System

- Max Throughput: 600 Mbps
- $4 \times 2$ V-LSTBC System
  - Using LST(SDM), the throughput increases.
  - Using STBC, the transmission length increases.
- $4 \times 2$ V-LSTBC Decoding
  - The cost of $O(M^4)$ can decrease to $O(M^2)$ by using new algorithm.
- PPDU Flam Format is proposed.
  - IEEE802.11a/IEEE802.11n based Format
  - Using GA, its preamble is optimized.
- Evaluation of System based on standard channel models
  - Transmission with 600 Mbps(MAX) → 20m transmission
HU-VHT MIMO-OFDM Transmitter

- FEC Enc
- Puncture
- Spatial stream parse
- Stream
  - frequency Interleaver
  - Mapper
  - S/P
  - STBC Encoder
  - IFFT
  - P/S
- Stream2
  - frequency Interleaver
  - Mapper
  - SP
  - STBC Encoder
  - IFFT
  - P/S
HU-VHT MIMO-OFDM Receiver

1. S/P → FFT → Interference Canceller → Channel Estimator → P/S
2. S/P → FFT → Interference Canceller → Channel Estimator → P/S

- De-Interleaver
- De-Mapper
- Spatial Stream De-parse
- De-Puncture
- Viterbi Dec
HU–VHT MIMO–OFDM vs. IEEE802.11n (Model B)

CNR [dB] vs. PER

4x2 V-LSTBC

4x2 HU-VHT MIMO (iid)

4x2 HU-VHT MIMO (corr)

4x4 IEEE802.11n (iid)

4x4 IEEE802.11n (corr)

7dB

4x4 IEEE802.11n
Comparisons of Link Budget

15 m is improved.
Block Diagram of 4x4 MIMO-OFDM Circuit

**Transmitter**
- Scrambler
- Encoder
- Interleave & Puncture
- Mapper
- Pilot Insertion
- IFFT
- Re-order & GI Insertion
- Preamble Insertion

**Receiver**
- Frame & Freq. Synchronization
- FFT
- Re-order & Pilot Remove
- Demapper
- Viterbi Decoding
- De-interleave & Dummy Data Insertion
- MIMO Channel Est. & Decoding
- De-scrambler
Complexity in MIMO Detection

<table>
<thead>
<tr>
<th>Detection Algorithm</th>
<th>Complexity (MIMO)</th>
<th>Complexity (MIMO-OFDM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ML</td>
<td>$O(2^{QN})$</td>
<td>$K \times O(2^{QN})$</td>
</tr>
<tr>
<td>OSIC</td>
<td>$O(N^4)$</td>
<td>$K \times O(N^4)$</td>
</tr>
<tr>
<td>Linear</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MMSE</td>
<td>$O(N^3)$</td>
<td>$K \times O(N^3)$</td>
</tr>
<tr>
<td>ZF</td>
<td>$O(N^2)$</td>
<td>$K \times O(N^2)$</td>
</tr>
</tbody>
</table>

$N$: No. of Antennas, $Q$: Quantization Level, $K$: No. of OFDM Subcarriers

- **MIMO-OFDM**
  - Considerable Complexity Even for Linear Detection
    - IEEE802.11n ... $K=128$, WiMAX ... $K=1024$
  - Conventional Hardware Architectures
    - Insufficiency for Real-Time MIMO-OFDM Detection
MMSE Detection

- Received Signal (Freq. Domain)
  \[ y_k(t) = H_k s_k(t) + n_k(t) \]

- MMSE Detection
  \[ G_k = (H_k^H H_k + \sigma_k^2 I)^{-1} H_k^H \]

- MIMO Decoding
  \[ \hat{s}_k(t) = G_k y_k(t) \]
Algorithm Consideration

- **Matrix Inversion (Most Costly)**
  - QR Decomposition
  - Sherman-Morrison
  - Matrix Inversion Lemma
  - Cholesky Decomposition

  \[ \text{Rely on Iterative Operations} \]

- **Analytic Solution** *(Strassen’s Matrix Inversion)*
  - Suitable for Pipelined Architecture Hardware
  - Simple Circuit Structure Using Systematic Operations
  - Reduce Complexity by Making Use of Properties of Complex Conjugate Symmetric (in case of MMSE)
Circuit Structure of MMSE Detector

- Complete Pipelined Architecture
  - Total 30 Pipeline Stages

Matrix Inputs

- \( H_{11}(k) \)
- \( H_{12}(k) \)
- \( H_{44}(k) \)

\( \sigma^2(k) \)

4x4 Matrix Multiplication

4 stages

4x4 Matrix Inversion

22 stages

Pipeline Delay

4x4 Matrix Multiplication

4 stages

Matrix Outputs

- \( P_{11}(k) \)
- \( P_{12}(k) \)
- \( P_{44}(k) \)

- \( R_{11}(k) \)
- \( R_{12}(k) \)
- \( R_{44}(k) \)

- \( S_a(k) \)
- \( S_b(k) \)

- \( Q_{11}(k) \)
- \( Q_{12}(k) \)
- \( Q_{44}(k) \)

- \( G_{11}(k) \)
- \( G_{12}(k) \)
- \( G_{44}(k) \)

\( k: \) Subcarrier Index

1/SNR

Scaling Factor in Block Floating-Point

Total 30 Pipeline Stages

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Matrix Operations

- Use of 2x2 Submatrices
  - Conjugate Symmetry in Non Diagonal Submatrices

\[ P_k = H_k^H H_k + \sigma_k^2 I \]

- Complexity Reduction
  - Strassen’s Matrix Multiplication and Inversion
  - Use of Conjugate Symmetry Submatrices
Matrix Inversion (1)

Strassen’s Matrix Inversion
- Block Operations by 2x2 Submatrices

$$\Omega = \begin{pmatrix} A & B \\ C & D \end{pmatrix}$$

$$\Omega^{-1} = \begin{pmatrix} A^{-1} + A^{-1}BE^{-1}CA^{-1} \\ -E^{-1}CA^{-1} \end{pmatrix}$$

$$E^{-1} = D - CA^{-1}B$$

Conjugate Symmetric

<table>
<thead>
<tr>
<th>Method</th>
<th>Mul</th>
<th>Add/Sub</th>
<th>Div/Rec</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct</td>
<td>1126</td>
<td>768</td>
<td>1</td>
</tr>
<tr>
<td>Cholesky</td>
<td>264</td>
<td>108</td>
<td>4</td>
</tr>
<tr>
<td>Strassen</td>
<td>120</td>
<td>150</td>
<td>2</td>
</tr>
</tbody>
</table>

Comparison of Real Operations
Matrix Inversion (2)

Pipeline Stages by 2x2 Matrix Operation Units

Matrix Inputs

A
B
D

Matrix Outputs

A'
B'
C'
D'

Block Floating Arithmetic Scaling

s1, s2, s3, s4

Scale In

Scale Out
Block Diagram of MIMO Decoder
Evaluation of Calculation Precision

- Simulation
  - IEEE802.11n Standards (4x4 MIMO-OFDM)
  - Multipath Rayleigh Fading (i.i.d. MIMO Spatial Correlation)

![Graph showing BER vs. Eb/N0 (dB)]

The graph shows the BER (Bit Error Rate) for different Eb/N0 (dB) values, with various precision levels (16 bits, 18 bits, 20 bits, and floating point) represented by different line styles. The data points and lines indicate the calculated precision levels for each bit configuration, illustrating the relationship between signal-to-noise ratio and error rate.
Circuit Implementation

- RTL Design
  - Verilog-2001
- 90-nm CMOS Implementation
  - 1.0-V Voltage Supply
  - 160-MHz Clock Frequency

<table>
<thead>
<tr>
<th>Wordlength (bits)</th>
<th>Area (mm²)</th>
<th>Gate Count</th>
<th>Power Dissipation (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>6.23</td>
<td>1,559,400</td>
<td>496.2</td>
</tr>
<tr>
<td>18</td>
<td>7.45</td>
<td>1,862,400</td>
<td>593.4</td>
</tr>
<tr>
<td>20</td>
<td>8.81</td>
<td>2,203,300</td>
<td>701.2</td>
</tr>
</tbody>
</table>
## Performance Comparison

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Matrix</strong></td>
<td>2 x 2</td>
<td>4 x 4</td>
<td>4 x 4</td>
<td>4 x 4</td>
<td></td>
</tr>
<tr>
<td><strong>Detection Algorithm</strong></td>
<td>ZF</td>
<td>ZF</td>
<td>MMSE</td>
<td>MMSE</td>
<td></td>
</tr>
<tr>
<td><strong>Hardware Configuration</strong></td>
<td>DSP</td>
<td>ASIC 90 nm</td>
<td>ASIC 0.25 µm</td>
<td>ASIC 90 nm</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TMS3206713</td>
<td>43 k gates</td>
<td>89 k gates</td>
<td>1.86 M gates</td>
<td></td>
</tr>
<tr>
<td><strong>Operating Freq.</strong></td>
<td>225 MHz</td>
<td>500 MHz</td>
<td>167 MHz</td>
<td>160 MHz</td>
<td></td>
</tr>
<tr>
<td><strong>Latency Time</strong></td>
<td>104 x $K$ (µs)</td>
<td>180 x $K$ (ns)</td>
<td>600 x $K$ (ns)</td>
<td>187.5 (ns)</td>
<td></td>
</tr>
</tbody>
</table>

$K$: No. of OFDM Subcarriers


Available Data Speed

- **Necessary Conditions**
  - Clock Frequency ≥ Baseband Bandwidth
  - Processing Latency ≤ GI Duration (400 ns)

A 2.6-Gbps MIMO-OFDM receiver is available by the proposed MMSE detector.

- 5/6 Coding Rate
- 64-QAM
- 400-ns GI Duration
4x4 MIMO-OFDM with 512 SUBCARRIERS

<table>
<thead>
<tr>
<th><strong>Transmitter</strong></th>
<th><strong>Area (mm^2)</strong></th>
<th><strong>Gate count</strong></th>
<th><strong>Power dissipation (mW)</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Scrambling</td>
<td>0.013</td>
<td>3,350</td>
<td>0.01</td>
</tr>
<tr>
<td>Encoding</td>
<td>0.013</td>
<td>3,210</td>
<td>0.03</td>
</tr>
<tr>
<td>Interleaving and puncturing</td>
<td>0.28</td>
<td>70,330</td>
<td>6.0</td>
</tr>
<tr>
<td>Mapping</td>
<td>0.12</td>
<td>2,960</td>
<td>0.03</td>
</tr>
<tr>
<td>Subcarrier assignment</td>
<td>0.59</td>
<td>147,610</td>
<td>13.0</td>
</tr>
<tr>
<td>IFFT</td>
<td>2.68</td>
<td>670,190</td>
<td>123.1</td>
</tr>
<tr>
<td>GI addition</td>
<td>0.89</td>
<td>223,560</td>
<td>24.6</td>
</tr>
<tr>
<td>Total</td>
<td>4.59</td>
<td>1,124,210</td>
<td>166.7</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Receiver</strong></th>
<th><strong>Area (mm^2)</strong></th>
<th><strong>Gate count</strong></th>
<th><strong>Power dissipation (mW)</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Synchronization</td>
<td>0.034</td>
<td>8,510</td>
<td>0.7</td>
</tr>
<tr>
<td>FFT</td>
<td>3.54</td>
<td>886,500</td>
<td>181.7</td>
</tr>
<tr>
<td>Subcarrier extraction</td>
<td>0.73</td>
<td>181,530</td>
<td>18.1</td>
</tr>
<tr>
<td>MIMO channel estimation and detection</td>
<td>12.88</td>
<td>3,219,000</td>
<td>233.7</td>
</tr>
<tr>
<td>De-mapping</td>
<td>0.33</td>
<td>83,050</td>
<td>5.9</td>
</tr>
<tr>
<td>De-interleaving and dummy bit insertion</td>
<td>1.37</td>
<td>342,640</td>
<td>30.9</td>
</tr>
<tr>
<td>Viterbi decoding</td>
<td>2.78</td>
<td>693,940</td>
<td>105.9</td>
</tr>
<tr>
<td>De-scrambling</td>
<td>0.013</td>
<td>3,350</td>
<td>0.02</td>
</tr>
<tr>
<td>Total</td>
<td>21.68</td>
<td>5,418,520</td>
<td>576.9</td>
</tr>
</tbody>
</table>
## Performance Evaluation

<table>
<thead>
<tr>
<th>Transmitter</th>
<th>Area (mm²)</th>
<th>Gate count</th>
<th>Power dissipation (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>128 subcarriers</td>
<td>2.53</td>
<td>632,780</td>
<td>89.6</td>
</tr>
<tr>
<td>256 subcarriers</td>
<td>3.09</td>
<td>772,450</td>
<td>117.7</td>
</tr>
<tr>
<td>512 subcarriers</td>
<td>4.59</td>
<td>1,124,210</td>
<td>166.7</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Receiver</th>
<th>Area (mm²)</th>
<th>Gate count</th>
<th>Power dissipation (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>128 subcarriers</td>
<td>18.47</td>
<td>4,618,450</td>
<td>451.4</td>
</tr>
<tr>
<td>256 subcarriers</td>
<td>19.19</td>
<td>4,798,180</td>
<td>496.0</td>
</tr>
<tr>
<td>512 subcarriers</td>
<td>21.68</td>
<td>5,418,520</td>
<td>576.9</td>
</tr>
</tbody>
</table>
Summary

- We have proposed the high-speed OFDM transceivers with the 80MHz-bandwidth.

- The proposed transceiver offers available hardware solution for real-time MIMO detection.

- The SISO-OFDM and MIMO-OFDM transceiver consumes a maximum of 260mW and 540mW in power dissipation in a 90-nm CMOS process.
Who?

Yoshikazu Miyanaga

He received the B.S., M.S., and Dr. Eng. degrees from Hokkaido University, Sapporo, Japan, in 1979, 1981, and 1986, respectively. He is currently a Professor at Graduate School of Information Science and Technology, Hokkaido University.

His research interests are in the areas of signal processing for wireless communications, nonlinear signal processing and low-power LSI systems.

He was a chair of Technical Group on Smart Info-Media System, IEICE. He is an advisory member of this technical group. Currently, he is IEICE fellow.

He served as a member in the board of directors, IEEE Japan Council as a chair of student activity committee from 2002 to 2004. He is a chair of student activity committee in IEEE Sapporo Section from 2001. He is a chair of IEEE Circuits and Systems Society, Digital Signal Processing Technical Committee from 2006.

References of this Topic in 2006


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