Advanced Modeling and Simulation Strategies for Power Integrity in High-Speed Designs

Ramachandra Achar
Carleton University
5170ME, Dept. of Electronics
Ottawa, Ont, Canada – K1S 5B6
*Email: achar@doe.carleton.ca;
Ph: 613-520-5651; Fax: 613-520-5708
AGENDA

• Introduction – Power Distribution Networks

• Power-Grid Modeling/Analysis Challenges

• Advanced Analysis Methods
  ➔ Partitioning
  ➔ Wave-form Relaxation
  ➔ Initial-guess generation
  ➔ Parallelization Schemes

• Numerical Results

• Conclusions
A PDS consists of:

- Voltage Regulator Modules (VRMs)
- Decoupling or Bypass Capacitors on the PCB and packages
- Printed Circuit Board (PCB) power planes
- Package power planes
- Chip power distributions

Most of the digital ICs require a PDS to deliver a voltage with a tolerance defined in datasheet.
Power Integrity in High-Speed Designs

**Trends**
- Decreasing Feature Size
- Increasing Frequency
- Mixed-domain integration (RF, optical, MEMs)
- Low Power

**Issues**
- Increased sensitivity to Supply variations
- Reduced noise margins
- Timing errors, Failed Designs

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity”
On-Chip PDNs: Flip Chip

- Uniform distribution of power
- Shorter contacts: reduced parasitics
- More widely used

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity"
Flip Chip PDN: Modeling

RC-PDN

VDD contact

Level 2

Level 1

Current Sources Representing Power-drain

Leakage + Switching Current

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity”
Flip Chip PDNs: “Large Power Grids”

- Can contain millions of nodes!
- Existing solvers too slow or inaccurate
- Can’t exploit the parallel platforms

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity”
## Power Grid Analysis: In the literature……

### Direct Methods
- **Multigrid** [Najm et. al., TCAD 2002]
- **Hierarchical** [Blaauw et. al., TCAD 2002]
- **MOR** [He et. al., DAC 2002]
- and many more…

### Iterative Methods
- **Krylov-subspace** [Chen et. al., DAC 2001]
- **Successive Over-relaxation** [Wong et. al., ICCAD 2007]
- **Random Walks** [Nassif et. al., TCAD 2005]
- and many more…

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity”
In the literature......

Direct Methods

→ Fast
→ Memory inefficient
→ Sequential process

Iterative Methods

→ Slow
→ Memory efficient
→ Parallelizable

→ Waveform Relaxation based Power Grid Analysis

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity”
WR Overview - Partitioning

Circuit

Points of Weak Coupling
WR Overview - Relaxation

Gauss Seidel

\{ V_1, I_1 \} \rightarrow \{ V_2, I_2 \}

- Better Convergence
- Memory Efficient

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity"
Recent work:

(Dense Coupled Interconnects)


(Dense Coupled Interconnects with FD parameters)


(Large Multiport Networks)


© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity”
Efficient Partitioning Schemes

Improved initial-guess computation

CPU efficient parallelization
Partitioning

How to Partition the Power Grid?

"strong" coupling in all directions in a Power Grid

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity
Voltage Profiles - Sample 50X50 power grid

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity
Block Row Partitioning

Waveform Relaxation sources

*i*th subcircuit

V<sub>DD</sub> contact

Waveform Relaxation sources

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity”
MNA Equation for Power Grids

\[ GX(t) + C \dot{X}(t) = Bu(t) \]

For applying WR, \( X(0) \) is required.

"DC Solution" of the power grid is very expensive!!!

Must Solve:

\[ GX(0) = B_{DC} \]

Proposed \( \Rightarrow \) DC solution is made part of the WR iterations
Estimation of $A_{WR}$

Estimation based on locality in DC solution

[Image of a diagram with a grid and a red area highlighting $A_{WR}$]

[Eli Chiprout, ICCAD 2004]

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity”
Parallelization Schemes

Parallel GS-WR

coupling limited to neighboring block(s)
I. Simulate Odd blocks

II. Update WR sources for Even blocks

III. Simulate Even blocks

IV. Update WR sources for Odd blocks

V. Proceed to next iteration
Enhanced pipelining

Pipelining via physical & time partitioning

- Scales well with the # of BRP partitions
- Scales well with the # of processors
- 100% CPU use ensured if
  \[
  \text{# of time blocks} = \text{# of processors}
  \]
Pipelining via physical & time partitioning

- # ph. blocks – 8
- # iter. – 2
- # procs. – 3
- # time blocks – 3

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity”
Power-Grid: 7.5 million nodes

<table>
<thead>
<tr>
<th>Proposed GS-WR method</th>
<th>Direct- LU (CPU time) (min.)</th>
<th>Speed-Up</th>
</tr>
</thead>
<tbody>
<tr>
<td># CPUs</td>
<td>CPU time (min.)</td>
<td>494</td>
</tr>
<tr>
<td>1</td>
<td>211</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>58</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>31</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>15</td>
<td></td>
</tr>
</tbody>
</table>

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity”
Example: 7.5 million nodes

Speed-Up Curve w.r.t. Direct-LU

© R. Achar, CASS-DLP, Advanced Modeling and Simulation Strategies for Power Integrity"
Conclusions

• Power-Grid Analysis :
  ➢ Large circuits
  ➢ CPU & Memory Intensive

• Emerging Parallel Platforms

• WR algorithms for transient analysis of power-grids
  ➢ Combines the merits of both direct & iterative methods
  ➢ Fast, Memory efficient
  ➢ Parallel & Scalable

Slide Acknowledgements: Prof. Nakhla and Current/Past Graduate students of CAE Group, Dept. of Electronics, Carleton University