Workshop: Relative Timing Driven Asynchronous Design (TDAD)

November 2nd to November 6th 2015
Activity Report
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Within the context of the 2015 Outreach initiative for China and Latin America, IEEE CASS supported this event, held at Universidad Tecnológica Nacional, Facultad Regional Buenos Aires, situ in Buenos Aires, Argentina during the week of November 2 to November 6. 2015.

The speaker Professor Dr Kenneth Stevens (KS) from the Computer Engineering Department University of Utah, Salt Lake city, delivered a series of lectures and recitation sessions that covered theory and design applications on Relative Timing Driven Asynchronous Design of Integrated Circuits, for a total of 22 contact hours. The first hour consisted of an overview of the subject matter to be covered in detail during the remaining hours. KS spelled out the level of knowledge assumed as a prerequisite to successfully exploit the workshop. It permitted a natural selection within the audience which was to continue immersing themselves into the topic. It worked fine, the audience after the first lecture decreased by five and remained at a steady state value of 11 attendants untill the end of workshop. The audience was a combination of graduate and undergraduate students in Electronic Engineering. A companion document provides a summary evaluation of the attendants regarding the overall benefit of the workshop while protecting the anonymity of the students. The setup for the workshop demanded from CAD specialists from UTN (Mr. Sebastian Pazos and Mr. Fernando Aguirre) a couple of days of work for the preparation of an appropriate common environment to become accessible to all the students for the generation and sharing of the design activity. The environment consisted of: EDA tools from the 3 large EDA vendors (Cadence, Mentor & Synopsys): Verilog,

Primetime, CALIBRE, Design Compiler, ICC compiler, enlarged with University of Utah (U of U) / Granite Mountain Technology (GMT) tools for the merging of the support environment to include Relative Timing based Asynchronous design support. The commercial database SQL was also included, due to the significant data complexity support to handle timing constraints in the designs.

After the first introductory hour, the next 8 hours of work, delivered over the course of two days. Monday and Tuesday, were aimed at introducing the concept of relative timing, a key concept in this asynchronous paradigm. During this period, KS went deeper into the required combinational control logic for the asynchronous systems. KS started by lecturing on Petri nets and CCS models, extensively used in *TDAD* (Timing Driven Asynchronous Design) for the representation of combinatorial concurrent systems, during the synthesis of the logic control blocks. The Sorcerer flow and tools were primarily used during these two days. The Flow implements a characterization mechanism based on formal verification of both behavior and timing. This flow being the most complex part of the system demands design expertise that understands the macro control blocks, during formal verification and characterization of these macros. This activity constitutes the low level circuit design.

Wednesday and Thursday were focused on block level synthesis, which included timing analysis between blocks. The Apprentice flow and tools from U of U and GMT were introduced at this time. This flow characterizes macros that leverage the traditional EDA design flow in such a way that these macros can be rapidly assembled and composed into systems. The Apprentice flow enables rapid hardware design in a method that rivals software design (but with more knobs and constraints). Designs macros are characterized in an object oriented fashion so that even those who are not experts can build efficient systems on with first pass correctness using these blocks. The students verified these assertions during Wednesday and Thursday sessions.

The starting point was a Verilog description of the system, with the addition of the macro control blocks. Resulting Verilog code was analyzed using Synopsys tools for testing the satisfaction of timing constraints and propagation delays. This procedure sets up the basis for the analysis and synthesis of larger systems. Precisely this aspect of the design methodology was discussed during the Friday sessions. A comparison between the synchronous and asynchronous versions for several systems, all of them designed by the KS team was shown and is reported in Table I. For these designs, the advantages of the Timing driven asynchronous

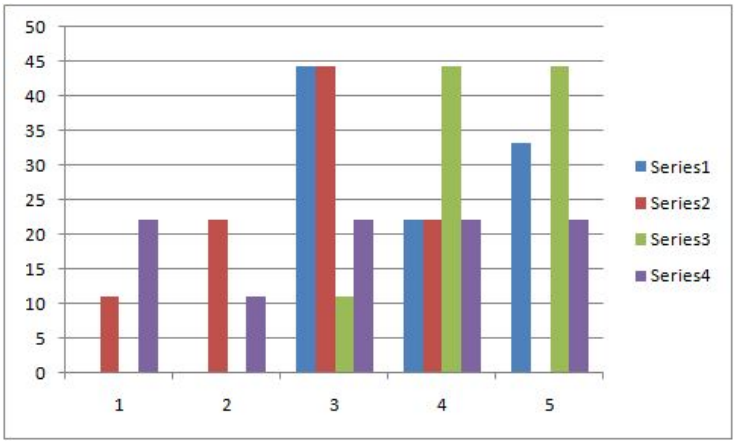
implementation over the synchronous one is apparent. The figure of merit used in the comparisons is energy times performance square.

Table 1: Design comparison between traditional flows and GMT's flows

Design	Energy	Area	Freq.	Latency	Aggregate
Pentium F.E.† [61]	2.05	*0.85*	2.92	2.38	12.11×
10-bit FIFO [25]	2.37	1.61	1.06	2.91	11.77×
2-phase Link* [58]	1.11	0.92	*0.98*	1.77	1.77×
SAS [13, 12, 58]	2.54	1.36	*1.00*	9.54	32.95×
Mixed Signal+	3.25	1.02	*1.00*	*1.00*	3.32×
NoC - Aeth/Orion [23]	4.85	6.54	2.10	1.84	122.56×
NoC - COSI [24]	1.87	5.72	1.19	2.25	28.18
64-pt FFT [35]	2.43	2.42	1.97	3.17	36.72×
UART [2]	3.99	0.92	*1.00*	*1.00*	3.67×
OCP Socket [76]	4.65	1.36	2.75	–	17.39×
MSP-430	6.99	–	0.66	–	4.61×
Cryptography chip	2.25	2.23	0.95	–	4.77×

Clocked design is baseline. Numbers larger than 1.00 are improvements for all metrics. Unless noted, results are for physical layout. Results in darkred compare fabricated designs. *Reports wire area not including transistor area. Frequency reported for closest design match. †Area not optimized in Async test chip. Advantage estimated at 1.6 based on transistor count.

A survey made just after the workshop revealed the following results: 45% of the attendance says the workshop helped them getting used to the tools while they acknowledge the need for additional practice, as expected (Series 1, where 1 implies not having been able to catch up with the course, and 5 to be completely satisfied) . With regard to the subject matter, 45% agree that although they have heard about asynchronous design in generalities, none of them have ever used it (Series 2, where 1 implies an unknown topic and 5 a widely known one). Series 4 shows that the audience had some previous background, where 1 implies no experience at all and 5 to be quite experienced in the field of CMOS design. *Finally 45% of the total audience stated that the workshop completely fulfilled their expectations! (See Series 3)*



Picture No. 1: *This chart plots the results of the survey made after the course: Series 1: "Would you say that this workshop has allowed you to get used with its methods and tools?", Series 2: "Previous Background", Series 3: "Has this workshop fulfilled your expectations?", Series 4: "Do you have any experience in VLSI CMOS design?"*

Photo No. 1: *KS explaining the limits of growth that derive from technology enhancements.*

Photo No. 2: *A view of the audience in class.*